16-Bit, 2MSPS, µModule Data-Acquisition Solution

FEATURES

- Highly performance
  - Throughput: 2MSPS, no latency
  - INL: ±3ppm maximum from −40°C to 105°C
  - Total system dynamic range: 123dB typical
  - SNR: 97.5dBFS typical, THD: −122dBc typical
  - Offset error drift: +5.05µV/°C maximum
  - Gain error drift: +1.17ppm/°C maximum
- Ease of use features reduce system complexity
  - Second-order, 270kHz anti-aliasing filter
  - High-Z PGIA gain options: 1/3, 5/9, 20/9, 20/3
  - Flexible external reference voltage: 4.096V or 5V
  - Differential input voltage ranges, ±REFIN/Gain: ±15V, ±9V, ±2.25V, ±0.75V
  - Wide input common-mode voltage range: −8V to +10V
  - Low input bias current: −30pA typical
- High density solution reduces system footprint
  - 14mm x 9mm, 0.8mm pitch, 178-ball CSP BGA
  - 4× footprint reduction vs. equivalent discrete solution
  - On-board reference buffer with an internal VCM generation
- Total power dissipation: 445mW typical at 2MSPS
- Flexi-SPI digital interface
  - 1, 2, or 4 SDO lanes allows slower SCK
  - Echo clock mode simplifies use of digital isolator
  - Compatible with 1.2V to 1.8V logic
  - PGIA gain control (A0, A1) interface
  - Extended sample resolution to 30-bits
  - Overrange and synchronization bits

APPLICATIONS

- Automatic test equipment
- Machine automation
- Process controls
- Medical and industrial instrumentation
- Digital control loops

FUNCTIONAL BLOCK DIAGRAM

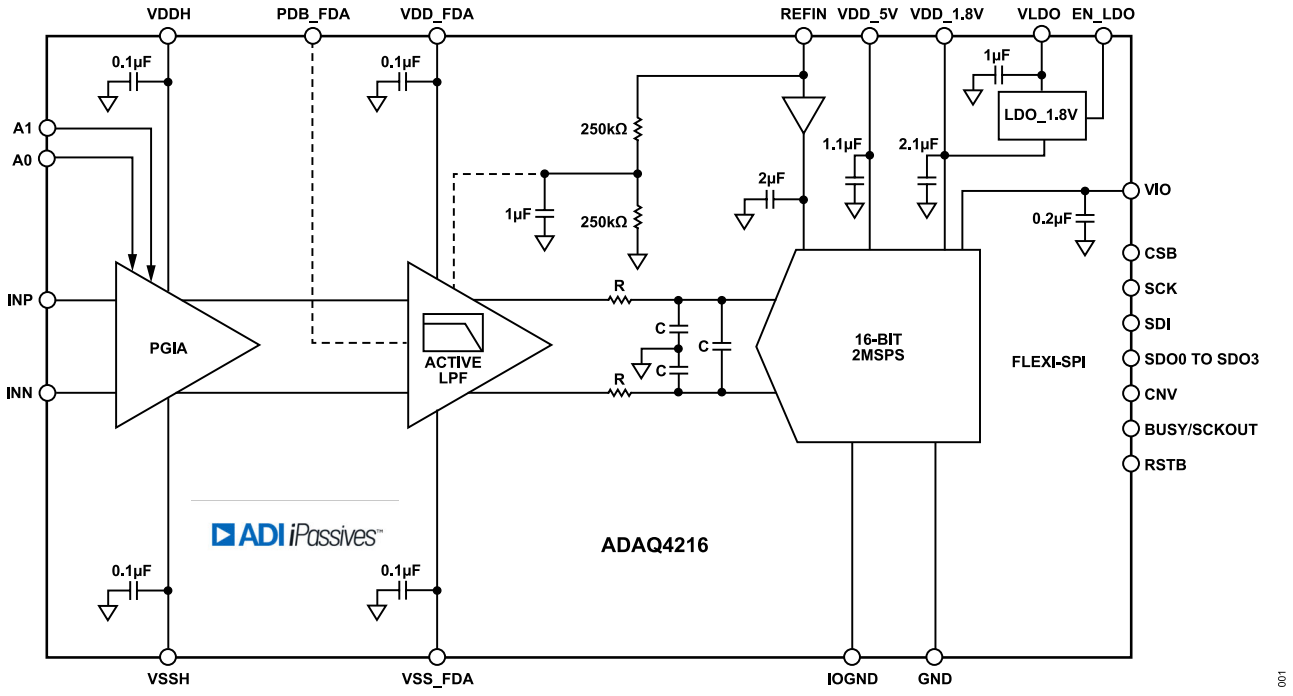


Figure 1. ADAQ4216 Functional Block Diagram

TABLE OF CONTENTS

REVISION HISTORY

1/2025—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADAQ4216 is a µModule® precision data-acquisition (DAQ) signal chain solution that reduces the development cycle of a precision measurement system by transferring the signal-chain design challenge of component selection, optimization, and layout from the designer to the device. With a guaranteed maximum ±3ppm INL and no missing codes at 16 bits, the ADAQ4216 achieves unparalleled precision from −40°C to +105°C.

Using system-in-package (SIP) technology, the ADAQ4216 combines the common signal processing blocks required in a data-acquisition solution in a small footprint, 14mm × 9mm, 0.8mm pitch, 178-ball CSP_BGA package.

The ADAQ4216 integrates the following:

- A low-noise, high-bandwidth programmable gain instrumentation amplifier (PGIA).
- A second-order anti-aliasing filter.
- A low-noise, low-distortion, high-bandwidth analog-to-digital converter (ADC) driver.
- A high precision 16-bit, 2MSPS successive approximation register (SAR) ADC.
- A 1.8V low dropout (LDO) regulator.
- Performance critical passives.

The ADAQ4216 incorporates the critical passive components with superior matching and drift characteristics using Analog Devices, Inc., *i*Passives® technology to minimize temperature-dependent error sources and to offer optimized performance. Integrating the critical power supply and reference bypass capacitors reduce sensitivity to the system level board layout. Reducing the solution footprint enables addition of more functions within the system and hence the smaller form factor instruments without sacrificing performance.

The system integration solves many design challenges while the µModule still provides the flexibility of a configurable PGIA, which allows gain or attenuation and supporting the acquisition of differential or single-ended input signal. The fast settling of the PGIA and ADC driver stage and no latency of the SAR ADC provide a unique solution for high channel count, multiplexed signal chain architectures, and control loop applications.

The digital features include Flexi-SPI serial-peripheral interface (SPI), which allow data access by multiple SPI modes as well as offset correction, gain adjustment, and averaging. The digital features reduces the burden on the host processor. A wide-data clocking window, multiple SDO lanes, and optional DDR data clocking reduce the serial clock frequency while operating at full speed of 2MSPS and make it easier to isolate the DAQ solution, which reduces power dissipation and EMI. The echo clock mode and host clock mode of the ADAQ4216 relax the timing requirements and simplify the use of digital isolators.

The Flexi-SPI serial-user interface is compatible with 1.2V to 1.8V using a separate VIO supply. The ADAQ4216 operation is specified from −40°C to +105°C.

SPECIFICATIONS

V_{DDH} = 18V, V_{SSH} = −18V, VDD_FDA = 5.4V, VSS_FDA = 0V, VDD_5V = 5.4V, V_{LDO} = 5.4V, V_{IO} = 1.8V, REFIN = 5V, f_S = 2MSPS, all gains, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
DIFFERENTIAL INPUT VOLTAGE RANGE, V_{IN}	V_{IN} = ±REFIN/Gain				
	Gain = 1/3	−15		+15	V
	Gain = 5/9	−9		+9	V
	Gain = 20/9	−2.25		+2.25	V
	Gain = 20/3	−0.75		+0.75	V
Analog Font-End Gain (G)	A0 = low, A1 = low		1/3		V/V
	A0 = high, A1 = low		5/9		V/V
	A0 = low, A1 = high		20/9		V/V
	A0 = high, A1 = high		20/3		V/V
Input Common-Mode Voltage Range	All gains	−8		+10	V
Common-Mode Rejection Ratio (CMRR)	DC		95		dB
Input Current[1]	INP, INN, T_A=25°C	−130	−30	+75	pA
Input Resistance	INP, INN		10^{12}		Ω
Input Capacitance	INP, INN		22		pF
THROUGHPUT					
Complete Cycle		500			ns
Conversion Time		264	282	300	ns
Acquisition Phase[2]		244	260	275	ns
Throughput Rate		0		2	MSPS
DC ACCURACY					
No Missing Codes		16			Bits
Integral Nonlinearity Error (INL)[1]	All gains, VSS_FDA = 0V	−3	±1	+3	ppm
Differential Nonlinearity Error (DNL)[1]	All gains, VSS_FDA = 0V		±0.5		LSB
Transition Noise	G = 1/3		0.29		LSBrms
	G = 5/9		0.18		LSBrms
	G = 20/9		0.05		LSBrms
	G = 20/3		0.03		LSBrms
Offset Error	G = 1/3	−1.0	±0.10	+1.0	mV
	G = 5/9	−1.1	±0.11	+1.1	mV
	G = 20/9	−1.2	±0.13	+1.2	mV
	G = 20/3	−1.8	±0.23	+1.8	mV
Offset Error Drift	T= −40°C to 105°C, End point method				
	G = 1/3, 5/9, 20/9	−8.27	±2.35	+3.82	µV/°C
	G = 20/3	−11.93	±3.44	+5.05	µV/°C
Gain Error	REFIN = 5V	−0.06	±0.006	+0.06	%FS
Gain Error Drift	REFIN = 5V, T= −40°C to 105°C, End point method				
	All gains	−1.03	±0.07	+1.17	ppm/°C
Power-Supply Rejection Ratio (PSRR)	V_{DDH} = +15V to +18V step		122		dB
	V_{SSH} = −15V to −18V step		129		dB
	VDD_FDA = +4.5V to +5.5V step		109		dB
	VSS_FDA = 0V to −1V step		104		dB
	VDD_5V = +5.3V to +5.5V step		109		dB
	V_{LDO} = + 5.3V to +5.5V step		113		dB
Low Frequency Noise[3]	Bandwidth = 0.1Hz to 10Hz		6		µV p-p

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AC ACCURACY					
Dynamic Range	G = 1/3		97.6		dB
	G = 5/9		97.5		dB
	G = 20/9		97.4		dB
	G = 20/3		96.7		dB
Total System Dynamic Range			123		dB
Noise Spectral Density (NSD)	f_{IN} = 1kHz				
	G = 1/3		214.7		nV/$\sqrt{Hz}$
	G = 5/9		130.3		nV/$\sqrt{Hz}$
	G = 20/9		34.2		nV/$\sqrt{Hz}$
	G = 20/3		13		nV/$\sqrt{Hz}$
Total RMS Noise,RTI	G = 1/3		139.8		μV_{RMS}
	G = 5/9		84.9		μV_{RMS}
	G = 20/9		21.5		μV_{RMS}
	G = 20/3		7.8		μV_{RMS}
Signal-to-Noise Ratio (SNR)	f_{IN} = 1kHz, −0.5dBFS				
	G = 1/3	96.5	97.5		dBFS
	G = 5/9	96.4	97.4		dBFS
	G = 20/3	96.3	97.3		dBFS
	G = 20/3	95.1	96.1		dBFS
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1kHz, −0.5dBFS				
	G = 1/3		122		dBc
	G = 5/9		118		dBc
	G = 20/9		122		dBc
	G = 20/3		122		dBc
Total Harmonic Distortion (THD)	f_{IN} = 1kHz, −0.5dBFS				
	G = 1/3	−114	−122		dBc
	G = 5/9	−105.5	−118		dBc
	G = 20/9	−115.5	−122		dBc
	G = 20/3	−115.5	−122		dBc
Signal-to-Noise-and-Distortion (SINAD) Ratio	f_{IN} = 1kHz, −0.5dBFS				
	G = 1/3	96.4	97.4		dBFS
	G = 5/9	96.3	97.3		dBFS
	G = 20/9	96.2	97.2		dBFS
	G = 20/3	95	96		dBFS
Oversampled Dynamic Range	OSR = 2		99		dB
	OSR = 1024		128		dB
−3dB Input Bandwidth	$V_{OUTDIFF}$ = 2V p-p				
	G = 1/3		270		kHz
	G = 5/9		270		kHz
	G = 20/9		250		kHz
	G = 20/3		225		kHz
Aperture Delay			0.7		ns
Aperture Jitter			1.4		ps rms

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE BUFFER	External reference drives REFIN				
REFIN Voltage Range	5.3V ≤ VDD_5V ≤ 5.5V	4.95	5	5.05	V
	4.75V ≤ VDD_5V ≤ 5.25V	4.046	4.096	4.146	V
REFIN Bias Current	REFIN = 5V		10	13.5	µA
REFIN Input Impedance			500		kΩ
REFIN Input Capacitance			40		pF
Reference Buffer Offset Error	REFIN = 5V or 4.096V, T_A = 25°C	−150	±20	+150	µV
Reference Buffer Offset Drift			±0.3		µV/°C
Power-On Settling Time			3		ms
DIGITAL INPUTS, ADC	1.14V ≤ VIO ≤ 1.89V				
Logic Levels					
Input Voltage Low (V_{IL})		−0.3		+0.35 × V_{IO}	V
Input Voltage High (V_{IH})		0.65 × V_{IO}		V_{IO} + 0.3	V
Input Current Low (I_{IL})		−10		+10	µA
Input Current High (I_{IH})		−10		+10	µA
Input Pin Capacitance			2		pF
DIGITAL INPUTS, A0, A1					
Logic Levels					
Input Voltage Low (V_{IL})		2			V
Input Voltage High (V_{IH})				0.8	V
Input Current (I_{IL} or I_{IH})			0.002		µA
Input Pin Capacitance			2		pF
DIGITAL INPUT, FDA					
PDB_FDA Input Current	PDB_FDA = FDD_FDA or 0V		50		µA
DIGITAL OUTPUTS	1.14V ≤ VIO ≤ 1.89V	Conversion results available immediately after completed conversion			
Pipeline Delay					
Output Voltage Low (V_{OL})	Sink Current (I_{SINK}) = 2mA			0.25 × V_{IO}	V
Output Voltage High (V_{OH})	Source Current (I_{SOURCE}) = 2mA	0.75 × V_{IO}			V
LDO CHARACTERISTICS					
VDD_1.8V Output Voltage		1.71	1.8	1.89	V
Load Regulation	I_{OUT} = 1mA to 100mA		0.003		%/mA
Dropout Voltage[4]	I_{OUT} = 100mA		45		mV
Start-up Time [5]			200		µs
Current Limit Threshold			260		mA
EN_LDO Input Current	EN_LDO = VLDO		0.001	1	µA
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			15		°C
POWER SUPPLIES					
V_{DDH}			18		V
V_{SSH}			−18		V
VDD_FDA		3	5	VSS_FDA +10	V
VSS_FDA		VDD_FDA − 10	0	+0.1	V
VDD_5V	REFIN = 5V	5.3	5.4	5.5	V
	REFIN = 4.096V	4.75	5	5.25	V
VDD_1.8V		1.71	1.8	1.89	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{IO}[6]		1.14		1.89	V
V_{LDO}		2.2	5.4	5.5	V
Standby Current	Inputs grounded				
V_{DDH}			8		mA
V_{SSH}			−9		mA
VDD_FDA			4.8		mA
VSS_FDA			−3.5		mA
VDD_5V			525		µA
V_{IO}			<1		µA
V_{LDO}			108		µA
Shutdown Current	Inputs grounded				
VDD_FDA	PDB_FDA = 0V		32		µA
VSS_FDA	PDB_FDA = 0V		−25.2		µA
VDD_5V	ADC in shutdown mode		5		µA
V_{IO}			<1		µA
V_{LDO}	EN_LDO = 0V, ADC in shutdown mode		0.8		µA
Operating Current	2MSPS, Input = −0.5dBFS				
V_{DDH}	V_{DDH} = +18V		10		mA
V_{SSH}	V_{SSH} = −18V		−9.8		mA
VDD_5V	VDD_5V = 5.4V		2.5	3.2	mA
VDD_FDA	VDD_FDA = 5.4V		5.6	7.5	mA
VSS_FDA	VSS_FDA = 0V	−7.5	−5.6		mA
V_{IO}	V_{IO} = 1.8V, 1-lane SDO		0.8		mA
V_{LDO}	V_{LDO} = 5.4V		8	10.5	mA
Power Dissipation	2MSPS		445		mW
t_{RESET_DELAY}	After power-on, delay from VDD_5V and VDD_1.8V valid to $\overline{RST}$ assertion	3			ms
t_{RESET_PW}	$\overline{RST}$ pulse width	50			ns
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+105	°C

[1] These specification are not production tested but are supported by characterization data during initial product release.

[2] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2MSPS.

[3] See the low frequency noise plot in Figure 63. 1/f noise is canceled internally by auto-zeroing. Noise spectral density is substantially uniform from DC to $f_S/2$.

[4] Drop-out voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage.

[5] Start-up time is defined as the time between the rising edge of EN_LDO to VDD_1.8V being at 90% of its nominal value.

[6] When VIO < 1.4 V, Bit IO2X must be set to 1. For more details, see the Output Driver Register section.

TIMING SPECIFICATIONS

V_{DDH} = 18V, V_{SSH} = −18V, VDD_FDA = 5.4V, VSS_FDA = 0V, VDD_5V = 5.4V, V_{LDO} = 5.4V, V_{IO} = 1.8V, REFIN = 5V, f_S = 2MSPS and all specifications are T_{MIN} to T_{MAX}, unless otherwise noted. For the timing voltage levels, see Figure 2. For V_{IO} < 1.4V, Bit IO2X must be set to 1.

Table 2. Digital Timing Interface

Parameter[1]	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	264	282	300	ns
Acquisition Phase[2]	t_{ACQ}	244	260	275	ns
Time Between Conversions	t_{CYC}	500			ns
CNV High Time	t_{CNVH}	10			ns

SPECIFICATIONS

Table 2. Digital Timing Interface (Continued)

Parameter[1]	Symbol	Min	Typ	Max	Unit
CNV Low Time	t_{CNVL}	20			ns
Internal Oscillator Frequency	f_{OSC}	75.1	80	84.7	MHz

[1] Timing specifications assume a 5pF load capacitance on digital output pins. t_{CONV}, t_{CYC}, t_{SCK}, and t_{SCKOUT} are production tested. All other timing specifications are guaranteed by characterization and design.

[2] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2MSPS.

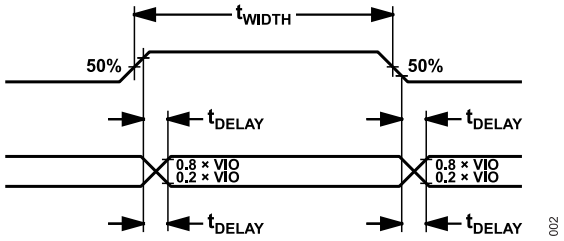


Figure 2. Voltage Levels for Timing

Table 3. Register Read/Write Timing

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ Pulse Width	t_{CSPW}	10			ns
SCK Period	t_{SCK}				
V_{IO} > 1.71V		11.6			ns
V_{IO} > 1.14V		12.3			ns
SCK Low Time	t_{SCKL}	5.2			ns
SCK High Time	t_{SCKH}	5.2			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	2.1			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
V_{IO} > 1.71V				9.4	ns
V_{IO} > 1.14V				11.8	ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			9	ns
SDI Valid Setup Time to SCK Rising Edge	t_{SSDI}	1.5			ns
SDI Valid Hold Time from SCK Rising Edge	t_{HSDI}	1.5			ns
$\overline{CS}$ Falling Edge to First SCK Rising Edge	t_{CSSCK}				
V_{IO} > 1.71V		11.6			ns
V_{IO} > 1.14V		12.3			ns
Last SCK Edge to $\overline{CS}$ Rising Edge	t_{SCKCS}	5.2			ns

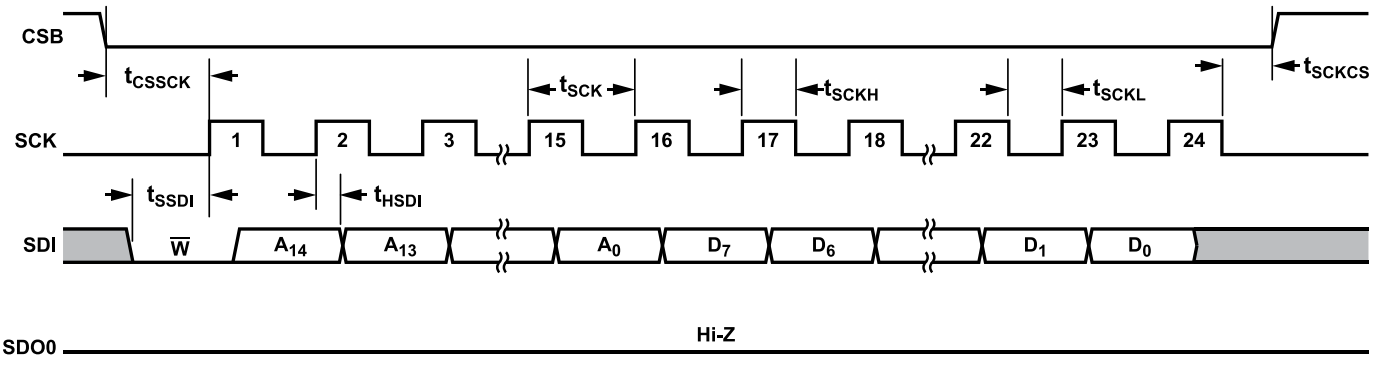


Figure 3. Register Configuration Mode Write Timing

SPECIFICATIONS

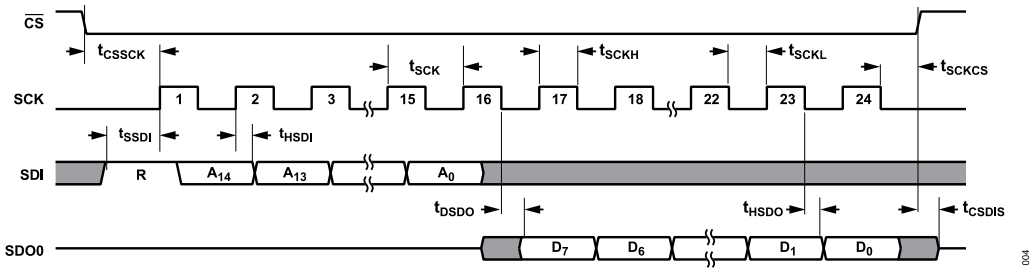


Figure 4. Register Configuration Mode Read Timing

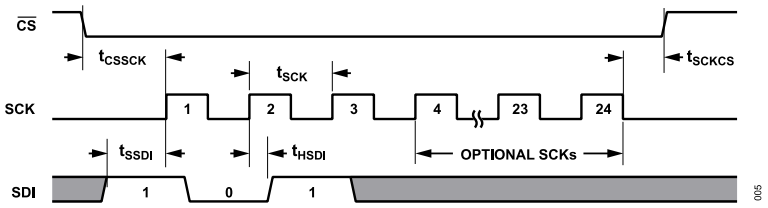


Figure 5. Register Configuration Mode Command Timing

Table 4. SPI-Compatible Mode Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK Period	t_{SCK}				
V_{IO} > 1.71V		9.8			ns
V_{IO} > 1.14V		12.3			ns
SCK Low Time	t_{SCKL}				
V_{IO} > 1.71V		4.2			ns
V_{IO} > 1.14V		5.2			ns
SCK High Time	t_{SCKH}				
V_{IO} > 1.71V		4.2			ns
V_{IO} > 1.14V		5.2			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	1.4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
V_{IO} > 1.71V				5.6	ns
V_{IO} > 1.14V				8.1	ns
$\overline{CS}$ Falling Edge to SDO Valid	t_{CSEN}				ns
V_{IO} > 1.71V				6.8	ns
V_{IO} > 1.14V				9.3	ns
$\overline{CS}$ Falling Edge to First SCK Rising Edge	t_{CSSCK}				
V_{IO} > 1.71V		9.8			ns
V_{IO} > 1.14V		12.3			ns
Last SCK Edge to $\overline{CS}$ Rising Edge	t_{SCKCS}	4.2			ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			9	ns
$\overline{CS}$ Falling Edge to BUSY Rising Edge	t_{CSBUSY}		6		ns

SPECIFICATIONS

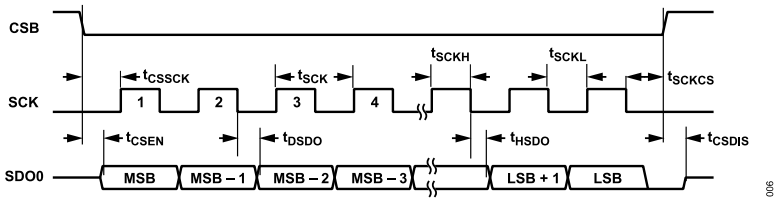


Figure 6. SPI Clocking Mode 1-Lane SDR Timing

Table 5. Echo-Clock Mode Timing, SDR, 1-Lane

Parameter	Symbol	Min	Typ	Max	Unit
SCK Period	t_{SCK}				
V_{IO} > 1.71V		9.8			ns
V_{IO} > 1.14V		12.3			ns
SCK Low Time, SCK High Time	t_{SCKL}, t_{SCKH}				
V_{IO} > 1.71V		4.2			ns
V_{IO} > 1.14V		5.2			ns
SCK Rising Edge to Data/SCKOUT Remains Valid	t_{HSDO}	1.1			ns
SCK Rising Edge to Data/SCKOUT Valid Delay	t_{DSDO}				
V_{IO} > 1.71V				5.6	ns
V_{IO} > 1.14V				8.1	ns
$\overline{CS}$ Falling Edge to First SCK Rising Edge	t_{CSSCK}				
V_{IO} > 1.71V		9.8			ns
V_{IO} > 1.14V		12.3			ns
Skew Between Data and SCKOUT	t_{SKEW}	−0.4	0	+0.4	ns
Last SCK Edge to $\overline{CS}$ Rising Edge	t_{SCKCS}	4.2			ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			9	ns

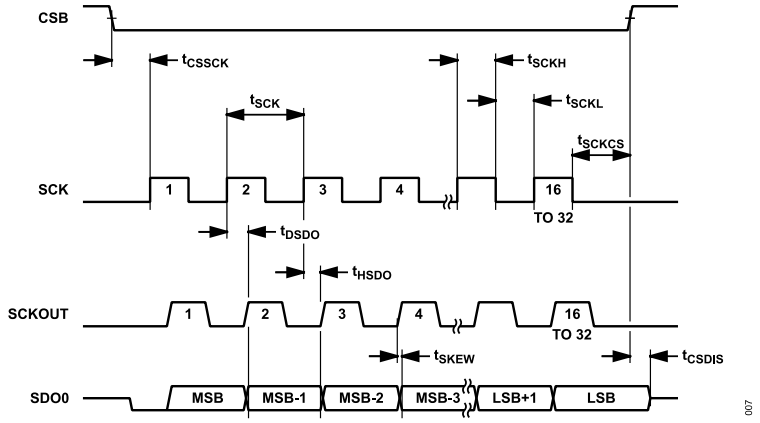


Figure 7. Echo-Clock Mode Timing, SDR, 1-Lane

Table 6. Echo-Clock Mode Timing, DDR, 1-Lane

Parameter	Symbol	Min	Typ	Max	Unit
SCK Period	t_{SCK}	12.3			ns
SCK Low Time, SCK High Time	t_{SCKL}, t_{SCKH}	5.2			ns
SCK Edge to Data/SCKOUT Remains Valid	t_{HSDO}	1.1			ns
SCK Edge to Data/SCKOUT Valid Delay	t_{DSDO}				
V_{IO} > 1.71V				6.2	ns
V_{IO} > 1.14V				8.7	ns

SPECIFICATIONS

Table 6. Echo-Clock Mode Timing, DDR, 1-Lane (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ Falling Edge to First SCK Rising Edge	t_{CSSCK}	12.3			ns
Skew Between Data and SCKOUT	t_{SKEW}	−0.4	0	+0.4	ns
Last SCK Edge to $\overline{CS}$ Rising Edge	t_{SCKCS}	9			ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			9	ns

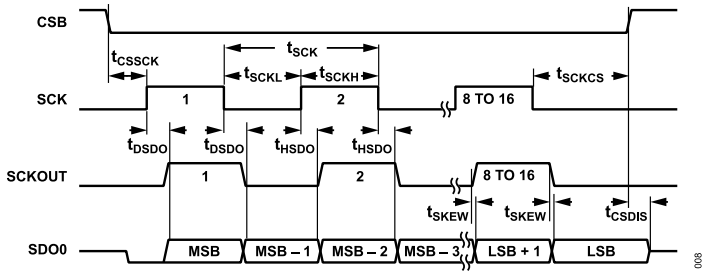


Figure 8. Echo-Clock Mode Timing, DDR, 1-Lane

Table 7. Host-Clock Mode Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCK Period	t_{SCKOUT}				
OSC_DIV = No Divide		11.8	12.5	13.3	ns
OSC_DIV = Divide by 2		23.6	25	26.6	ns
OSC_DIV = Divide by 4		47.4	50	53.2	ns
SCK Low Time	$t_{SCKOUTL}$	0.45 × t_{SCKOUT}		0.55 × t_{SCKOUT}	ns
SCK High Time	$t_{SCKOUTH}$	0.45 × t_{SCKOUT}		0.55 × t_{SCKOUT}	ns
$\overline{CS}$ Falling Edge to First SCKOUT Rising Edge	$t_{DSCKOUT}$				
V_{IO} > 1.71V		10	13.6	19	ns
V_{IO} > 1.14V		10	15	21	ns
Skew Between Data and SCKOUT	t_{SKEW}	−0.4	0	+0.4	ns
Last SCKOUT Edge to $\overline{CS}$ Rising Edge	$t_{SCKOUTCS}$	5.2			ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{CSDIS}			9	ns

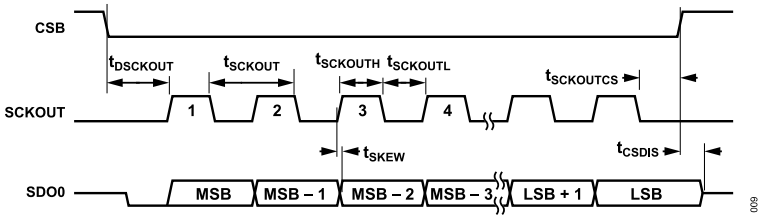


Figure 9. Host-Clock Mode Timing, SDR, 1-Lane

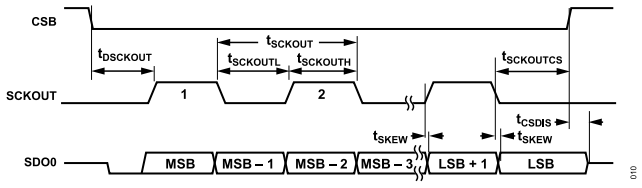


Figure 10. Host-Clock Mode Timing, DDR, 1-Lane

ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Parameter	Rating
Analog Inputs	
Input Voltage, INP, INN	V_{SSH} − 0.2V to V_{DDH} + 0.2V
REFIN to GND	−0.3V to VDD_5V + 0.3V
Input Current[1]	±20mA
Supply Voltage	
V_{DDH} to V_{SSH}	40V
VDD_FDA to GND	11V
VDD_5V to GND	−0.3V to +6.0V
V_{IO} to GND	−0.3V to +2.1V
V_{LDO} to GND	−0.3V to +6.5V
Digital Inputs to GND	−0.3V to V_{IO} + 0.3V
CNV to GND	−0.3V to V_{IO} + 0.3V
Digital Outputs to GND	−0.3V to V_{IO} + 0.3V
Temperature	
Storage Range	−55°C to +150°C
Operating Junction Range	−40°C to +105°C
Maximum Reflow (Package Body)	260°C

[1] The input pins have clamp diodes connected to the power supply pins. Whenever input signals exceed the power supply rail by 0.3V, limit the input current to 20mA or less.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOT}	Ψ_{JT}	Unit
BC-178-2	28.96	22.60	14.09	14.03	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field-induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADAQ4216

Table 10. ADAQ4216, 178-Ball CSP_BGA

ESD Model	Withstand Threshold (kV)	Class
HBM	±4	3A
FICDM	±1	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

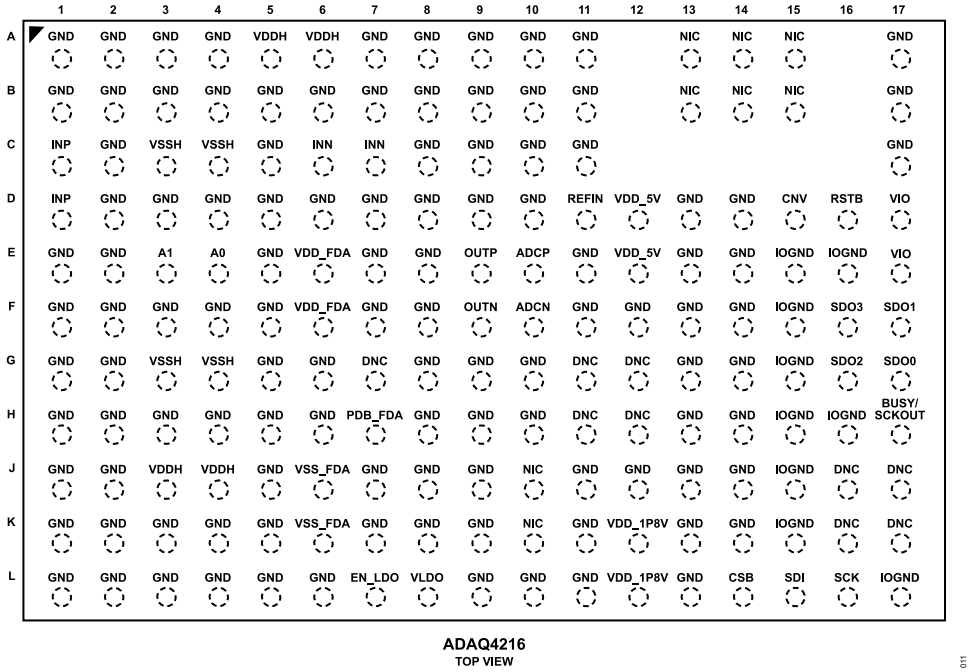


Figure 11. Pin Configuration

Table 11. Pin Function Descriptions

Pin Number	Mnemonic	Type[1]	Description
A1 to A4, A7 to A11, A17, B1 to B11, B17, C2, C5, C8 to C11, C17, D2 to D10, D13 to D14, E1 to E2, E5, E7 to E8, E11, E13 to E14, F1 to F5, F7 to F8, F11 to F14, G1 to G2, G5 to G6, G8 to G10, G13 to G14, H1 to H6, H8 to H10, H13 to H14, J1 to J2, J5, J7 to J9, J11 to J14, K1 to K5, K7 to K9, K11, K13 to K14, L1 to L6, L9 to L11, L13	GND	P	Power Supply Ground.
A5 to A6, J3 to J4	VDDH	P	PGIA Positive Power Supply. This pin has a 0.1µF bypass capacitor inside the package.
C1, D1	INP	AI	Positive Analog Input. Do not leave the INP pin floating. Leaving the INP pin floating can cause the PGIA to draw a larger current from the VDDH and VSSH supply.
C3 to C4, G3 to G4	VSSH	P	PGIA Negative Power Supply. This pin has a 0.1µF bypass capacitor inside the package.
C6 to C7	INN	AI	Negative Analog Input. Do not leave the INN pin floating. Leaving the INN pin floating can cause the PGIA to draw a larger current from the VDDH and VSSH supply.
D11	REFIN	AI	Reference Input. Drive REFIN with 4.096V to 5V (referred to ground). This pin is the input of the internal reference buffer and has a 2µF bypass capacitor at the output of the buffer.
D12, E12	VDD_5V	P	5V Power Supply. The range of VDD_5V depends on the reference value, 5.3V to 5.5V for a 5V reference, and 4.75V to 5.25V for a 4.096V reference. This pin has a 1µF and 0.1µF bypass capacitors inside the package.
D15	CNV	DI	Convert Input. A rising edge on this input powers up the device and initiates a new conversion. This signal must have low jitter to achieve the specified performance of the ADC. Logic levels are determined by the VIO pin.
D16	RSTB	DI	Reset Input (Active Low). Asynchronous ADC reset.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 11. Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Type[1]	Description
D17, E17	VIO	P	Input/Output Interface Digital Power. Nominally, this pin is at the same supply as the host interface (1.8V, 1.5V, or 1.2V). This pin has a 0.2µF bypass capacitor inside the package. For V_{IO} < 1.4V, Bit IO2X of the output driver register must be set to 1.
E3	A1	DI	PGIA Gain-Control Logic Input 1.
E4	A0	DI	PGIA Gain-Control Logic Input 0.
E6, F6	VDD_FDA	P	FDA Positive Power Supply. This pin has a 0.1µF bypass capacitor inside the package. Bypass this pin to GND with at least 2.2µF (0402, X5R) ceramic capacitor.
E9	OUTP	AO	Positive FDA Output.
E10	ADCP	AI	Positive ADC Input.
E15 to E16, F15, G15, H15 to H16, J15, K15, L17	IOGND	P	VIO Ground. Connect to the same ground plane as all GND pins.
F9	OUTN	AO	Negative FDA Output.
F10	ADCN	AI	Negative ADC Input.
F16	SDO3	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
F17	SDO1	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
G7, G11 to G12, H11 to H12	DNC		Do Not Connect.
G16	SDO2	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
G17	SDO0	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
H7	PDB_FDA	DI	Power-Down FDA. Active low. Connect the PDB_FDA pin to GND to power down the FDA. Otherwise, connect the PDB_FDA pin to VDD_FDA logic high supply.
H17	BUSY_SCKOUT	DO	BUSY Indicator in SPI Clocking Mode. This pin goes high at the start of a new conversion and returns low when the conversion finishes. Logic levels are determined by the VIO pin. When SCKOUT is enabled, this pin function is either an echo of the incoming SCK from the host controller or a clock sourced by the internal oscillator.
J6, K6	VSS_FDA	P	FDA Negative Supply. This pin has a 0.1µF bypass capacitor inside the package. Bypass this pin to GND with at least 2.2µF (0402, X5R) ceramic capacitor. Connect to GND for fewer power supply rails.
A13 to A15, B13 to B15, J10, K10	NIC		Not Internally Connected. These pins are not connected internally.
J16 to J17, K16 to K17	DNC		Do Not Connect. These pins are internally connected to digital output drivers in high-Z mode.
K12, L12	VDD_1.8V	P	LDO Voltage Output. The output is typically at 1.8V. This pin has a 1µF and 0.1µF bypass capacitors inside the package.
L7	EN_LDO	DI	Enable LDO pin. For automatic start-up, connect EN_LDO to VLDO.
L8	VLDO	P	Internal LDO Input Supply. This pin has a 1µF bypass capacitor inside the package. The input range for VLDO is 2.2V to 5.5V.
L14	CSB	DI	Chip Select Input (Active Low).
L15	SDI	DI	Serial Data Input.
L16	SCK	DI	Serial-Data Clock Input. When the device is selected (CSB = low), the conversion result is shifted out by this clock.

[1] AI is analog input, AO is analog output, P is power, DI is digital input, and DO is digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DDH} = 18V, V_{SSH} = −18V, VDD_FDA = 5.4V, VSS_FDA = 0V, VDD_5V = 5.4V, V_{LDO} = 5.4V, V_{IO} = 1.8V, REFIN = 5V, f_S = 2MSPS and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

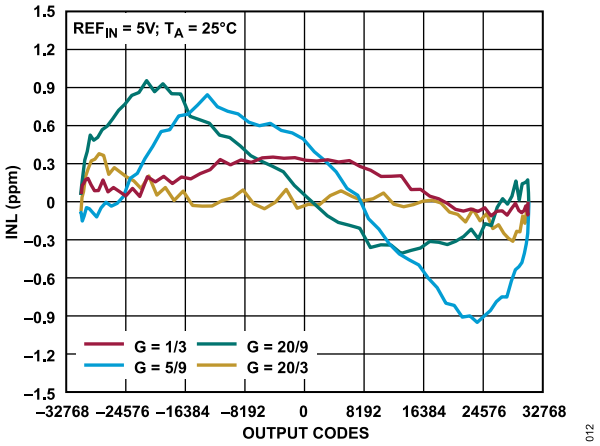


Figure 12. INL Error vs. Output Code, Differential Input, REFIN = 5V

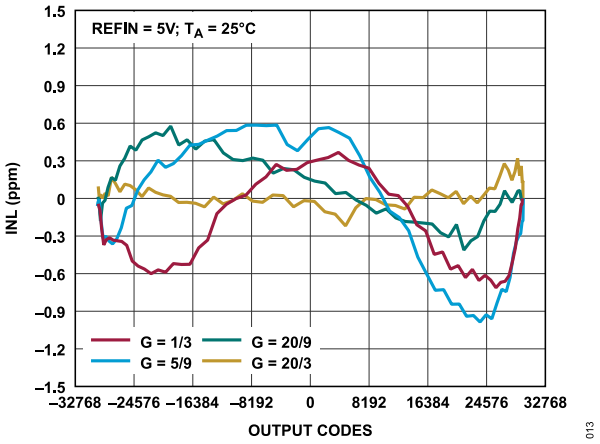


Figure 13. INL Error vs. Output Code, Single-Ended Input, REFIN = 5V

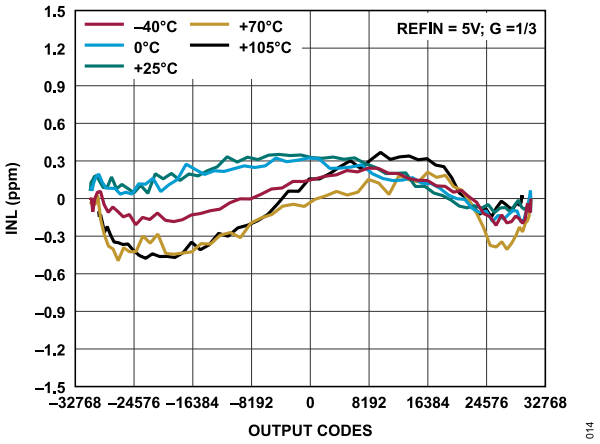


Figure 14. INL Error vs. Output Code across Temperature, G = 1/3

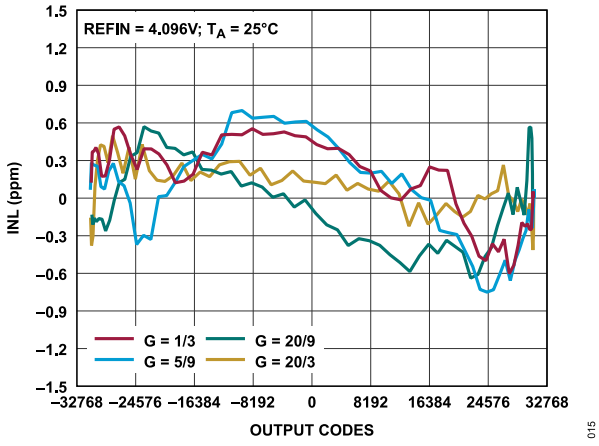


Figure 15. INL Error vs. Output Code, Differential Input, REFIN = 4.096V

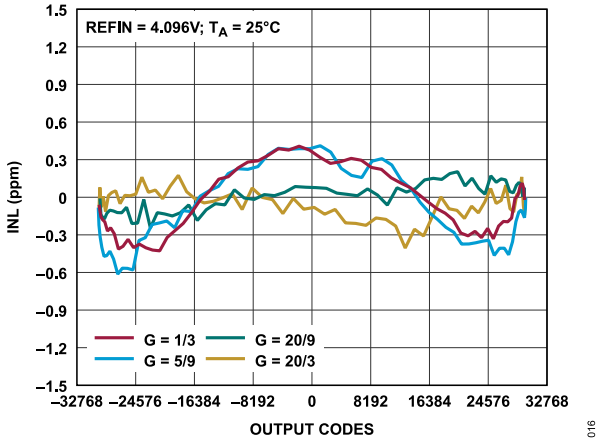


Figure 16. INL Error vs. Output Code, Single-Ended Input, REFIN = 4.096V

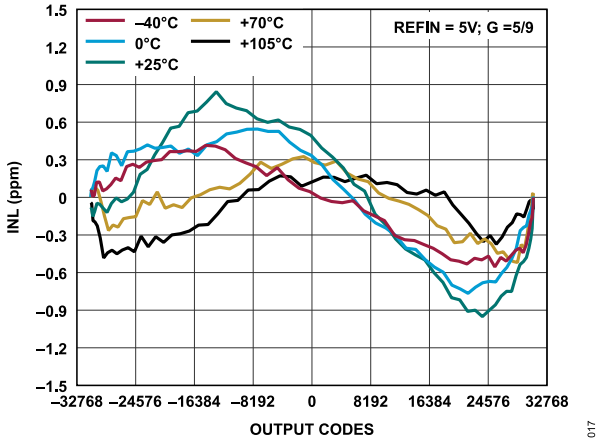


Figure 17. INL Error vs. Output Code across Temperature, G = 5/9

TYPICAL PERFORMANCE CHARACTERISTICS

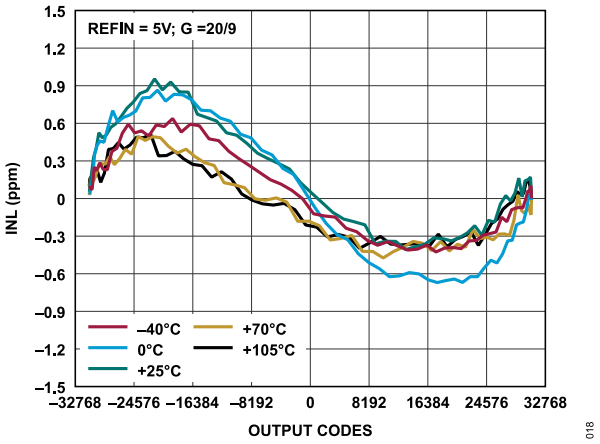


Figure 18. INL Error vs. Output Code across Temperature, G = 20/9

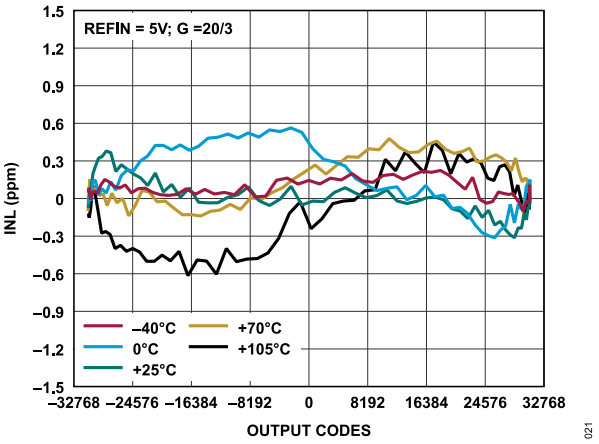


Figure 21. INL Error vs. Output Code across Temperature, G = 20/3

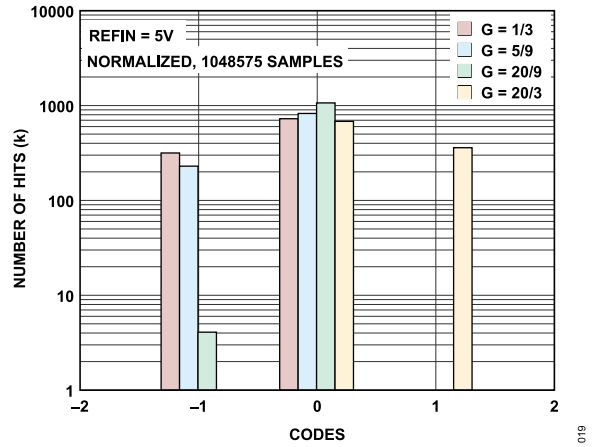


Figure 19. Code Histogram for Shorted Inputs, REFIN = 5V

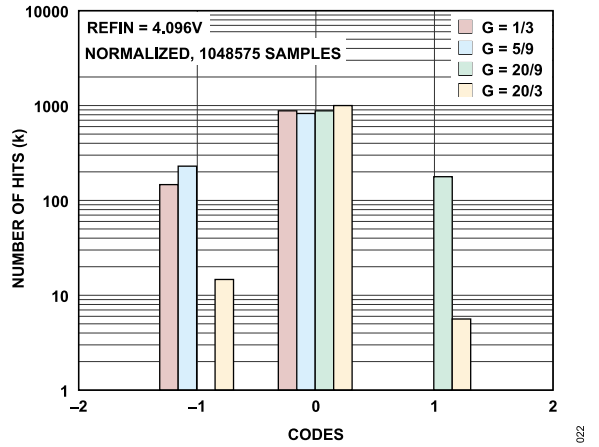


Figure 22. Code Histogram for Shorted Inputs, REFIN = 4.096V

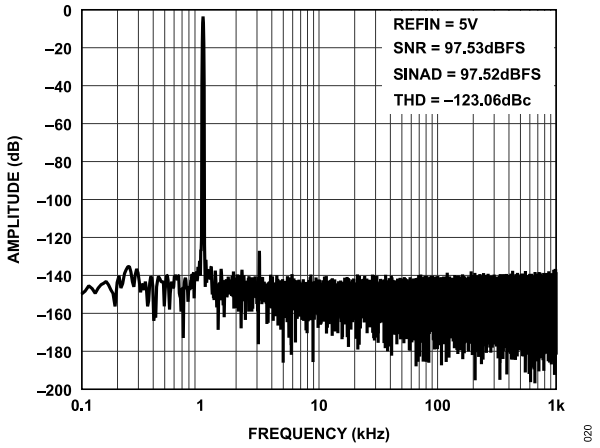


Figure 20. FFT, 2MSPS, f_{IN} = 1kHz, Differential Input = −0.5dBFS, G = 1/3, REFIN = 5V

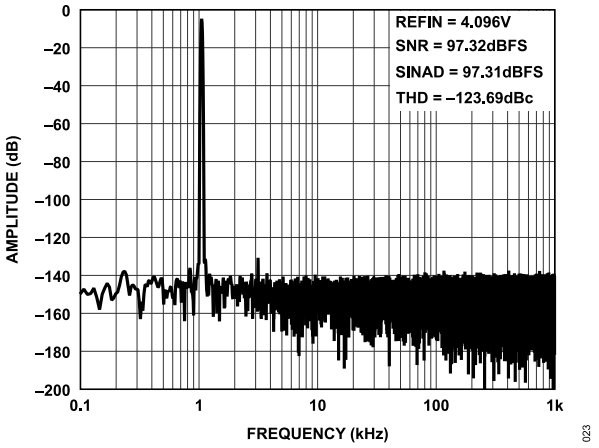


Figure 23. FFT, 2MSPS, f_{IN} = 1kHz, Differential Input = −0.5dBFS, G = 1/3, REFIN = 4.096V

TYPICAL PERFORMANCE CHARACTERISTICS

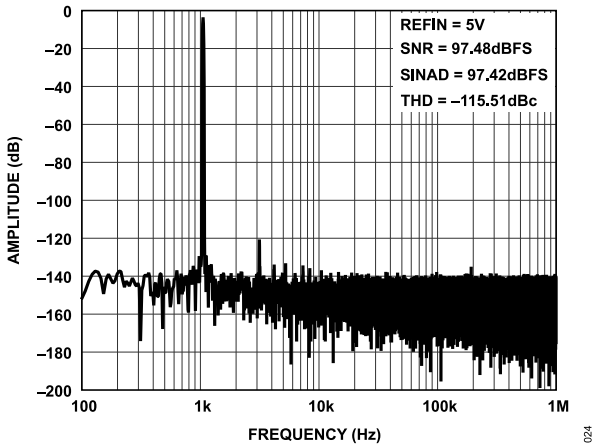


Figure 24. FFT, 2MSPS, f_{IN} = 1kHz, Differential Input = −0.5dBFS, G = 5/9, REFIN = 5V

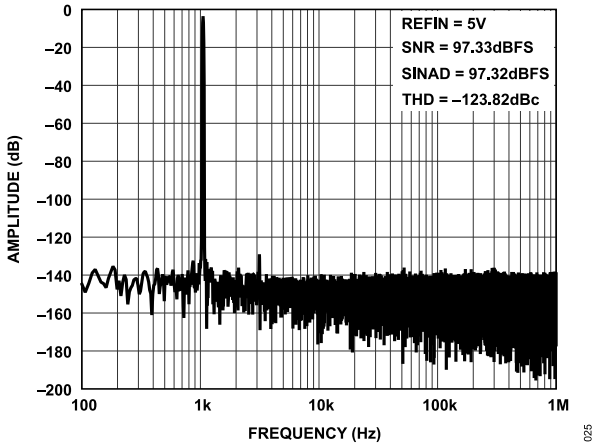


Figure 25. FFT, 2MSPS, f_{IN} = 1kHz, Differential Input = −0.5dBFS, G = 20/9, REFIN = 5V

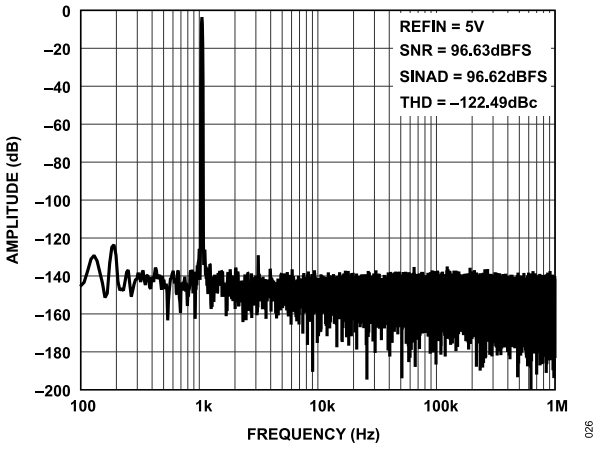


Figure 26. FFT, 2MSPS, f_{IN} = 1kHz, Differential Input = −0.5dBFS, G = 20/3, REFIN = 5V

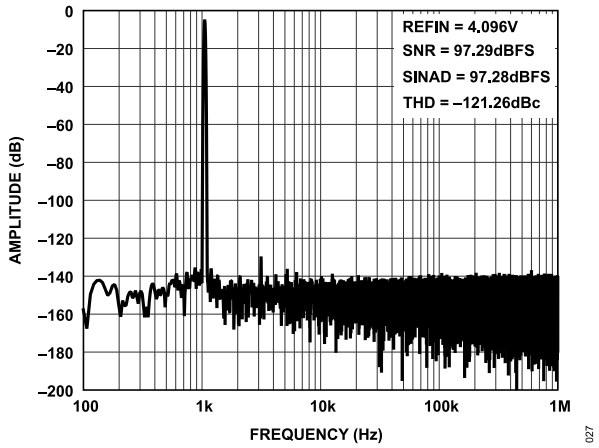


Figure 27. FFT, 2MSPS, f_{IN} = 1kHz, Differential Input = −0.5dBFS, G = 5/9, REFIN = 4.096V

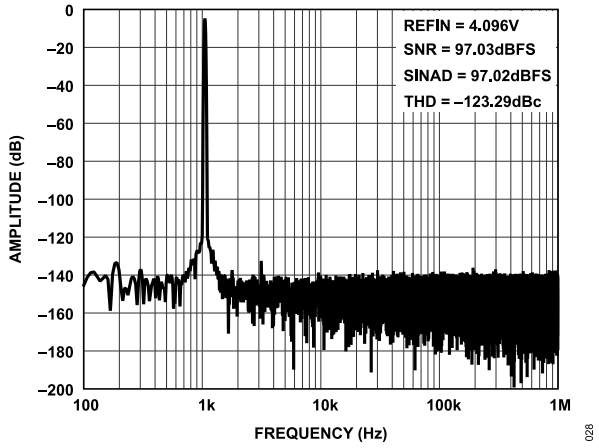


Figure 28. FFT, 2MSPS, f_{IN} = 1kHz, Differential Input = −0.5dBFS, G = 20/9, REFIN = 4.096V

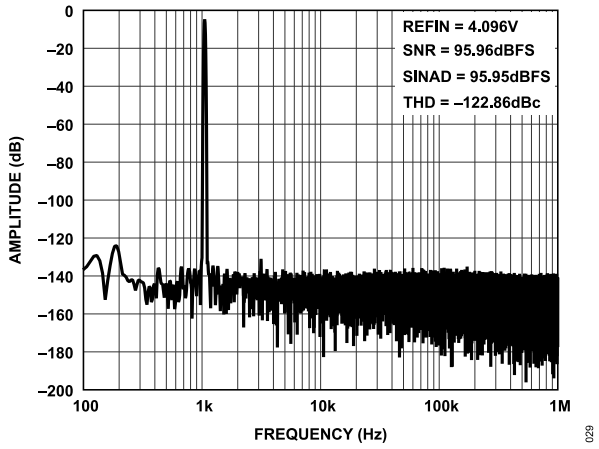


Figure 29. FFT, 2MSPS, f_{IN} = 1kHz, Differential Input = −0.5dBFS, G = 20/3, REFIN = 4.096V

TYPICAL PERFORMANCE CHARACTERISTICS

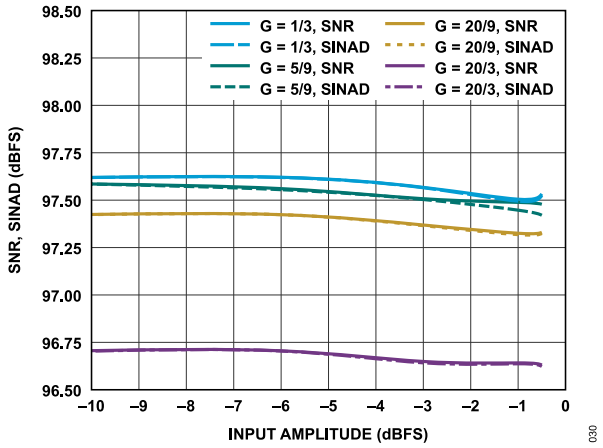


Figure 30. SNR, SINAD vs. Input Amplitude at f_{IN} = 1kHz

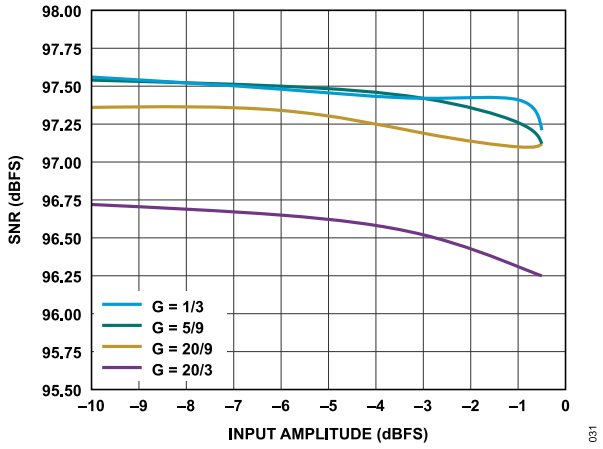


Figure 31. SNR vs. Input Amplitude at f_{IN} = 20kHz

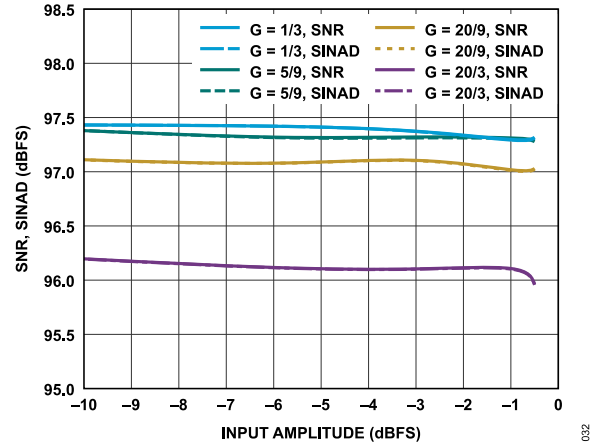


Figure 32. SNR, SINAD vs. Input Amplitude, f_{IN} = 1kHz, REFIN = 4.096V

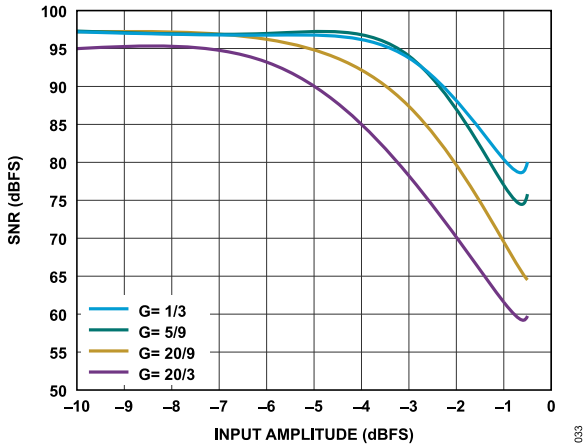


Figure 33. SNR vs. Input Amplitude at f_{IN} = 50kHz

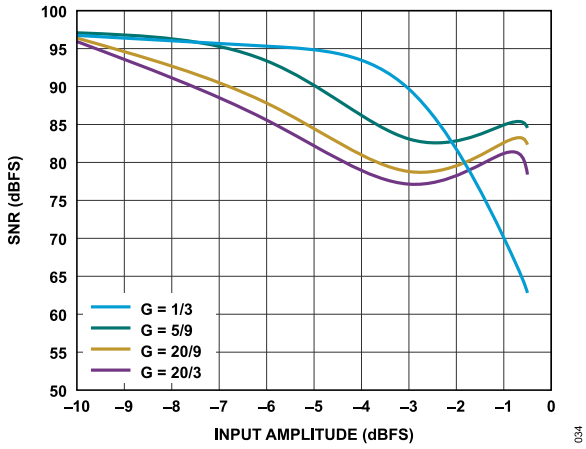


Figure 34. SNR vs. Input Amplitude at f_{IN} = 100kHz

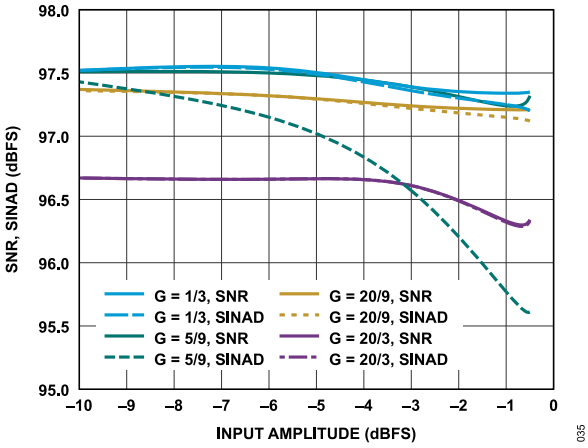


Figure 35. SNR, SINAD vs. Input Amplitude, f_{IN} = 1kHz, Single-Ended

TYPICAL PERFORMANCE CHARACTERISTICS

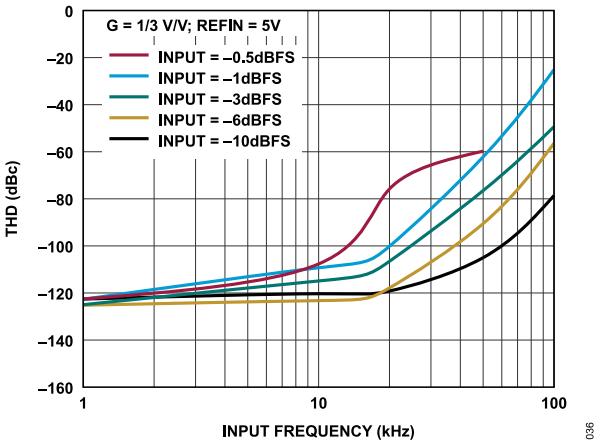


Figure 36. THD vs. Input Frequency, Various Amplitudes, G = 1/3

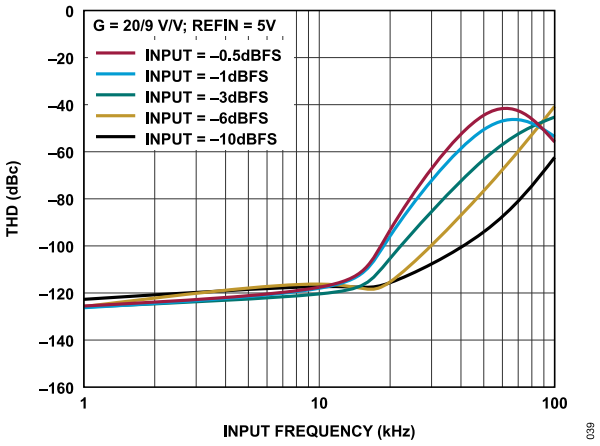


Figure 39. THD vs. Input Frequency, Various Amplitudes, G = 20/9

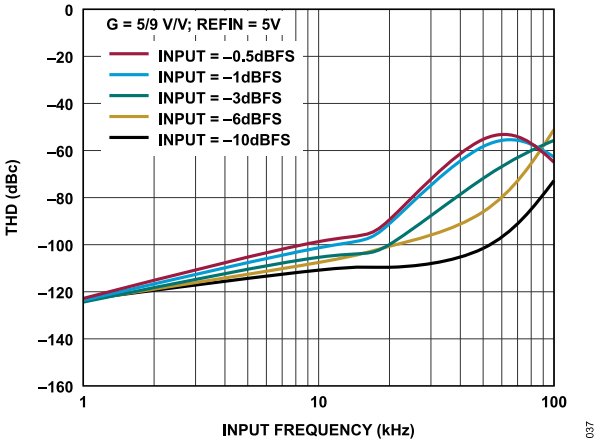


Figure 37. THD vs. Input Frequency, Various Amplitudes, G = 5/9

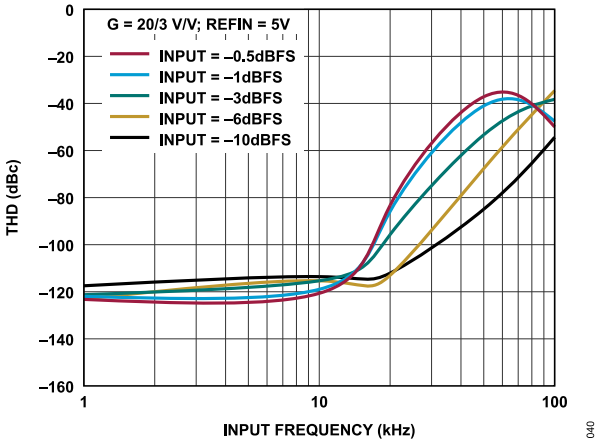


Figure 40. THD vs. Input Frequency, Various Amplitudes, G = 20/3

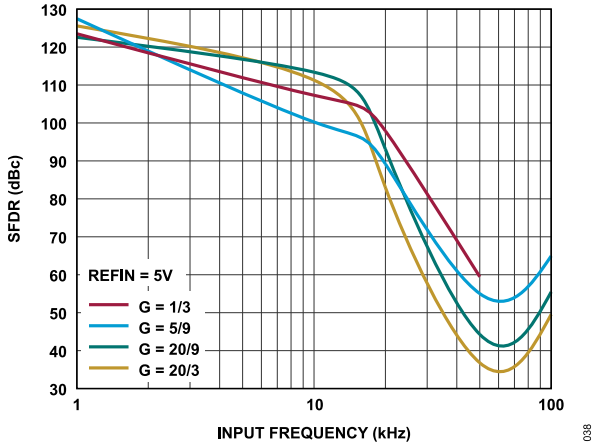


Figure 38. SFDR vs. Input Frequency, −0.5dBFS, REFIN = 5V

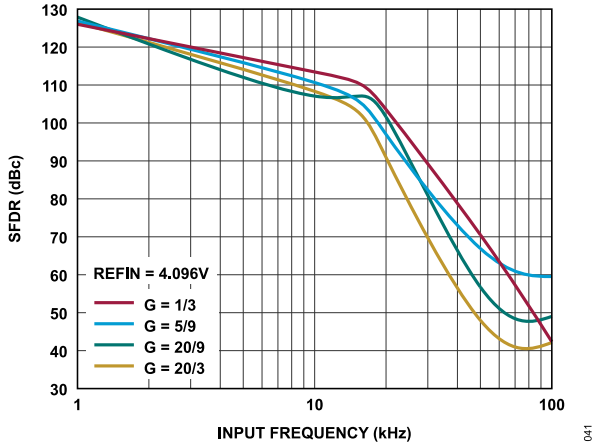


Figure 41. SFDR vs. Input Frequency, −0.5dBFS, REFIN = 4.096V

TYPICAL PERFORMANCE CHARACTERISTICS

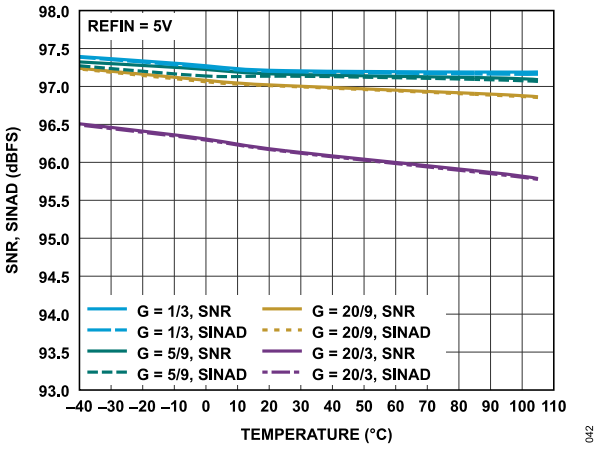


Figure 42. SNR, SINAD vs. Temperature, f_{IN} = 1kHz Differential Input, REFIN = 5V

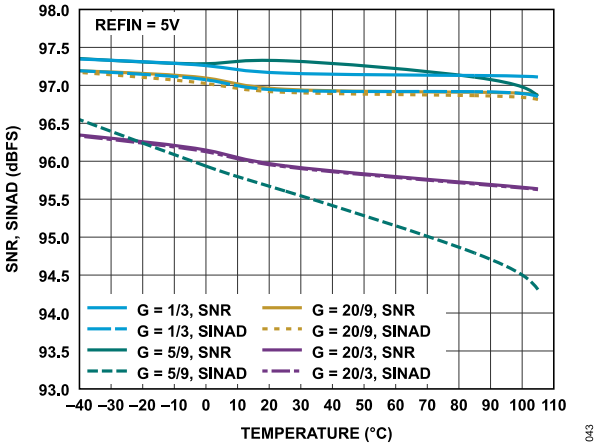


Figure 43. SNR, SINAD vs. Temperature, f_{IN} = 1kHz Single-Ended Input, REFIN = 5V

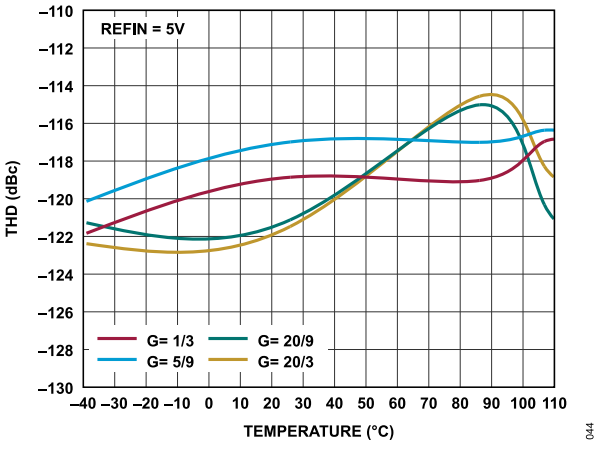


Figure 44. THD vs. Temperature, f_{IN} = 1kHz, Differential Input, REFIN = 5V

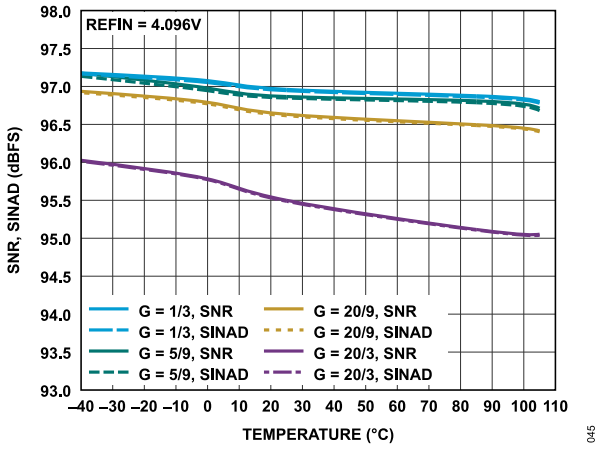


Figure 45. SNR, SINAD vs. Temperature, f_{IN} = 1kHz Differential Input, REFIN = 4.096V

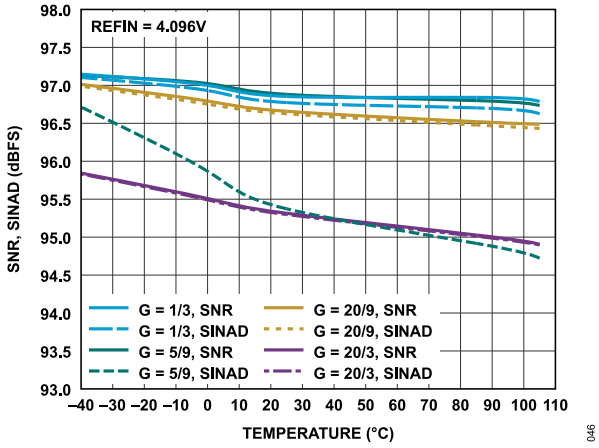


Figure 46. SNR, SINAD vs. Temperature, f_{IN} = 1kHz Single-Ended Input, REFIN = 4.096V

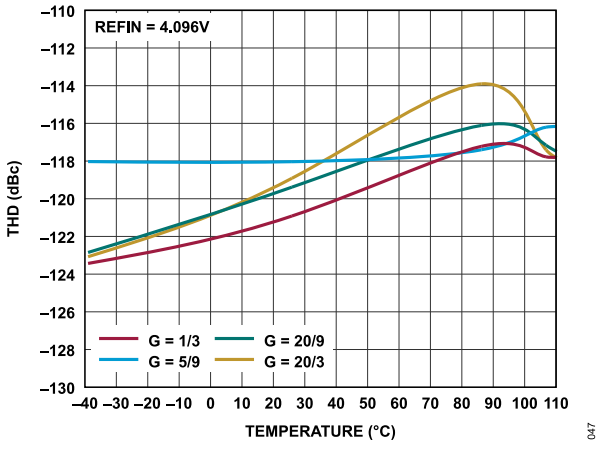


Figure 47. THD vs. Temperature, f_{IN} = 1kHz, Differential Input, REFIN = 4.096V

TYPICAL PERFORMANCE CHARACTERISTICS

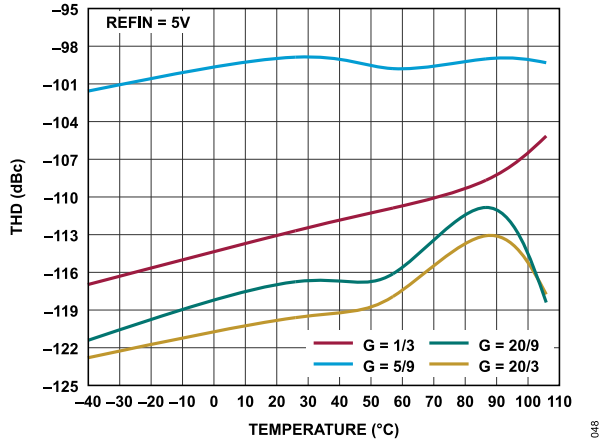


Figure 48. THD vs. Temperature, f_{IN} = 1kHz, Single-Ended Input, REFIN = 5V

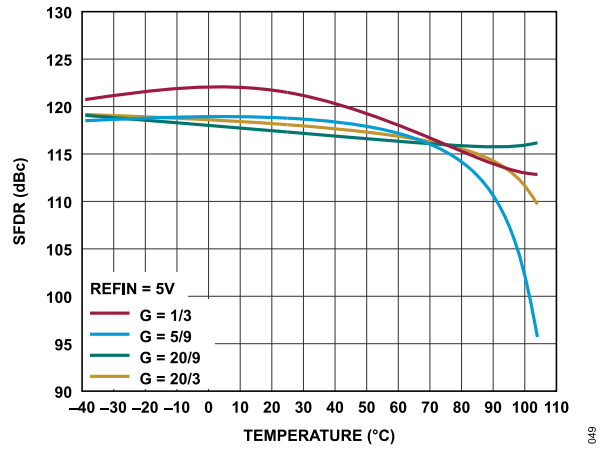


Figure 49. SFDR vs. Temperature, f_{IN} = 1kHz, REFIN = 5V

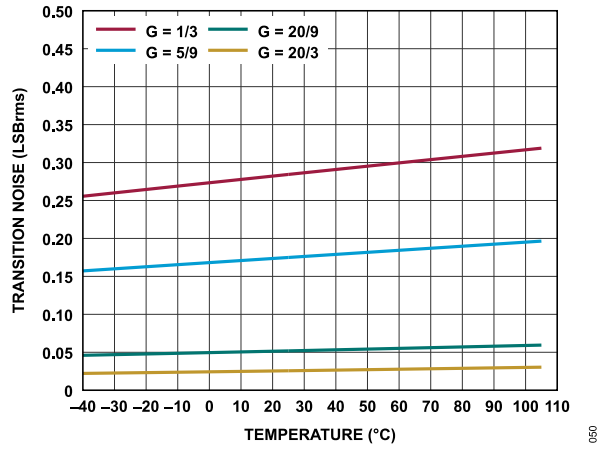


Figure 50. Transition Noise vs. Temperature, REFIN = 5V

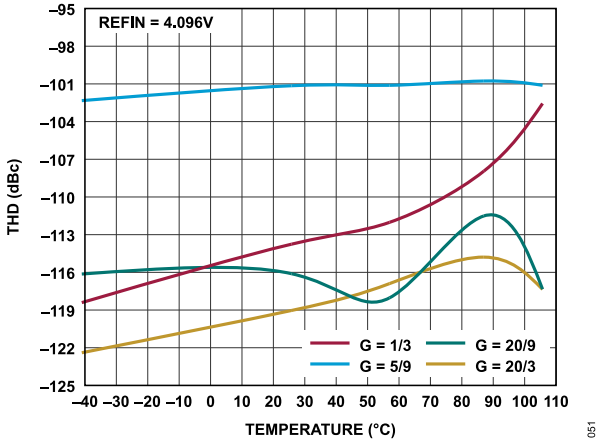


Figure 51. THD vs. Temperature, f_{IN} = 1kHz, Single-Ended Input, REFIN = 4.096V

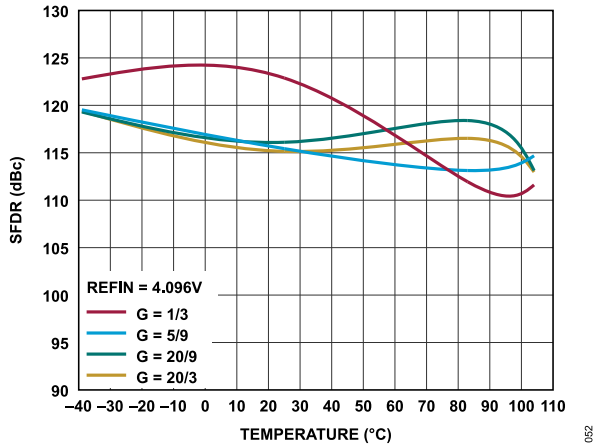


Figure 52. SFDR vs. Temperature, f_{IN} = 1kHz, REFIN = 4.096V

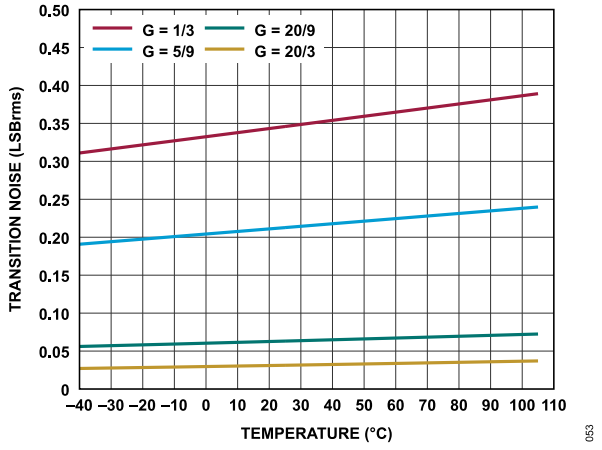


Figure 53. Transition Noise vs. Temperature, REFIN = 4.096V

TYPICAL PERFORMANCE CHARACTERISTICS

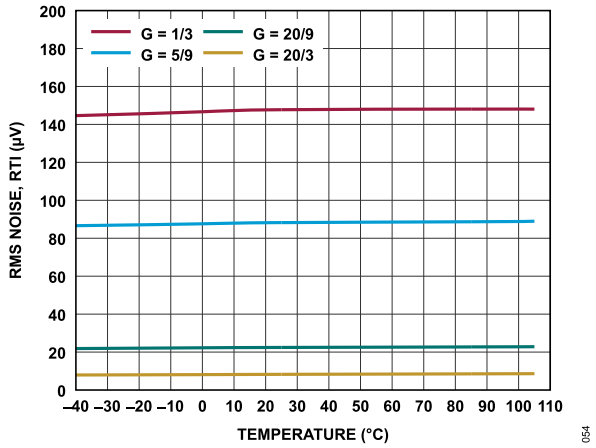


Figure 54. RMS Noise, RTI vs. Temperature, REFIN = 5V

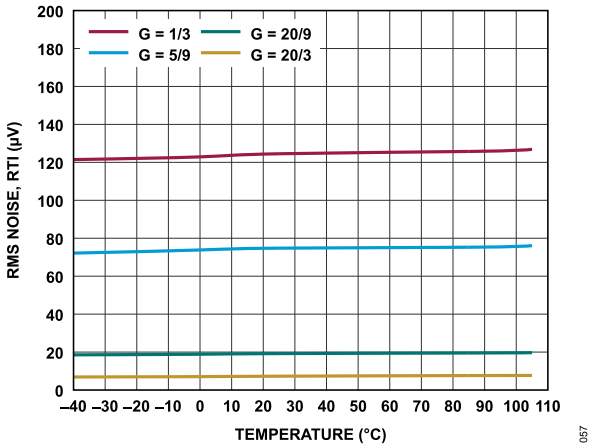


Figure 57. RMS Noise, RTI vs. Temperature, REFIN = 4.096V

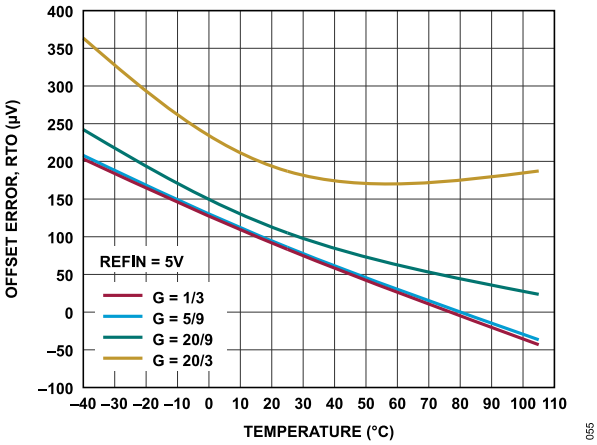


Figure 55. Offset Error vs. Temperature

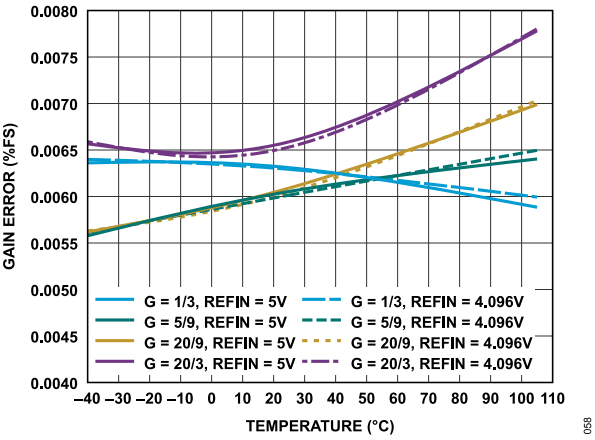


Figure 58. Gain Error vs. Temperature

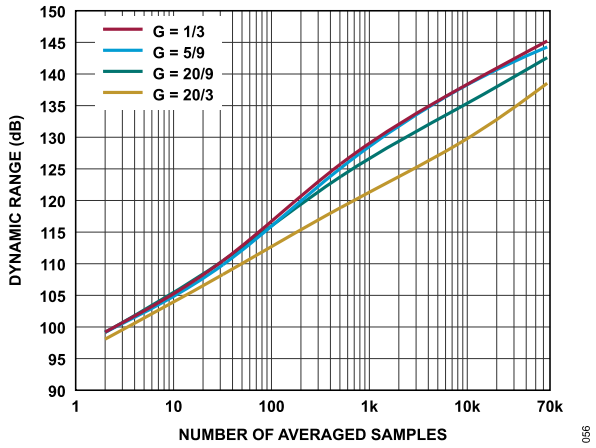


Figure 56. Dynamic Range vs. Number of Averages, Input = −60dBFS, REFIN = 5V

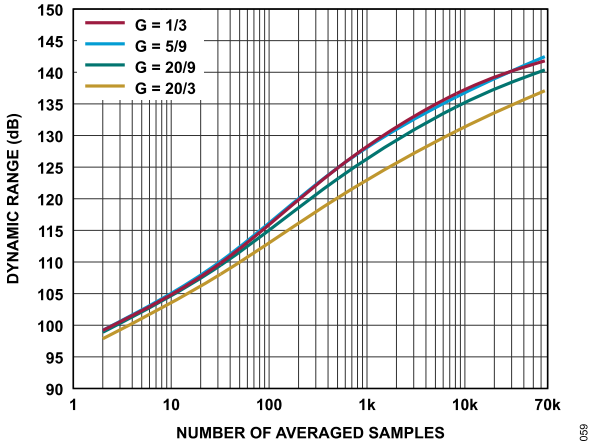


Figure 59. Dynamic Range vs. Number of Averages, Input = −60dBFS, REFIN = 4.096V

TYPICAL PERFORMANCE CHARACTERISTICS

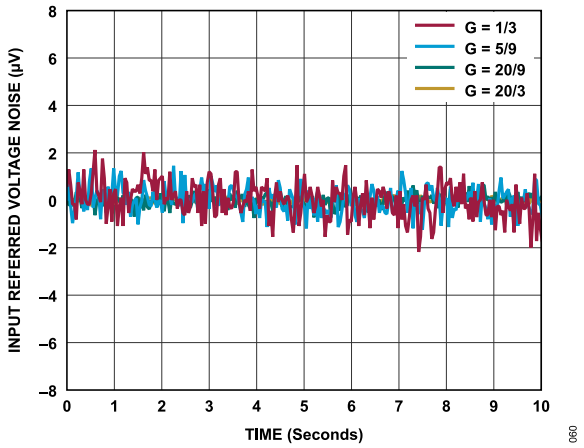


Figure 60. Low Frequency Noise (Output Data Rate = 256SPS After Averaging Blocks of 4096 Samples), REFIN = 5V

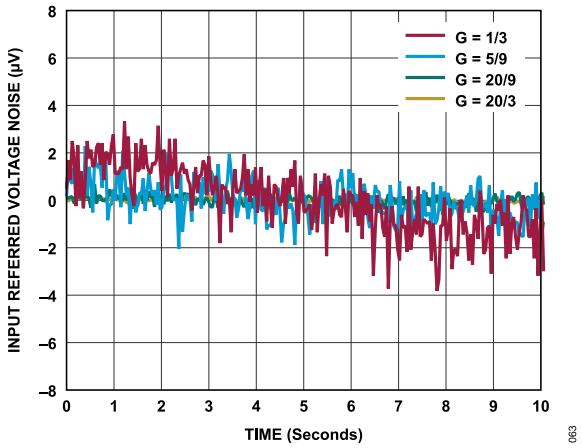


Figure 63. Low Frequency Noise (Output Data Rate = 256SPS After Averaging Blocks of 4096 Samples), REFIN = 4.096V

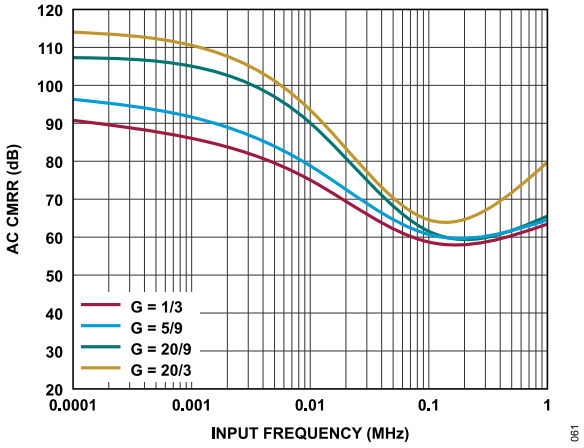


Figure 61. AC CMRR vs. Input Frequency, REFIN = 5V

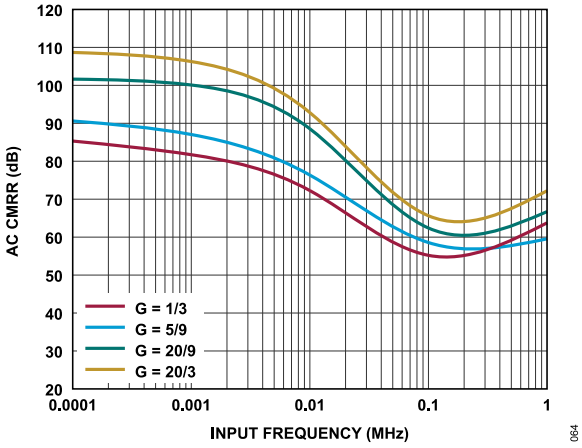


Figure 64. AC CMRR vs. Input Frequency, REFIN = 4.096V

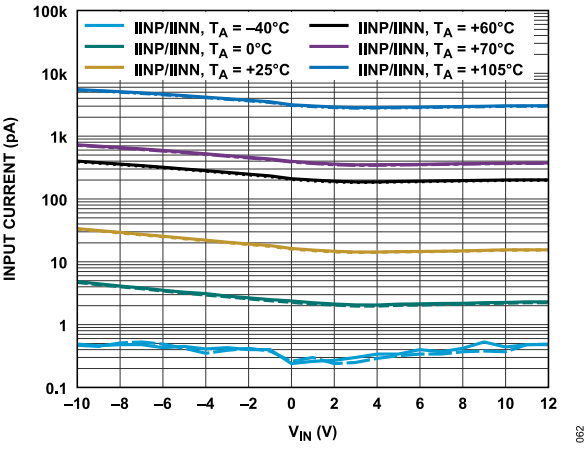


Figure 62. Input Current vs. Input Voltage across Temperature

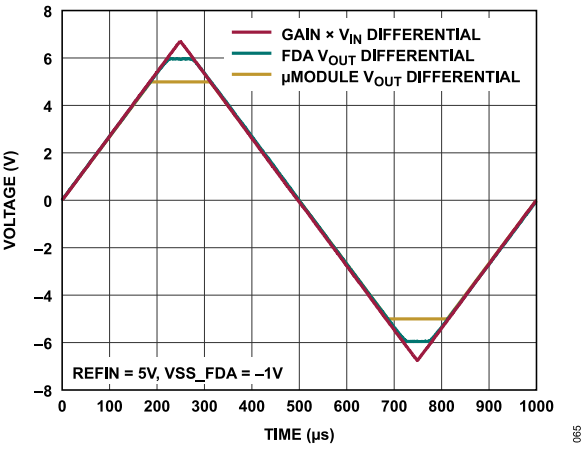


Figure 65. Output Overdrive Recovery, IN = 1kHz

TYPICAL PERFORMANCE CHARACTERISTICS

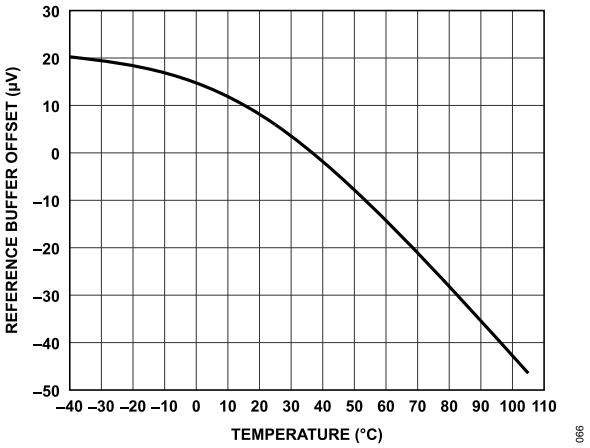


Figure 66. Reference Buffer Offset vs. Temperature

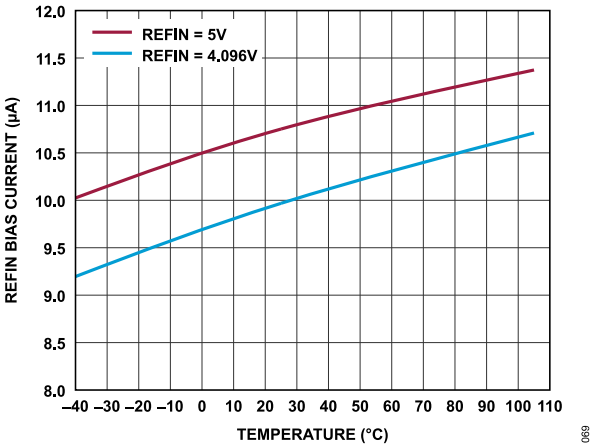


Figure 69. REFIN Current Normal Operation vs. Temperature

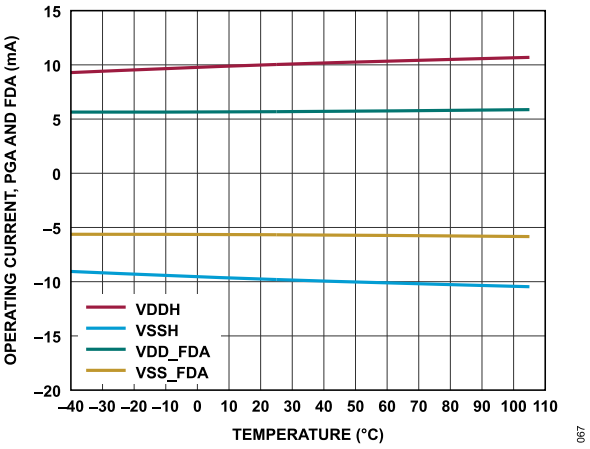


Figure 67. Operating Current PGA and FDA vs. Temperature

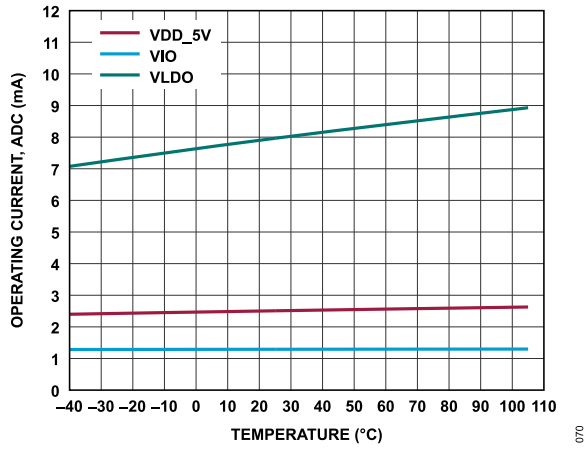


Figure 70. Operating Current ADC vs. Temperature

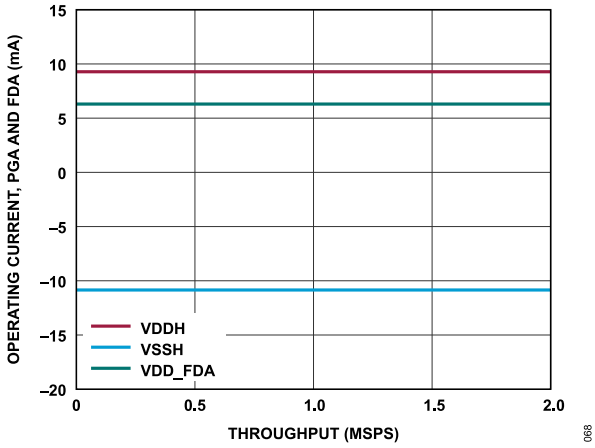


Figure 68. Operating Current PGA and FDA vs. Sample Rate

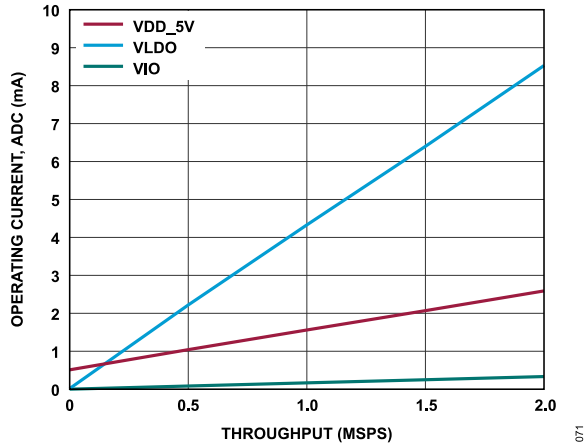


Figure 71. Operating Current ADC vs. Sample Rate

TYPICAL PERFORMANCE CHARACTERISTICS

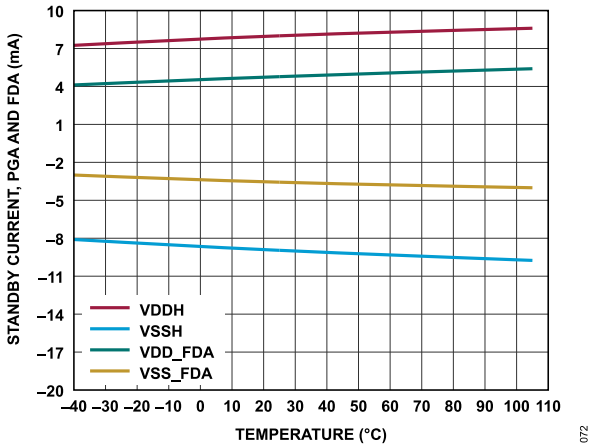


Figure 72. Standby Current PGA and FDA vs. Temperature

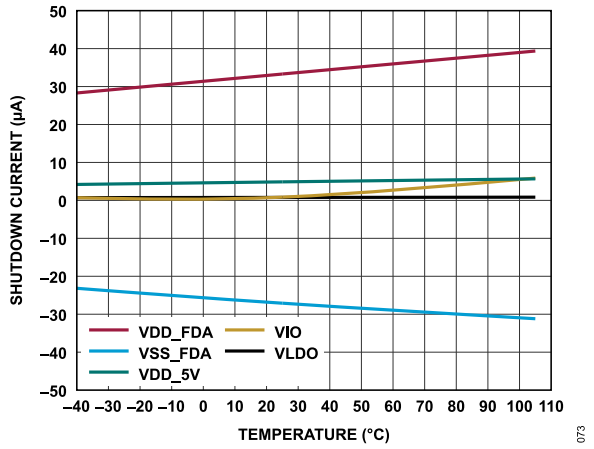


Figure 73. Shutdown Current vs. Temperature

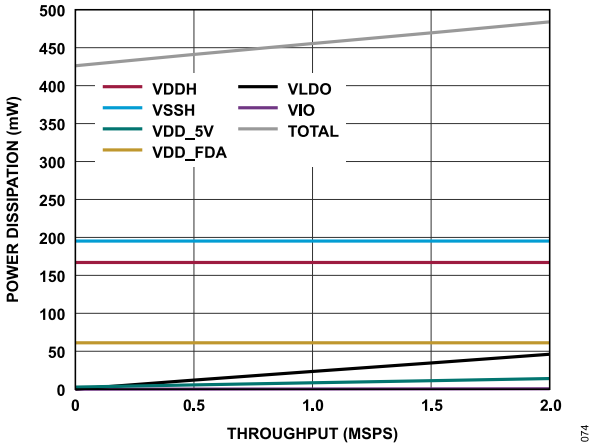


Figure 74. Power Dissipation vs. Throughput

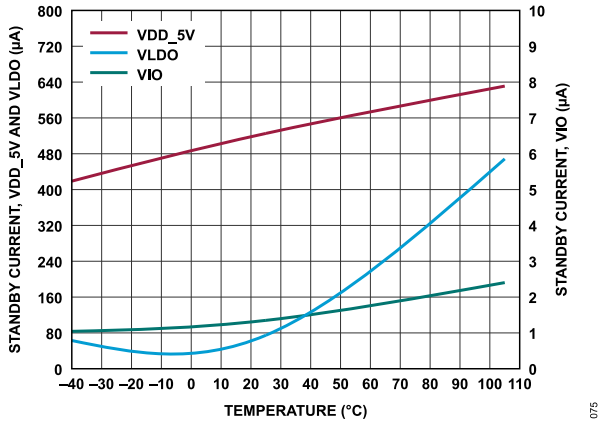


Figure 75. Standby Current ADC vs. Temperature

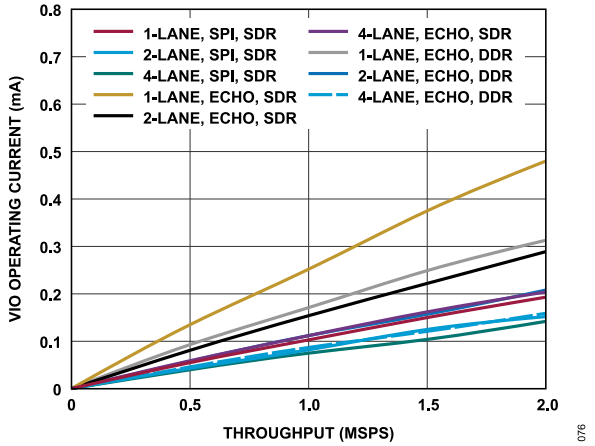


Figure 76. VIO Operating Current vs. Sample Rate

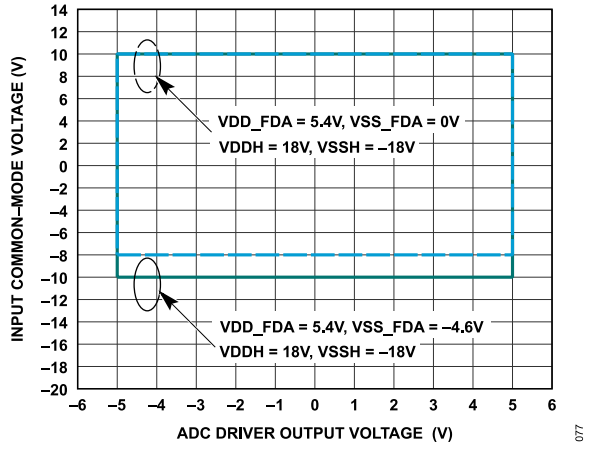


Figure 77. Input Common-Mode Voltage vs. ADC Driver Output Voltage, All Gains

TYPICAL PERFORMANCE CHARACTERISTICS

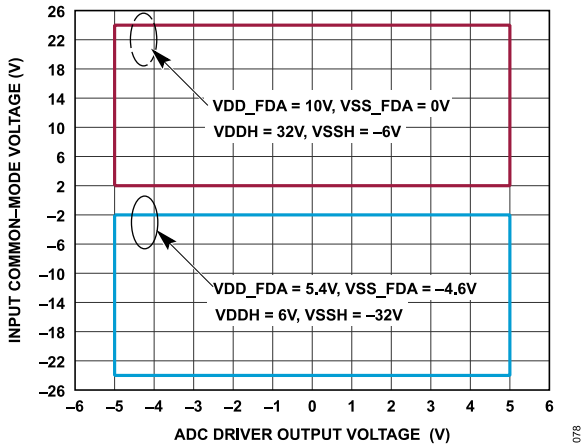


Figure 78. Input Common-Mode Voltage vs. ADC Driver Output Voltage, All Gains

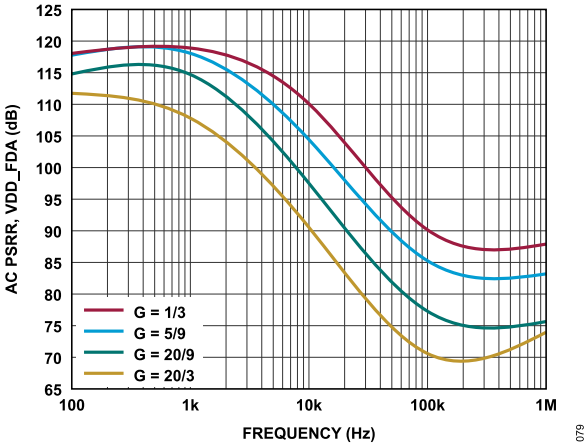


Figure 79. AC PSRR vs. Frequency, VDD_FDA

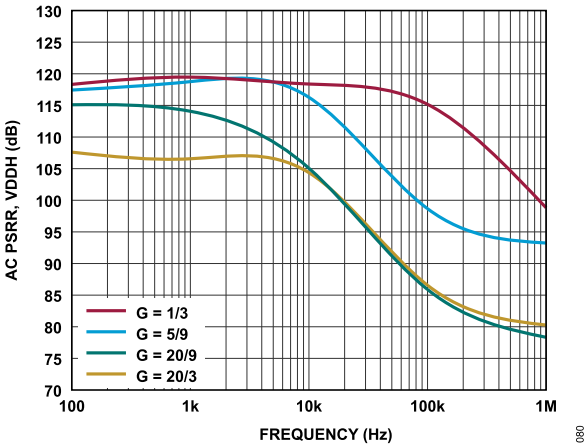


Figure 80. AC PSRR vs. Frequency, V_{DDH}

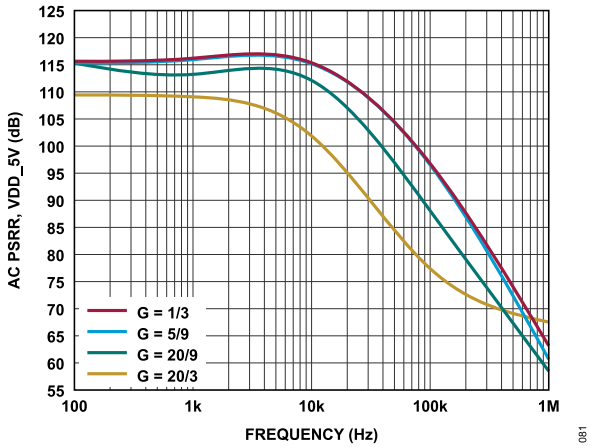


Figure 81. AC PSRR vs. Frequency, VDD_5V

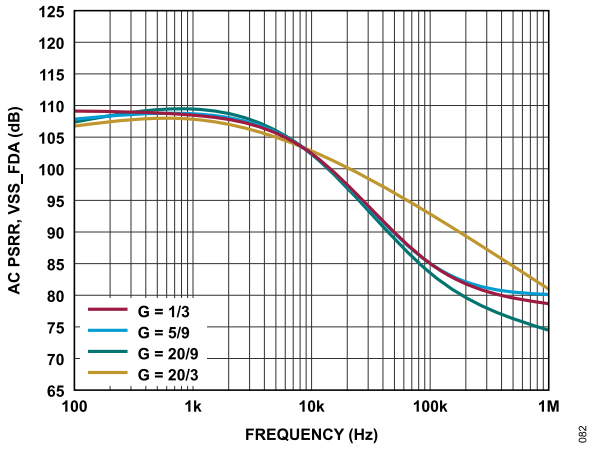


Figure 82. AC PSRR vs. Frequency, VSS_FDA

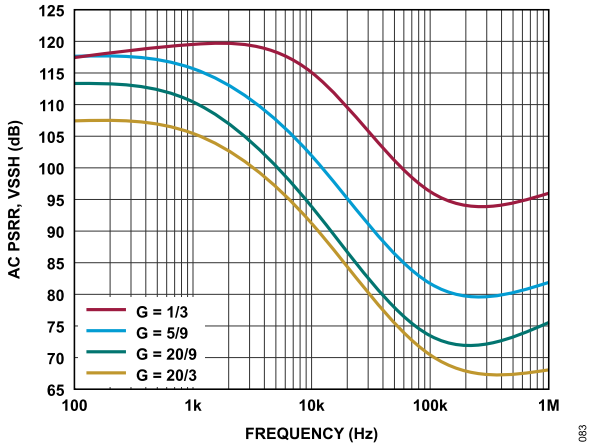


Figure 83. AC PSRR vs. Frequency, V_{SSH}

TERMINOLOGY

INTEGRAL NONLINEARITY ERROR (INL)

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½LSB before the first code transition. Positive full scale is defined as a level 1½LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 85).

DIFFERENTIAL NONLINEARITY ERROR (DNL)

In an ideal ADC, code transitions are 1LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

OFFSET ERROR

Offset error is the difference between the ideal midscale voltage, 0V, and the actual voltage producing the midscale output code, 0LSB.

GAIN ERROR

The first transition (from 100 ... 00 to 100 ... 01) occurs at a level ½LSB above nominal negative full scale. The last transition (from 011 … 10 to 011 … 11) occurs for an analog voltage 1½LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

SPURIOUS-FREE DYNAMIC RANGE (SFDR)

SFDR is the difference, in decibel relative to the carrier (dBc), between the rms amplitude of the input signal and the peak spurious signal.

EFFECTIVE NUMBER OF BITS (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD as follows: ENOB = (SINADdB − 1.76)/6.02. ENOB is expressed in bits.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of the input signal and is expressed in decibel relative to the carrier (dBc).

DYNAMIC RANGE

Dynamic range is the rms voltage of a full-scale sine wave to the total rms voltage of the noise measured. The value for dynamic range is expressed in decibels. It is measured with a signal at −60dBFS so that it includes all noise sources and DNL artifacts.

Total System Dynamic Range

The ratio of the root-mean-square (RMS) value of the full scale input at Gain = 1/3V/V to the input referred RMS noise measured when input pins are shorted together at Gain = 20/3V/V. The value is expressed in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms voltage of a full-scale sine wave to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and DC. The value for SNR is expressed in decibel relative to full scale (dBFS).

SIGNAL-TO-NOISE-AND-DISTORTION (SINAD) RATIO

SINAD is the ratio of the rms voltage of a full-scale sine wave to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding DC. The value of SINAD is expressed in decibel relative to full scale (dBFS).

APERTURE DELAY

Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

TRANSIENT RESPONSE

Transient response is the time required for the ADC to acquire a full-scale input step to ±1LSB accuracy.

COMMON-MODE REJECTION RATIO (CMRR)

CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 4.5Vp-p sine wave applied to the input common-mode voltage of frequency, f.

$CMRR$ (dB) = 10× log(P_{ADC_IN}/P_{ADC_OUT})

where:
P_{ADC_IN} is the common-mode power at the frequency, f, applied to the inputs.
P_{ADC_OUT} is the power at the frequency, f, in the ADC output.

POWER-SUPPLY REJECTION RATIO (PSRR)

PSRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 200mVp-p sine wave applied to the ADC VDD supply of frequency, f.

$PSRR$ (dB) = 10 × log(P_{VDD_IN}/P_{ADC_OUT})

where:
P_{VDD_IN} is the power at the frequency, f, at the VDD pin.
P_{ADC_OUT} is the power at the frequency, f, in the ADC output.

THEORY OF OPERATION

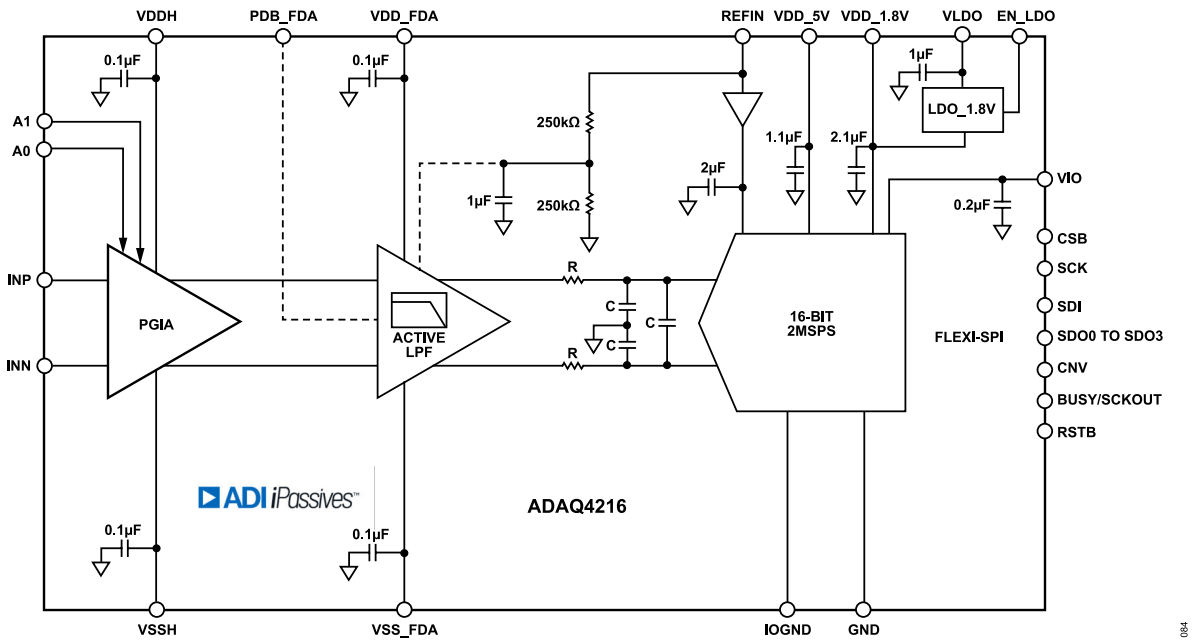


Figure 84. ADAQ4216 Functional Block Diagram

OVERVIEW

The ADAQ4216 is a precision µModule data-acquisition signal chain SiP solution that reduces the development cycle of precision measurement systems by transferring the design burden of component selection, optimization, and layout from the designer to the device. The ADAQ4216 reduces the end system component count by combining multiple common signal processing and conditioning blocks in a single device, including a low noise, high input impedance PGIA, a second order linear phase anti-aliasing filter, low distortion, wide-bandwidth ADC driver, a high precision 16-bit, 2MSPS SAR ADC with an integrated reference buffer. The device also incorporates the Analog Devices proprietary iPassives technology components necessary for optimum performance. The superior matching and drift characteristics of the resistors minimizes temperature dependent error sources. The analog front end of the ADAQ4216 features a wide common-mode range from −8V to +10V and supports both single-ended and differential signals that eases level shifting requirements as well.

The ADAQ4216 does not exhibit any pipeline delay or latency, which makes this µModule ideal for control loops and high speed applications. The digital features include offset correction, gain adjustment, and averaging, which offload the host processor. The user can configure the device for one of several output code formats (for more details, see the Summary of Selectable Output Data Formats section).

The ADAQ4216 uses a Flexi-SPI, which allows the data to be accessed by multiple SPI lanes, which relaxes clocking requirements for the host SPI controller. An echo clock mode is also available to assist in data clocking, which simplifies the use of isolated data interfaces. The PGIA gain of the ADAQ4216 can be controlled through A0 and A1 pins. The ADAQ4216 has a valid conversion after exiting shutdown mode. The architecture achieves ±3ppm INL maximum, with no missing codes at 16-bits and 97.5dB SNR. The ADAQ4216 dissipates only 445mW at 2MSPS.

TRANSFER FUNCTION

In the default configuration, the ADAQ4216 digitizes the full-scale difference voltage of 2 × V_{REF} into 2^{16} levels, resulting in an LSB size of 153µV with V_{REF} = 5V. Note that 1LSB at 16 bits is approximately 15.26ppm. The ideal transfer function is shown in Figure 85. The differential output data is in twos complement format. Table 12 summarizes the mapping of input voltages to differential output codes.

THEORY OF OPERATION

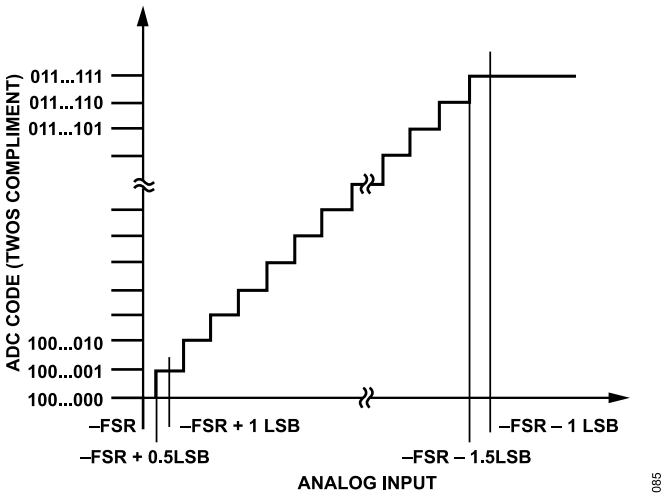


Figure 85. ADC Ideal Transfer Function for the Differential Output Codes (FSR Is Full-Scale Range)

Table 12. Input Voltage to Output Code Mapping

Description	Analog Input Voltage Difference	Digital Output Code (Twos Complement, Hex)
FSR − 1LSB	(32767 × V_{REF})/(G × 32768)	0x7FFF
Midscale + 1LSB	V_{REF}/(G × 32768)	0x0001
Midscale	0V	0x0000
Midscale − 1LSB	−V_{REF}/(G × 32768)	0xFFFF
−FSR + 1LSB	−(32767 × V_{REF})/(G × 32768)	0x8001
−FSR	− V_{REF}/G	0x8000

SIGNAL CHAIN OPERATION

The ADAQ4216 operates in two phases, the acquisition and the conversion phase. In the acquisition phase, the voltage present on each input pin (INP and INN) of PGIA is sampled independently. Issuing a rising edge pulse on the CNV pin initiates a conversion. The rising edge pulse on the CNV pin also asserts the BUSY signal to indicate a conversion in progress. At the end of the conversion, the BUSY signal is deasserted. The conversion result is a 16-bit code representing the input voltage difference and an 8-bit code representing the input common-mode voltage. Depending on the device configuration, this conversion result can be processed digitally and latched into the internal output register. The internal ADC acquisition circuit on each input pin is also precharged to the previous sample voltage, which minimizes the kick-back charge to the input driver stage (PGIA). The host processor retrieves the output code by the SDO pins that are internally connected to the internal output register.

DIGITAL SAMPLE PROCESSING FEATURES

The ADAQ4216 supports several digital and data processing features that can be applied to the signal samples. These features are enabled and disabled by the control registers of the ADAQ4216.

Full-Scale Saturation

The conversion results saturate digitally (before any post-processing) when either or both inputs exceed the analog limits specified herein. After applying offset and gain scaling, the results are reduced to 16-bit representation (saturating at maximum 0x7FFF and minimum 0x8000). A user must be avoid unintentional saturation, especially when applying digital offset and/or gain scaling. For more details on the use of these features, see the Digital Offset Adjust and Digital Gain sections.

Common-Mode Output

When the host controller writes 0x1 to the OUT_DATA_MD bit field of the modes register (for more details, see the Modes Register section), an 8-bit code representing the input common-mode voltage is appended to the 16-bit code representing the input voltage difference. The LSB size of the 8-bit code is V_{REF}/256. The 8-bit code saturates at 0 and 255 when the common mode input voltage is 0V and V_{REF}, respectively. The 8-bit code is not affected by digital offset and gain scaling, which is applied only to the code representing the input voltage difference.

Block Averaging

The ADAQ4216 provides a block averaging filter (SINC1) with programmable block length 2^N, N = 1, 2, 3, …, 16. The filter is reset after processing each block of 2^N samples. The filter is enabled by writing 0x3 to the OUT_DATA_MD bit field of the modes register (for more details, see the Modes Register section) as well as a value (1 ≤ N ≤ 16) to the AVG_VAL bit field in the averaging mode register (for more details, see the Averaging Mode Register section). In this configuration, the output sample word is 32 bits. The 30 most significant bits (MSBs) represent the numerical value of the 16-bit codes averaged in blocks of 2^N samples. The automatic scaling allows the 16MSBs of the 30-bit code to be equal to the 16-bit codes when averaging blocks of constant values. The 31st bit (OR) is an overrange warning bit that is high when one or more samples in the block are subject to saturation. The 32nd bit (SYNC) is high once every 2^N conversion cycles to indicate when the average values are updated at the end of each block of samples. For more details, see the Digital Sample Processing Features section.

The effective data rate in averaging mode is $f_{CNV}/2^N$. The reset value of N in the AVG_VAL bit field is 0x00 (no averaging). Figure 109 shows an example timing diagram in averaging mode. Figure 86 shows the frequency response of the filter for an N = 1, 2, 3, 4, 5.

THEORY OF OPERATION

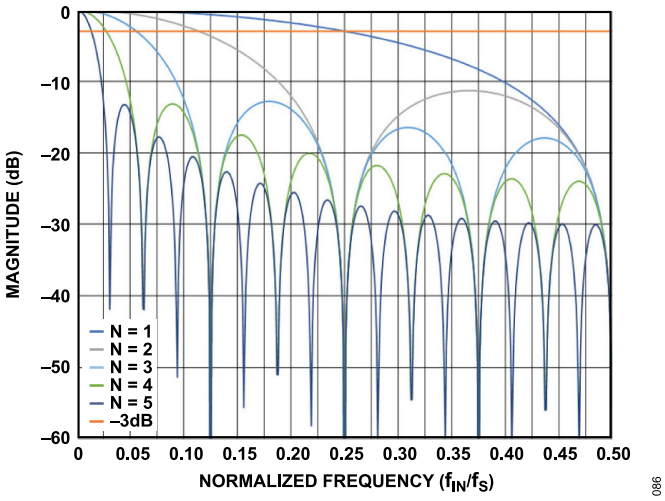


Figure 86. Frequency Response Examples for the Block Averaging Filter

Digital Offset Adjust

The ADC can be programmed to add a 16-bit signed offset value to the sample data (for more details, see the Register Details section). When adding an offset to the samples, it is possible to cause the sample data to saturate numerically. The user must take this into account when using the offset feature. The default value is 0x0000. For more details, see the Offset Registers section.

Digital Gain

The ADC can be programmed to apply a 16-bit unsigned digital gain (Register 0x1C and Register 0x1D) to the digital samples (for more details, see the Register Details section). The gain is applied to each sample based on the following equation:

$Code_{OUT} = Code_{IN} \times (USER\_GAIN/0x8000)$

where:

$0x0000 \leq USER\_GAIN \leq 0xFFFF$.

The effective gain range is 0 to 1.99997. Note that applying gain to the samples may cause numerical saturation. The default value is 0x8000 (gain = 1). To measure input voltage differences exceeding $\pm V_{REF}$, set the gain less than the unity to avoid the numerical saturation of the 16-bit or 30-bit output differential codes. For more details, see the Gain Registers section.

Test Pattern

To facilitate functional testing and debugging of the SPI, the host controller can write a 32-bit test pattern to the ADAQ4216 (for more details, see the Test Pattern Registers section). The value written to the test pattern registers is output using the normal sample cycle timing. The 32-bit test pattern output mode is enabled by writing 0x4 to the OUT_DATA_MD bit field of the modes register (for more details, see the Modes Register section). The default value stored in the test pattern registers is 0x5A5A0F0F.

Summary of Selectable Output Data Formats

Figure 87 summarizes the output data formats that are available on the ADAQ4216, which are selected in the modes register (for more details, see the Modes Register section). Note that the OR and SYNC flags are each 1-bit.

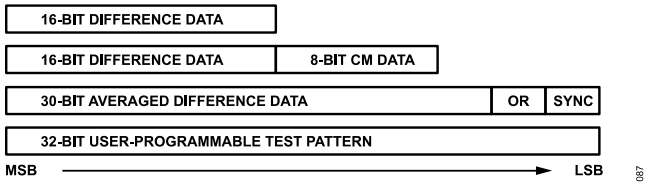


Figure 87. Summary of Selectable Output Sample Formats

APPLICATIONS INFORMATION

TYPICAL APPLICATION DIAGRAM

Figure 88 shows the typical system-level block diagram of a floating voltmeter including power tree and digital isolators. Echo clock and master clock mode relax the timing requirements and simplify the use of digital isolators. Figure 89 to Figure 96 shows the typical application examples of differential signals applied to each of the ADAQ4216 inputs for a given gain.

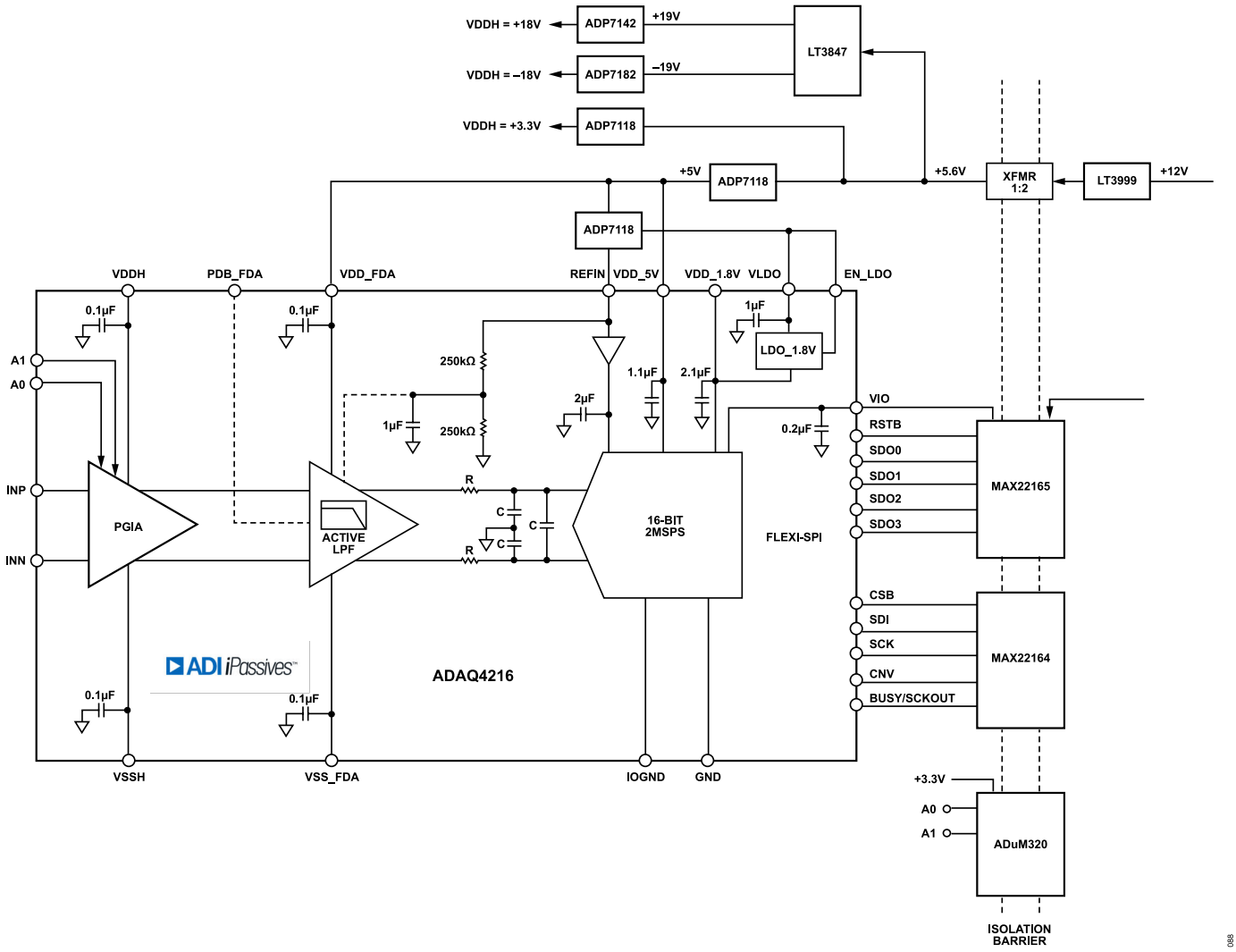


Figure 88. Functional Block Diagram of a Fully Isolated Data-Acquisition System

APPLICATIONS INFORMATION

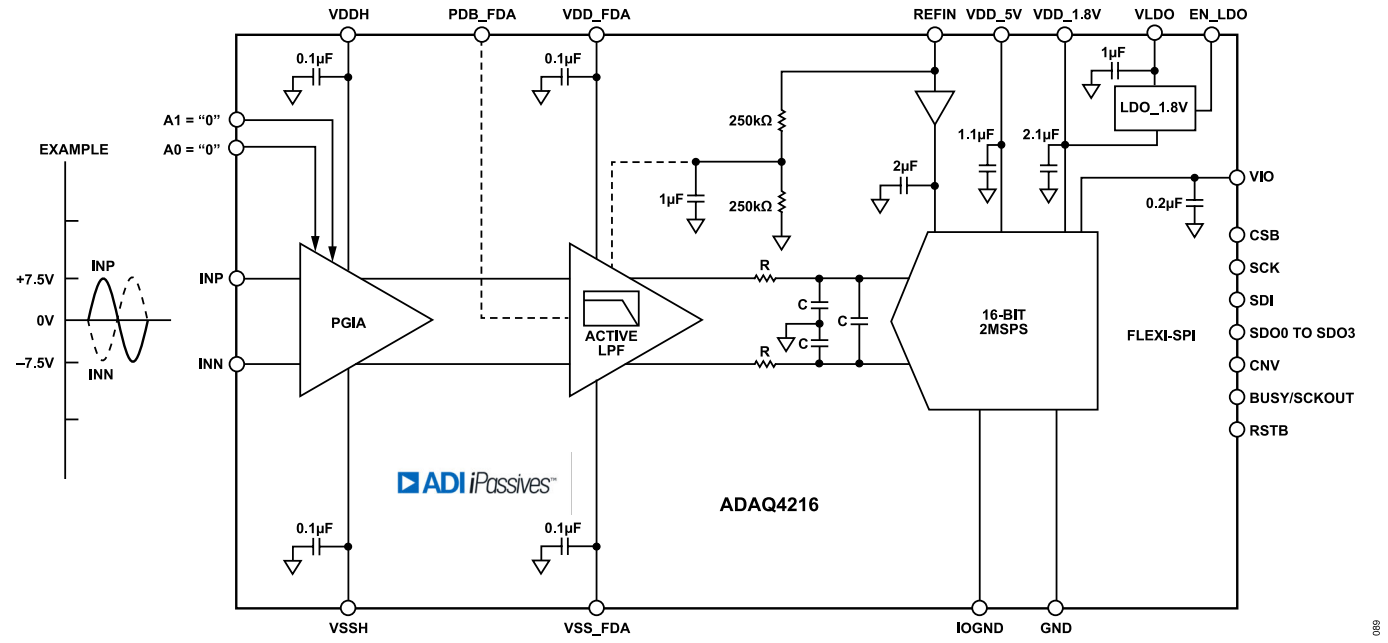


Figure 89. Differential Input Configuration with G = 1/3V/V

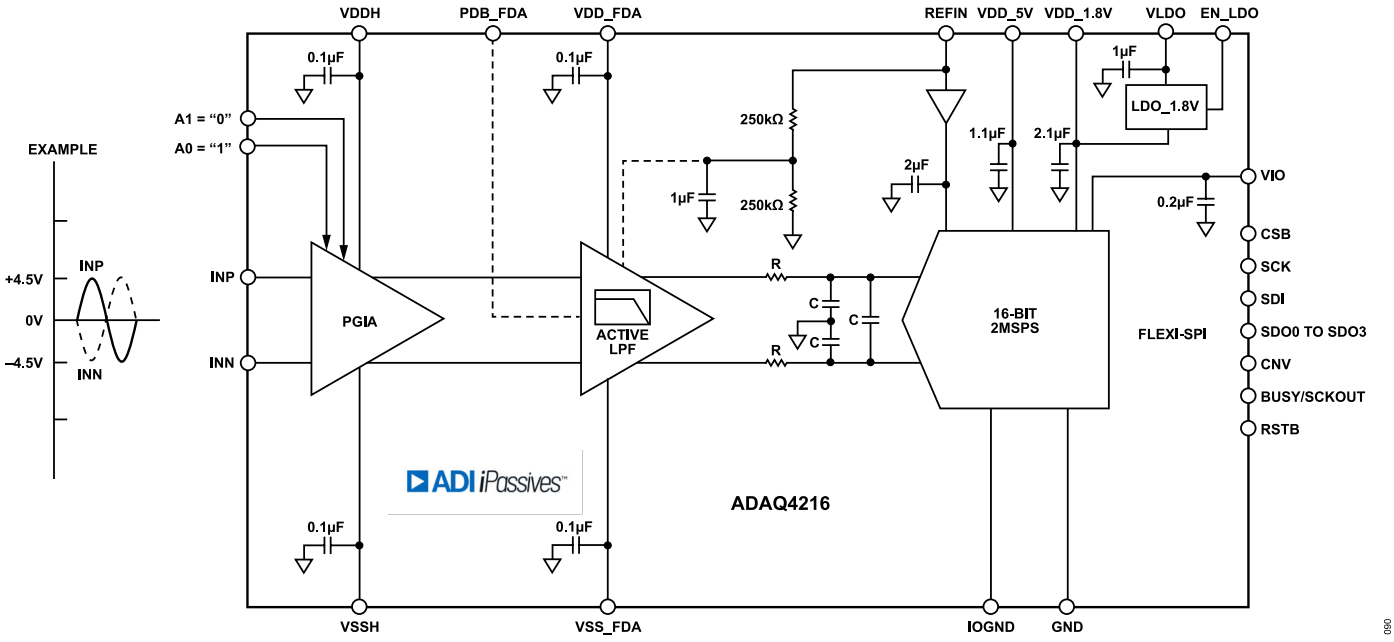


Figure 90. Differential Input Configuration with G = 5/9V/V

APPLICATIONS INFORMATION

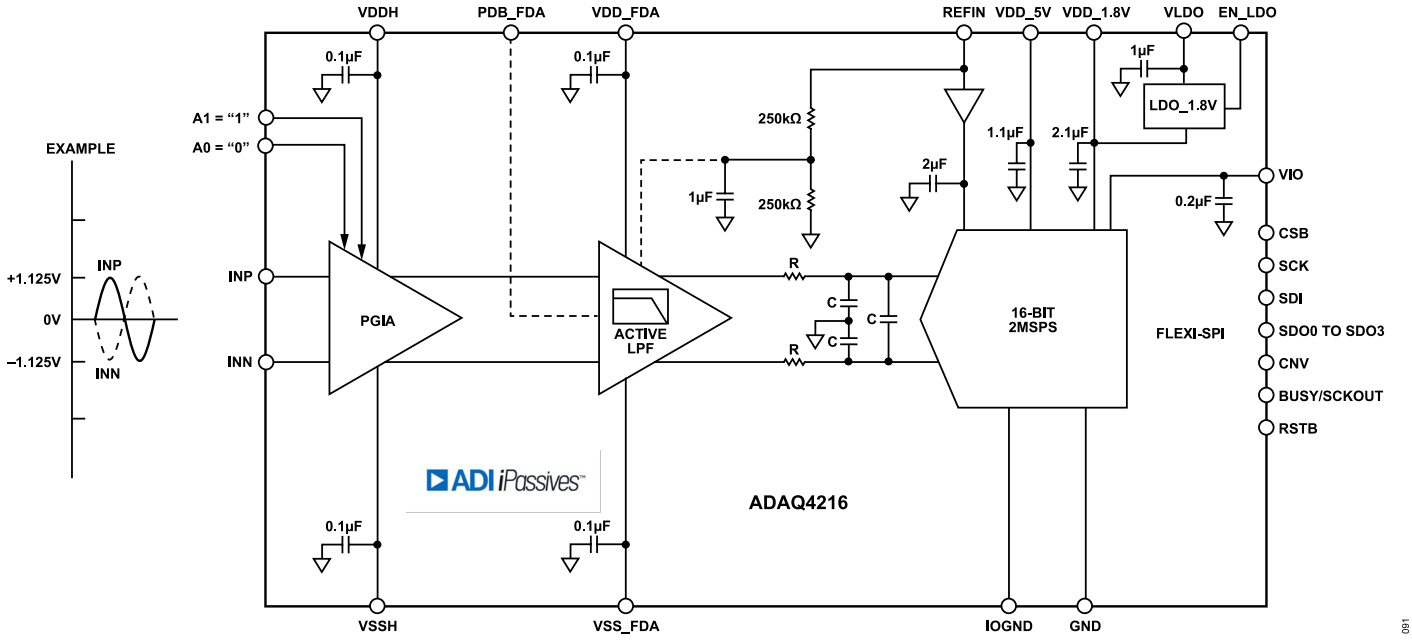


Figure 91. Differential Input Configuration with G = 20/9V/V

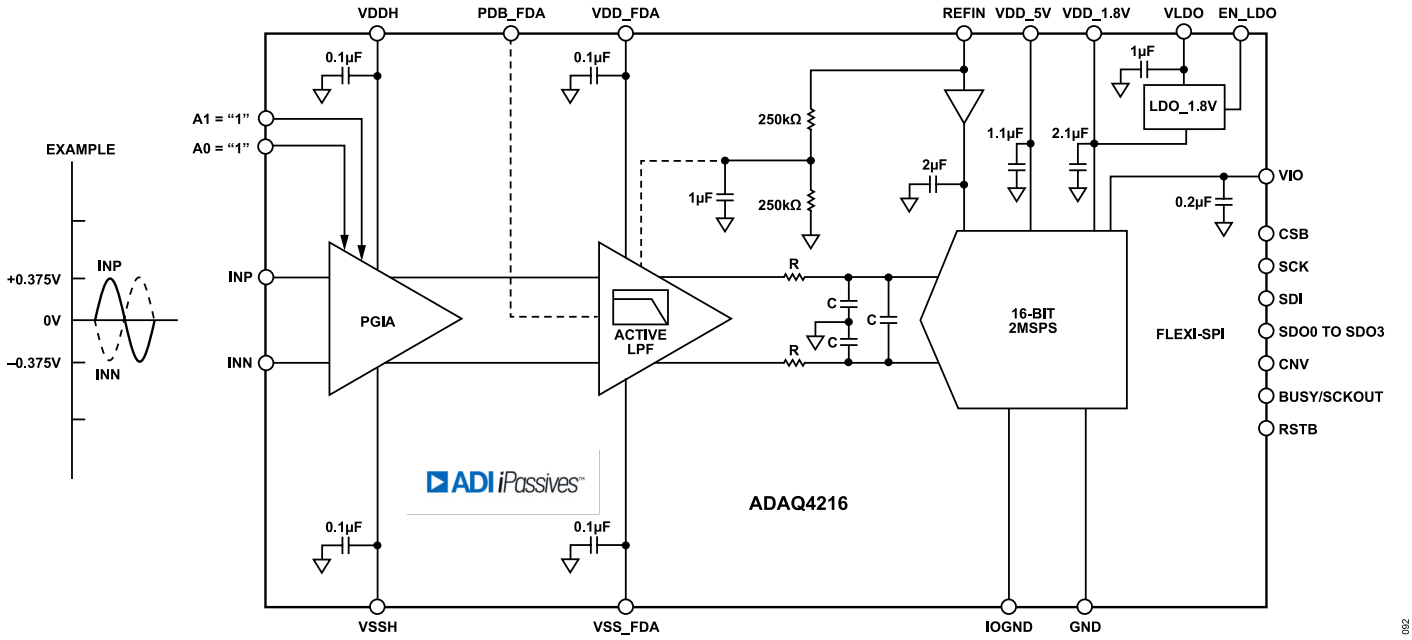


Figure 92. Differential Input Configuration with G = 20/3V/V

APPLICATIONS INFORMATION

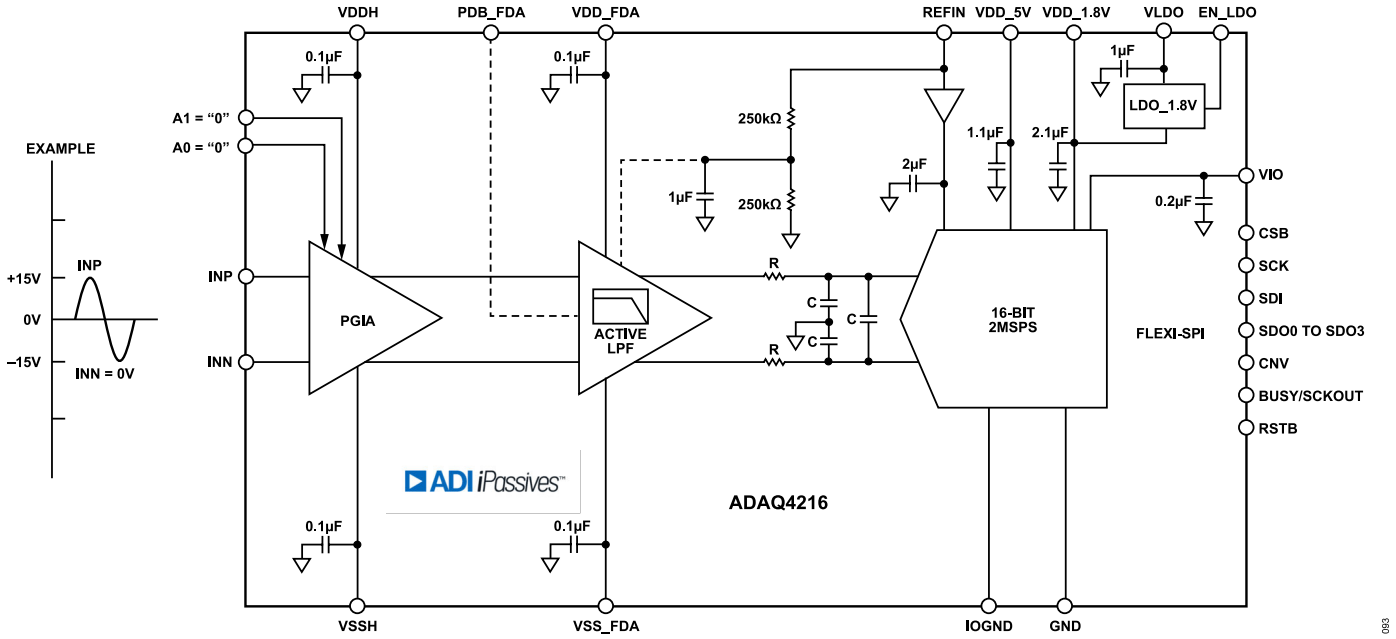


Figure 93. Single-Ended Input Configuration with G = 1/3V/V

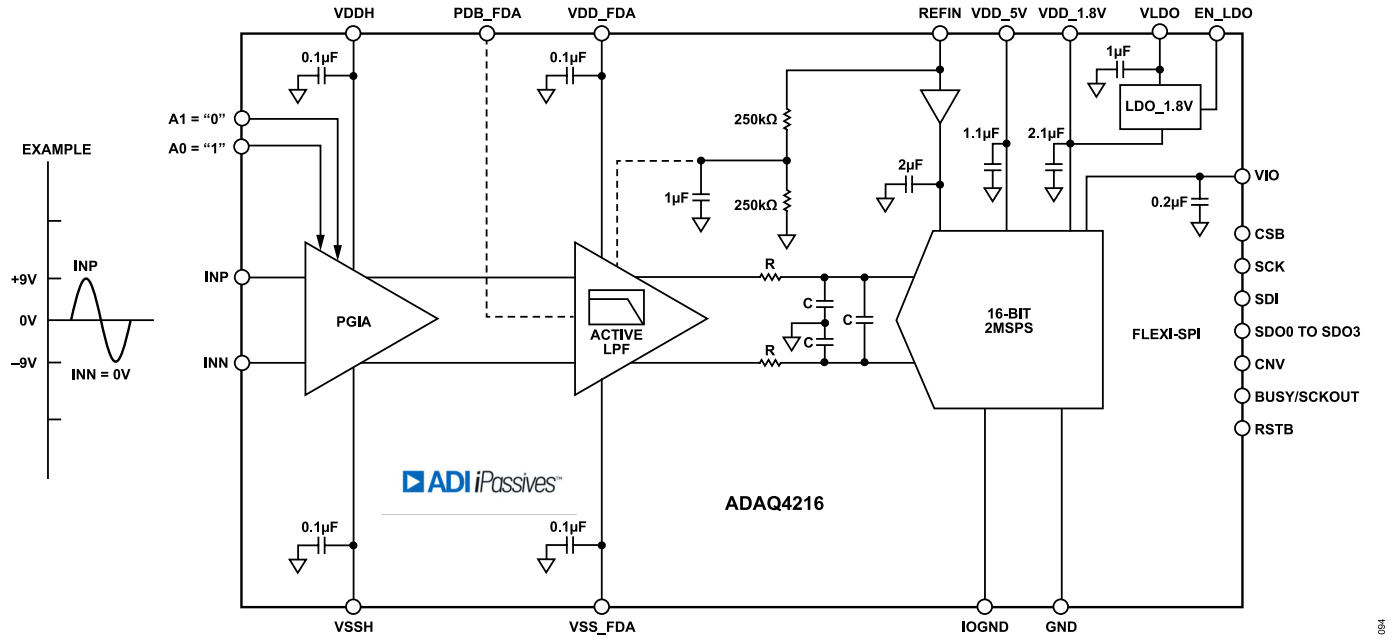


Figure 94. Single-Ended Input Configuration with G = 5/9V/V

APPLICATIONS INFORMATION

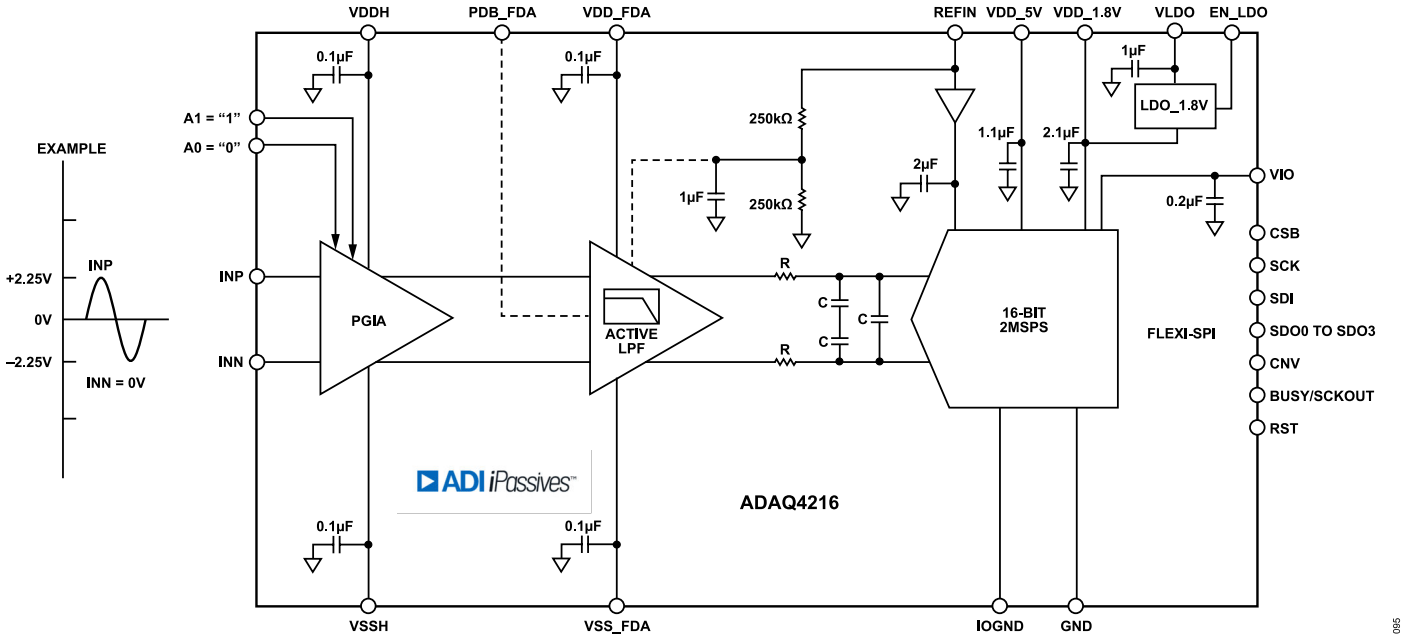


Figure 95. Single-Ended Input Configuration with G = 20/9V/V

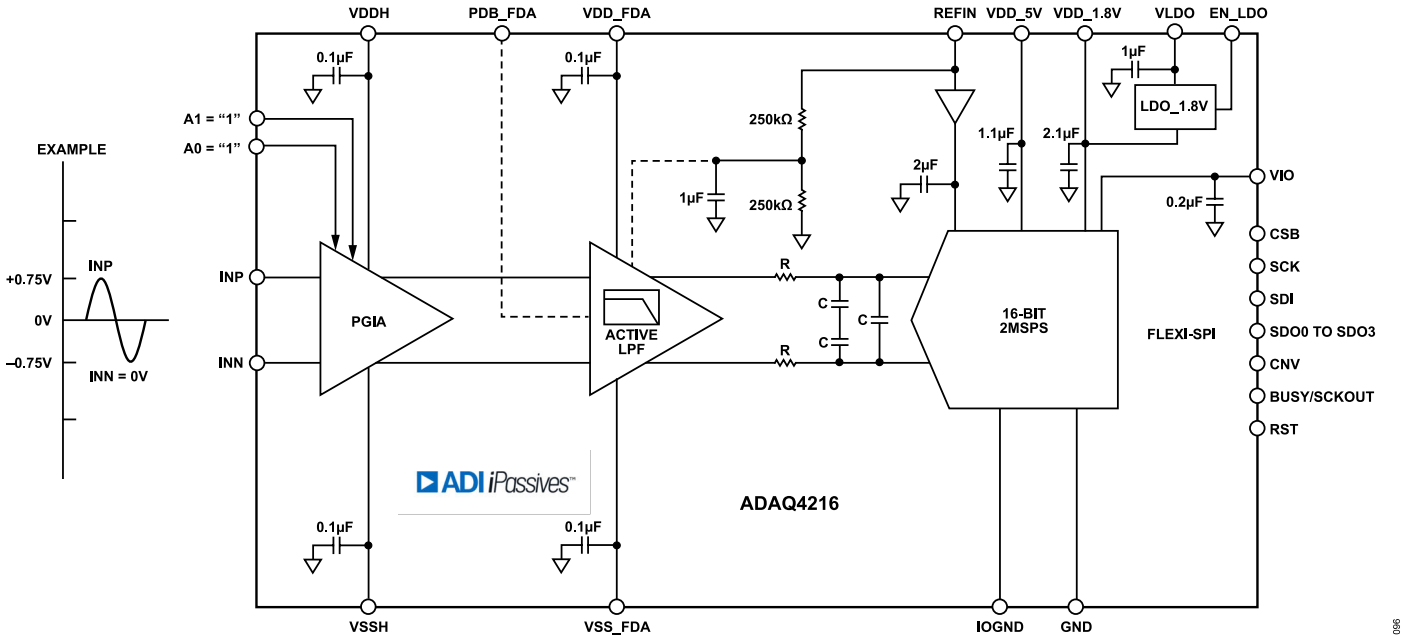


Figure 96. Single-Ended Input Configuration with G = 20/3V/V

APPLICATIONS INFORMATION

REFERENCE CIRCUITRY DESIGN

The ADAQ4216 requires an external reference to define its input range. This reference must be within 4.096V to 5V. The optimal choice for a 4.096V reference is the ADR4540 or the LTC6655LN-4.096, for a 5V reference, use the ADR4550 or LTC6655LN-5. The µModule has several features that reduce the charge pulled from the reference, which makes the ADAQ4216 much easier to use than the discrete implementations. The external reference is connected to the REFIN pin, which has an internal precision buffer that isolates the reference from the µModule circuitry. The buffer has a high-input impedance and small input current (5nA typical). The REFIN pin is also connected to a 500kΩ voltage divider that generates the VOCM of the ADC driver, which draws input current (10µA typical). An internal 2µF capacitor on the output of the buffer provides optimal reference bypassing and simplifies PCB design by reducing component count and layout sensitivity. An RC circuit between the reference and the REFIN pin can be used to filter reference noise (see Figure 97). Suggested values are 100Ω < R < 1kΩ and C ≥ 10µF.

In applications where a burst of samples is taken after idling for long periods, as shown in Figure 98, the reference current (I_{REF}) quickly goes from approximately 10µA to about of 12µA at 2MSPS. This step in DC current draw triggers a transient response in the reference that must be considered because any deviation in the reference output voltage affects the accuracy of the output code. If the reference is driving the REFIN pins, the internal buffer is able to handle these transitions.

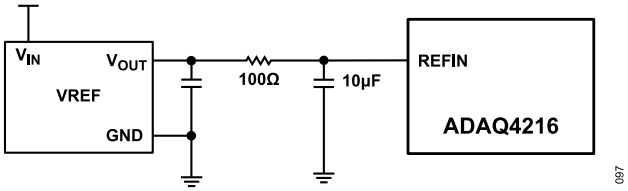


Figure 97. Reference with Noise Filter

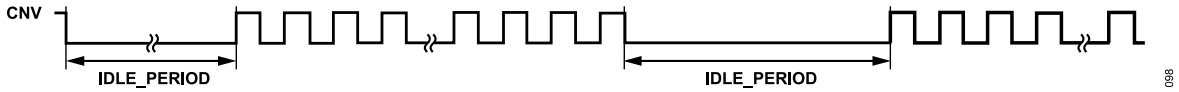


Figure 98. CNV Waveform Showing Burst Sampling

APPLICATIONS INFORMATION

ADC RESET

The ADAQ4216 provides two options for performing an ADC reset using the serial interface. A hardware reset is initiated by pulsing the voltage on the $\overline{RST}$ pin low. A software reset is initiated by setting both the SW_RESET and SW_RESETX bits in the Interface Configuration A register to 1 in the same write instruction (for more details, see the Interface Configuration A Register section).

Performing a hardware or software reset asserts the RESET_OCCURRED bit in the digital diagnostics register (for more details, see the Digital Diagnostics Register section). The RESET_OCCURRED bit is cleared by writing the bit with a 1. RESET_OCCURRED can be used by the digital host to confirm that the ADAQ4216 has executed a device reset.

The ADAQ4216 is designed to generate a power-on reset (POR) when VDD_5V and VDD_1.8V are first applied. A POR resets the state of the user configuration registers and asserts the RESET_OCCURRED bit. If VDD_5V or VDD_1.8V drops below its specified operating range, a POR occurs. It is recommended to perform a hardware or software reset after a POR.

Figure 99 shows the timing diagram for performing an ADC reset using the $\overline{RST}$ input. The minimum $\overline{RST}$ pulse width is 50ns, represented by $t_{RESETPW}$ in Figure 99 and Table 1. A reset must be performed no sooner than 3ms after the power supplies are valid and stable (this delay is represented by t_{RESET_DELAY} in Figure 99 and Table 1).

After a hardware or software reset, no SPI commands or conversions can be started for 750µs.

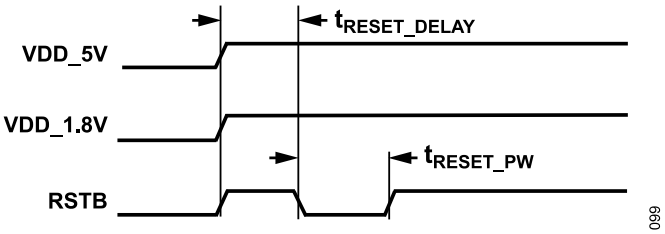


Figure 99. POR Timing

POWER SUPPLIES

The recommended power-up sequence for the supply pins of the ADAQ4216 is shown in Figure 100. The recommended sequence is power up the PGIA (VDDH and VSSH) first, then the FDA (VDD_FDA and VSS_FDA) along with the supplies of the ADC (VDD_5V, VLDO and VIO), then bring up the reference voltage (REFIN) and lastly turning on the input signal at INP and INN pins. Care must be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section.

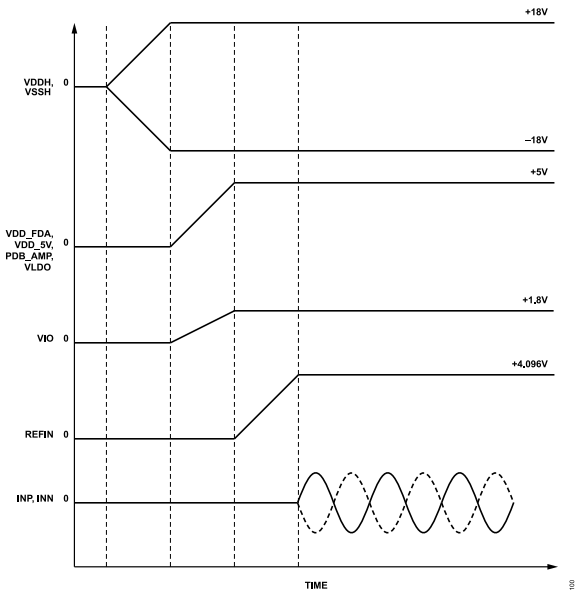


Figure 100. Power Supply Sequence

The voltage range for the VDD_5V supply depends on the chosen reference voltage (see the parameter Internal Reference Buffer in Table 1). Figure 101 shows the minimum and maximum values for VDD_5V with respect to REFIN. VDD_5V voltage values above the maximum or below the minimum result in either damage to the device or degraded performance.

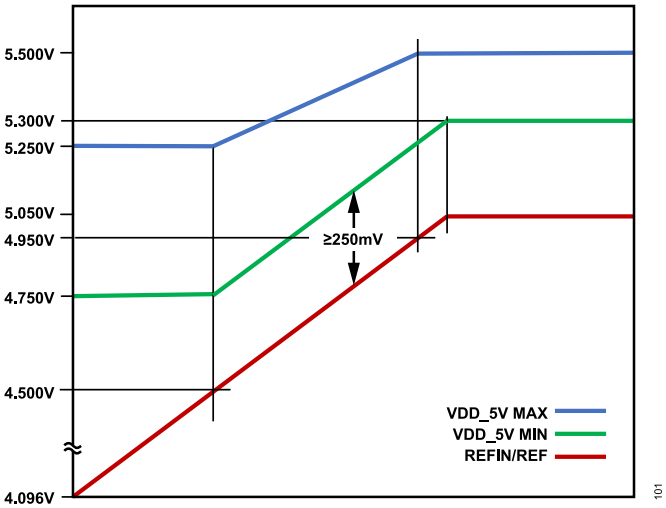


Figure 101. VDD_5V Minimum and Maximum Values for REFIN

The ADAQ4216 has a POR circuit that resets the ADAQ4216 at initial power-up or whenever VDD_5V or VDD_1.8V drops below its specified operating range.

Note that the VDD_5V and the VLDO supplies have internal 1µF bypass capacitors inside the package, VIO has an internal 0.2µF bypass capacitor, while VDDH, VSSH, VDD_FDA, VSS_FDA, and VDD have internal 0.1µF bypass capacitor. These internal capacitors reduce BOM count and solution size. If the bulk-supply bypass

APPLICATIONS INFORMATION

capacitors are not close to the ADC, add an external capacitors next to the ADC. The minimum rise time for all supplies is 100µs.

Power Consumption States

During a conversion, the power consumption of the ADAQ4216 is at its highest. When the conversion is complete, it enters a standby state and much of the internal circuitry is powered down, and current consumption drops to less than 20% relative to the conversion state. To ensure full accuracy, some circuitry, including the reference buffer, remains powered on during the standby state.

The device can be placed into a lower power shutdown state during periods when the convert clock is idle by writing 0x3 to the OPERATING_MODES bit field of the device configuration register (for more details, see the Device Configuration Register section). The default value of this bit field is [00] for normal operating mode. In the shutdown state, the current consumption typically drops to less than 10µA.

Shutdown Mode

When the ADC enters shutdown mode, the internal reference buffer is disabled and a 500Ω switch connects REFIN to the output of the internal reference buffer, which keeps the 2µF capacitor on the output of the internal buffer charged up to allow fast recovery when the ADC exits shutdown mode. Because of this keep-alive switch, there is some charge injected to the REFIN pin when the ADC enters shutdown mode (400pC) and exits shutdown mode (5pC). When leaving shutdown mode, the output of the internal buffer is accurate after 30µs.

SERIAL INTERFACE

The ADAQ4216 supports a multilane SPI serial digital interface with a common bit clock (SCK). The flexible VIO pins supply allows the ADAQ4216 to communicate with any digital logic operating between 1.2V and 1.8V. However, for the VIO pins levels less than 1.4V, the IO2X bit in the output driver register must be set to 1 (for more details, see the Output Driver Register section). The serial output data is clocked out on up to 4 SDO lanes (see Figure 102). An echo clock mode that is synchronous with the output data is available to ease timing requirements when using isolation on the digital interface. A host clock mode is also available and uses an internal oscillator to clock out the data bits. The SPI Clocking Mode, Echo Clock Mode, Host Clock Mode, Single-Data Rate Mode, Dual-Data Rate Mode, 1-Lane Output Data Clocking Mode, 2-Lane Output Data Clocking Mode, 4-Lane Output Data Clocking Mode, and Data Output Modes Summary sections describe the operation of the ADAQ4216 SPI.

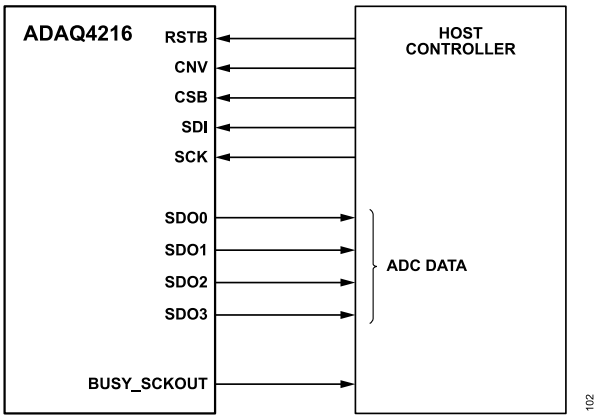


Figure 102. ADAQ4216 Multilane SPI

SPI SIGNALS

The SPI is a multilane interface that is used to both configure the ADC as well as retrieve sampled data. It consists of the following signals:

- $\overline{CS}$ (input) (chip select). $\overline{CS}$ must be set to low to initiate and enable a data transfer to or from the SDI pins or SDOx pins of the ADC. $\overline{CS}$ timing for reading sample data can be moderated by observing the state of the BUSY pin. For echo clock mode and host clock mode, $\overline{CS}$ timing must be controlled by the host processor because the BUSY_SCKOUT pin is used as the bit clock output for these clocking modes.
- SDI (input). Serial data input stream from the host controller to the ADC. The SDI signal is only used when writing data into one of the user registers of the ADAQ4216.
- CNV (input). The CNV signal is sourced by the host controller and initiates a sample conversion. The frequency of the CNV signal determines the sampling rate of the ADAQ4216. The maximum frequency of the CNV clock is 2MSPS.
- SCK (input). Serial data clock sourced by the host controller. The maximum SCK rate supported for output data transfer is 100MHz. For register reads and writes, the maximum SCK rate is 86MHz for the VIO pins > 1.71V, and 81MHz for 1.14V ≤ the VIO pins < 1.71V.
- SDO0 through SDO3 (outputs). Data lanes to the host controller. The number of active data lanes can be either 1-lane, 2-lane, or 4-lane (see Table 14). The number of data lanes is configured in the Modes Register section.
- BUSY_SCKOUT (output). The behavior of the BUSY_SCKOUT pin is dependent on the selected clocking mode. Table 13 defines the behavior of the BUSY_SCKOUT pin for each clocking mode.

Table 13. BUSY_SCKOUT Pin Behavior vs. Clocking Mode

Clocking Mode	Behavior
SPI Clocking Mode	Valid BUSY_SCKOUT pin signal for the ADC conversion status. The busy signal on the BUSY_SCKOUT pin goes high when a conversion is triggered by the CNV signal. The busy signal on the BUSY_SCKOUT pin goes low when the conversion is complete.
Echo Clock Mode	Bit clock. The BUSY_SCKOUT pin is a delayed version of SCK input.
Host Clock Mode	Bit clock. The BUSY_SCKOUT pin sources the clock signal from the internal oscillator.

Register Access Mode

The ADAQ4216 offers programmable user registers that are used to configure the device, as shown in the Registers section. By default, at power-up, the device is in conversion mode. Therefore, to access the user registers, a special access command must be sent by the host controller over the SPI, as shown in Figure 5. When this register access command is sent over the SPI, the device enters the register configuration mode. To readback the values from one of the user registers listed in the Registers section, the host controller must send the pattern shown in Figure 4. To write to one of the user registers, the host controller must send the pattern shown in Figure 3. In either case (read/write), the host controller must always issue 24 clock pulses on SCK line and pull $\overline{CS}$ low for the entire transaction.

After writing to/reading from the appropriate user registers, the host controller must exit the register configuration mode by writing 0x01 to register address 0x0014 as detailed in the EXIT Configuration Mode Register section. An algorithm for register read/write access is as follows:

1. Perform a readback from a dummy register address 0x3FFF, to enter the register configuration mode.
2. Readback from or write to the required user register addresses.
3. Exit the register configuration mode by writing 0x01 to register address 0x0014. Exiting register configuration mode causes the register updates to take effect.

SERIAL INTERFACE

Stream Mode

The ADAQ4216 also offers a way to perform bulk register read/write transactions while the ADAQ4216 is in register configuration mode. To perform bulk read/write registers transactions, $\overline{CS}$ must be kept low and SCK pulses must be issued in multiples of 8 as each register is only one byte (8 bits) wide. In stream mode, only address decrementing is allowed, which means that the user can readback from/write to the initial register address and register addresses that are directly below the initial register address. It is recommended that register accesses in stream mode be applied to register blocks with contiguous addresses. However, it is possible to address registers that are not present in the register map. To do so, simply write all zeros to these registers, or, when reading back, simply discard the contents read from these registers since it is random data. To see which register address is valid and continuous, see the Registers section. For example, to readback a 16-bit offset value in one shot, the user must issue 16 SCK pulses starting from Register Address 0x0018. Figure 103 shows timing diagram for bulk read starting at a given address.

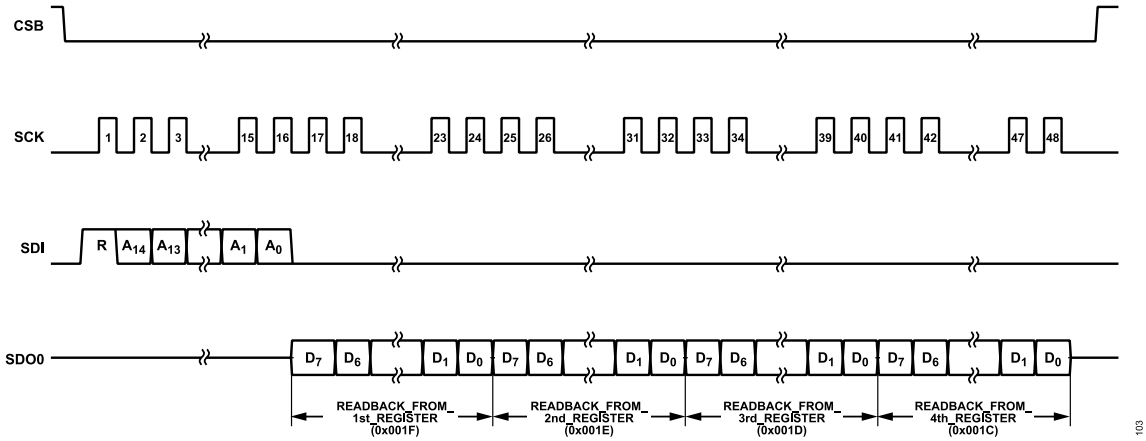


Figure 103. Stream Mode Bulk Register Readback Operation

SERIAL INTERFACE

SAMPLE CONVERSION TIMING AND DATA TRANSFER

A conversion is started on the rising edge of the CNV signal, as shown in Figure 104. Once the conversion is complete, $\overline{CS}$ can be asserted, which causes the current conversion result to be loaded into the output shift register.

As shown in Figure 104, there are two optional data transfer zones for sample N. Zone 1 represents the use case where $\overline{CS}$ is asserted immediately following the deassertion of BUSY signal for the sample N conversion (in SPI conversion mode), or after 300ns for echo and host clock modes. For Zone 1, the available time to read out sample N is given by:

Zone 1 data read window

$$= t_{CYC} - t_{CONV} - t_{QUIET\_CNV\_ADV}$$

For example, if F_{CNV} is 2MSPS (t_{CYC} = 500ns) and using the typical value of t_{CONV} (282ns), the available window width is 198.4ns (= 500ns – 282ns – 19.6ns).

Zone 2 represents the case where assertion of $\overline{CS}$ to read sample N is delayed until after the conversion for sample N+1 has been initiated.

To prevent data corruption, a quiet zone must be observed before and after each rising edge of the CNV signal, as shown in Figure 104. The quiet zone immediately before the rising edge of CNV is labeled as $t_{QUIET\_CNV\_ADV}$, and is equal to 19.6ns. The quiet zone immediately after the rising edge of CNV is labeled $t_{QUIET\_CNV\_DELAY}$, and is equal to 9.8ns. Assuming that the $\overline{CS}$ is asserted immediately after the quiet zone around the rising edge of CNV, the amount of time available to clock out the data is:

Zone 2 data read window

$$= t_{CYC} - t_{QUIET\_CNV\_DELAY} - t_{QUIET\_CNV\_ADV}$$

For example, if F_{CNV} is 2MSPS (t_{CYC} = 500ns) and using the typical value of t_{CONV} (282ns), the available window width is 470.6ns (= 500ns – 9.8ns – 19.6ns). The Zone 2 transfer window is longer than the Zone 1 window. This can enable the use of a slower SCK on the SPI and ease the timing requirements for the interface. When using Zone 2 for the data transfer, it is recommended to assert $\overline{CS}$ immediately after the quiet zone. However, it must be asserted at least 25ns before the falling edge of BUSY for sample N+1. If not, then sample N is overwritten with sample N+1.

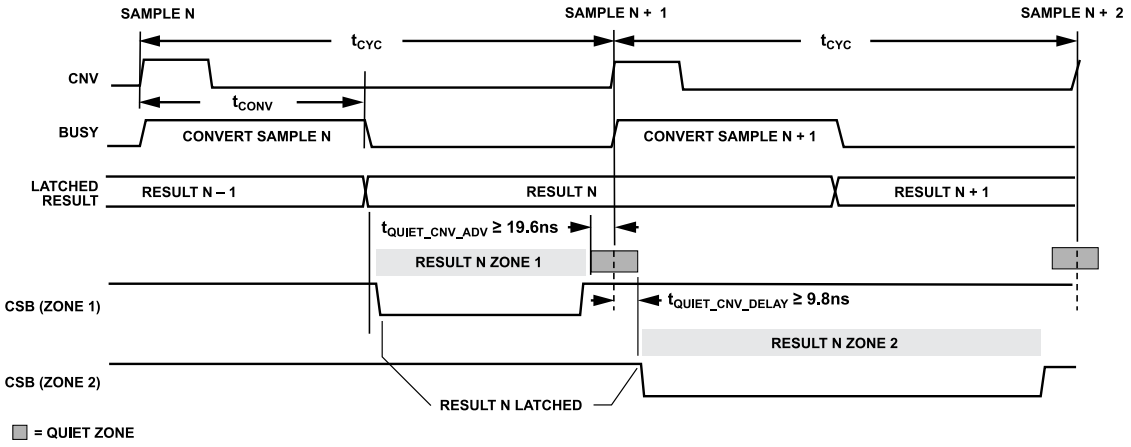


Figure 104. Example Timing for Data Transfer Zones

SERIAL INTERFACE

CLOCKING MODES

This section covers the various clocking modes supported by the ADAQ4216 SPI. These modes are available for 1-lane, 2-lane, and 4-lane. The clocking mode is configured in the modes register (for register descriptions, see Table 16).

SPI Clocking Mode

SPI clocking mode is the default clocking mode of the ADAQ4216 and is equivalent to a host-sourced bit clock (SCK), in which the host controller uses its own clock to latch the output data. The SPI-compatible clocking mode is enabled by writing 0x0 to the CLK_MD bit field of the modes register (for more details, see the Modes Register section). The interface connection is shown in Figure 102. In this mode, the BUSY_SCKOUT pin signal is valid and indicates the completion of a conversion (high-to-low transition of the BUSY_SCKOUT pin). A simplified sample cycle is shown in Figure 105. When not in averaging mode, if the host controller does not use the BUSY_SCKOUT pin signal to detect the completion of a conversion and instead uses an internal timer to retrieve the data, the host controller must wait at least 300ns after the rising edge of the CNV pulse before asserting $\overline{CS}$ low. When operating in block averaging mode, the host controller must assert $\overline{CS}$ low no sooner than 300ns after the rising edge of the CNV pulse for the last sample in the block.

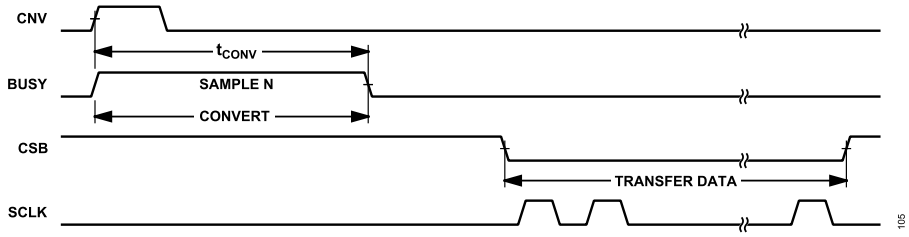


Figure 105. Typical Sample Cycle for SPI Clocking Mode

SERIAL INTERFACE

Echo Clock Mode

Figure 106 shows the signal connections for the echo clock mode. The echo clock mode is enabled by writing 0x1 to the CLK_MD bit field of the modes register (for more details, see the Modes Register section). In this mode, the BUSY_SCKOUT pin cannot be used to detect a conversion completion. The BUSY_SCKOUT pin becomes a bit clock output and is sourced by looping through the SCK of the host controller to the BUSY_SCKOUT pin (with some fixed delay, 5.4ns to 7.9ns, which depends on the voltage of the VIO pins). To begin retrieving the conversion data in nonaveraging mode, the host controller must assert $\overline{CS}$ low no sooner than 300ns after the rising edge of the CNV pulse. When the ADC is configured for block averaging mode, the host controller must assert $\overline{CS}$ low no sooner than 300ns after the rising edge of the CNV pulse for the last sample in the block. Example timing diagrams are shown in the Data Clocking Requirements and Timing section. When echo clock mode is enabled, the BUSY_SCKOUT pin is aligned with the SDOx pins transitions, making the data and clock timing insensitive to asymmetric propagation delays in the paths of the SDOx pins and SCK pins.

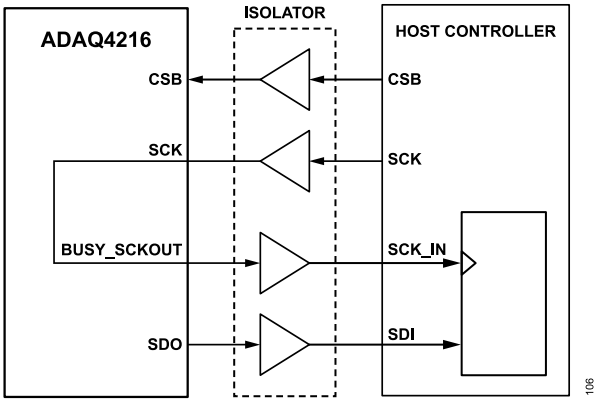


Figure 106. Echo Clock Mode Signal Path Diagram

Host Clock Mode

When enabled, host clock mode uses the internal oscillator as the bit clock source. The host clock mode is enabled by writing 0x2 to the CLK_MD bit field of the modes register. The bit clock frequency can be programmed in the OSC_DIV bit field in the internal oscillator register, with available divisor values of 1, 2, or 4 (for more details, see the Internal Oscillator Register section). Figure 107 shows the signal connections for the host clock mode. In this mode, the BUSY_SCKOUT pin provides the bit clock output and cannot be used to detect a conversion completion. The ADAQ4216 automatically calculates the number of clock pulses required to clock out the conversion data based on word size, number of active lanes, and choice of single-data rate mode or dual-data rate mode. The number of clock pulses can be read from the OSC_LIMIT bit field of the internal oscillator register. Note that for a 16-bit differential data word (the OUT_DATA_MD field = 000 in the Modes Register), the ADAQ4216 add an additional eight clock pulses for a total of 24 clock pulses. The 16-bit data word is padded with eight zero bits. The SCK_IN from the host must not be active. When retrieving the conversion data in nonaveraging mode, the host must not assert $\overline{CS}$ low sooner than 300ns after the rising edge of the CNV pulse. When the ADC is configured in averaging mode for 2^N averages, the host must not assert $\overline{CS}$ low sooner than 300ns after the rising edge of the CNV pulse for the last sample in the block.

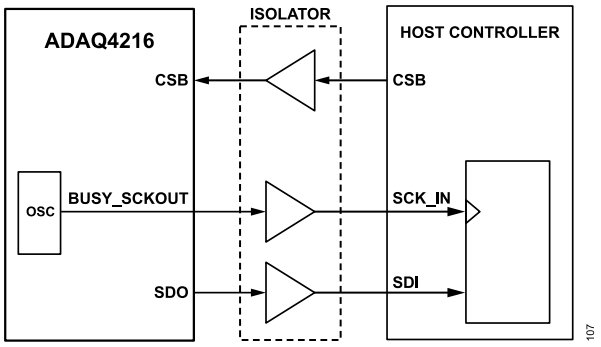


Figure 107. Host Clock Mode Signal Path Example

Single-Data Rate Mode

Single-data rate clocking (SDR), in which one bit (per active lane) is clocked out during a single clock cycle, is supported for all output configurations and sample formats (see Table 14). The SDR clocking mode is enabled by default at power-up or can be enabled by writing 0 to the DDR_MD bit of the modes register (for more details, see the Modes Register section).

Dual-Data Rate Mode

Dual-data rate (DDR) mode (two data bit transitions per clock cycle per active lane) is available only for host clock mode and echo clock mode.

The DDR clocking mode is enabled by writing 1 to the DDR_MD bit of the modes register (for more details, see the Modes Register section). The DDR mode uses half the number of SCK pulses to clock out conversion data in comparison to SDR mode.

1-Lane Output Data Clocking Mode

1-lane is the default output data clocking mode at power-up. The 1-lane output data clocking mode is enabled by writing 0x0 to the LANE_MD bit of the modes register (for more details, see the Modes Register section). The active lane is SDO0. Example timing diagrams for 1-lane mode using SPI clocking mode, echo clock mode, and host clock mode are shown in the Data Clocking Requirements and Timing section.

2-Lane Output Data Clocking Mode

When 2-lane output data clocking mode is enabled, the sample word bits are split between two SDO lanes. Figure 113 shows how the bits are allocated between the lanes for 2-lane mode. The bit

SERIAL INTERFACE

arrangement is the same for SPI clock mode, echo clock mode, and host clock mode. A 2-lane output data clocking mode is enabled by writing 0x1 to the LANE_MD bit of the modes register (for more details, see the Modes Register section). The host controller must recombine the data coming from the SDO lanes to reconstruct the original sample word. The number of SCK pulses required to clock out the conversion data is reduced by one-half with respect to the 1-lane mode. Table 14 lists the active SDO lanes for 2-lane mode. Example timing diagrams for 2-lane mode using SPI clock mode, echo clock mode, and host clock mode are shown in the Data Clocking Requirements and Timing section.

4-Lane Output Data Clocking Mode

When 4-lane output data clocking mode is enabled, the sample word bits are split between four SDO lanes. Figure 114 shows how the bits are allocated between the lanes for 4-lane mode. The bit arrangement is the same for SPI clock mode, echo clock mode, and host clock mode. A 4-lane output data clocking mode is enabled by writing 0x2 to the LANE_MD bit of the modes register (for more details, see the Modes Register section). The host controller must recombine the data coming from the SDO lanes to reconstruct the original sample word. The number of SCK pulses required to clock out the conversion data is reduced by one-fourth with respect to the 1-lane output data clocking. The active SDO lanes for 4-lane mode are shown in Table 14. Example timing diagrams for 4-lane mode using SPI clock mode, echo clock mode, and host clock mode are shown in the Data Clocking Requirements and Timing section.

Data Output Modes Summary

Table 14 is a summary of the supported data output modes of the ADAQ4216.

Table 14. ADAQ4216 Supported Data Output Modes

Number of Lanes	Active SDO Lanes	Clock Mode	Supported Data Clocking Mode	Output Sample Data-Word Length
1	SDO0	SPI	SDR only	16, 24 or 32
		Echo	SDR and DDR	16, 24 or 32
		Host	SDR and DDR	24 or 32
2	SDO0, SDO1	SPI	SDR only	16, 24 or 32
		Echo	SDR and DDR	16, 24 or 32
		Host	SDR and DDR	24 or 32
4	SDO0, SDO1, SDO2, SDO3	SPI	SDR only	16, 24 or 32
		Echo	SDR and DDR	16, 24 or 32
		Host	SDR and DDR	24 or 32

SERIAL INTERFACE

DATA CLOCKING REQUIREMENTS AND TIMING

Basic and Averaging Conversion Cycles

Figure 108 shows the basic conversion cycle for a single sample. This cycle applies to SPI clocking mode. When using echo clock mode and host clock mode, the BUSY_SCKOUT pin function is disabled and the bit clock is sourced on the BUSY_SCKOUT pin. The data transfer must meet the requirements described in the Sample Conversion Timing and Data Transfer section.

Table 15 contains the minimum and maximum values for the conversion timing parameters, which apply to all clocking modes.

Table 15. Conversion Cycle Timing Parameters

Parameter	Min	Max
t_{CNVH}	10ns	No specific maximum
t_{CNVL}	20ns	No specific maximum
t_{CONV}	264ns	300ns

The duration of the data transfer period is dependent on the sample resolution, number of active lanes, SCK frequency, and data clocking mode (SDR or DDR). The nominal value of the transfer duration is given by

$$Data\ \ Transfer\ \ Duration = t_{TRANS} = \frac{N_{BITS}}{M_{LANES}} \times \frac{1}{f_{SCK}} \times \frac{1}{K}\ \ seconds$$

where:
N_{BITS} = number of bits to clock out.
M_{LANES} = number of lanes used to clock out the data (1, 2, or 4).
f_{SCK} = SCK clock frequency, in Hz.
K = 1 (SDR only, DDR not available for SPI mode clocking).

For a given f_{SCK}, number of data lanes, sample word size, and SDR/DDR mode, the minimum sample period when using Zone 1 for the data transfer is as follows:

Minimum Zone 1 Sample Period:

$$t_{CYC} \geq \left(\frac{N_{BITS}}{M_{LANES} \times f_{SCK} \times K}\right) + t_{CONV} + t_{QUIET\_CNV\_ADV}$$

The minimum sample period when using Zone 2 for data transfer is as follows:

$$t_{CYC} \geq \left(\frac{N_{BITS}}{M_{LANES} \times f_{SCK} \times K}\right) + t_{QUIET\_CNV\_DELAY} + t_{QUIET\_CNV\_ADV}$$

Figure 109 shows a typical conversion cycle when the averaging mode is active and SPI clocking mode is being used. The BUSY signal is asserted for a number of CNV clock periods that are equal to the configured number of samples to be averaged. The averaged sample is available when the BUSY signal is deasserted. Similar to nonaveraged mode, if the configured clocking mode is either echo clock or host clock, the BUSY signal is replaced by the output bit clock (SCKOUT). The host controller must manage the timing for asserting $\overline{CS}$.

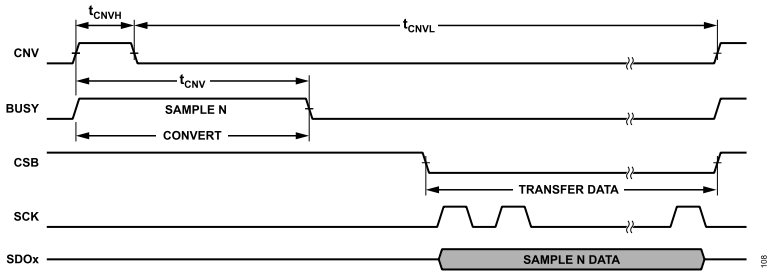


Figure 108. Basic Single Sample Conversion Cycle

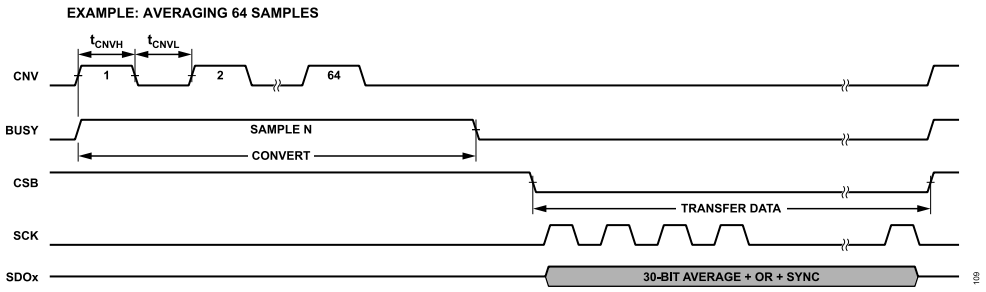


Figure 109. Example Conversion Cycle for Averaging Mode

SERIAL INTERFACE

The two transfer zones that exist in nonaveraging mode also exist in averaging mode (see Figure 110, Figure 111, and Figure 112).

To prevent data corruption, it is necessary to avoid SPI rising and falling edges signals taking place during quiet zones.

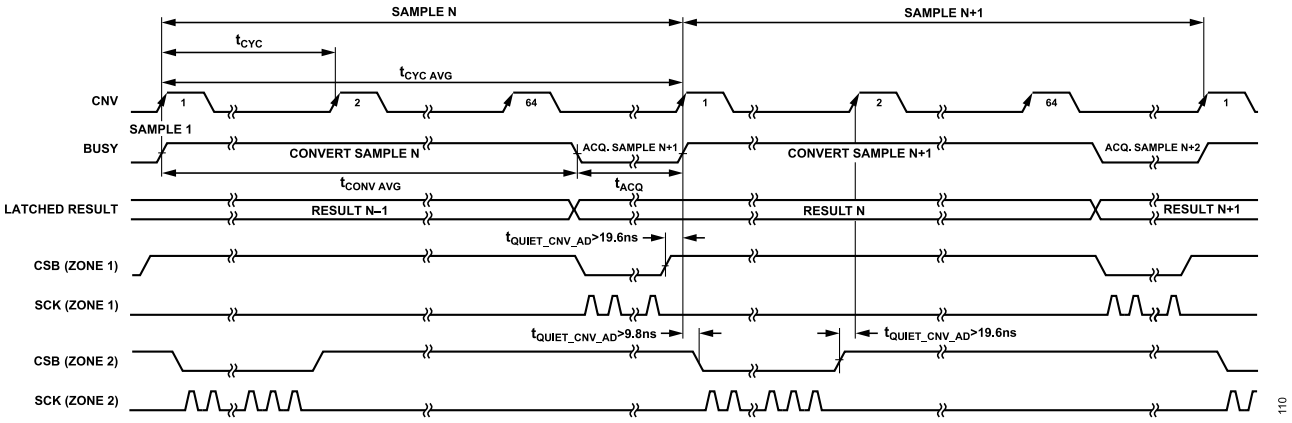


Figure 110. Example of Different Zones in Averaging Mode (64 Samples Averaged)

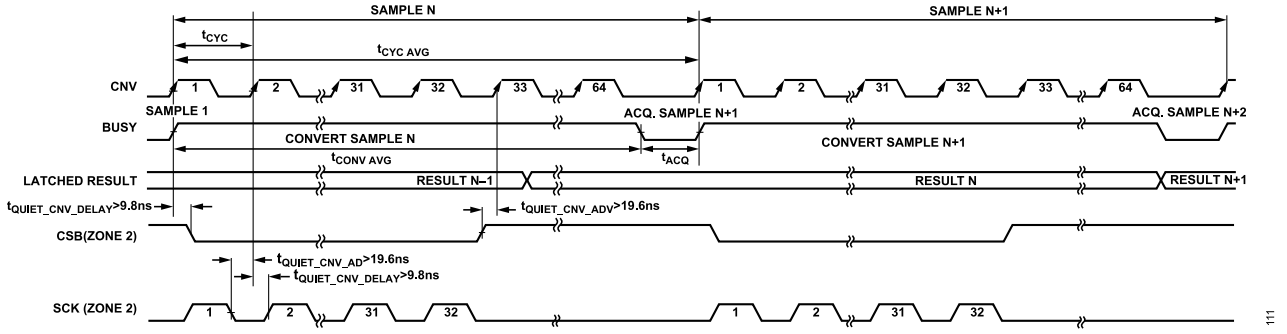


Figure 111. Example of Zone 2 in Averaging Mode (1 Bit per Sample)

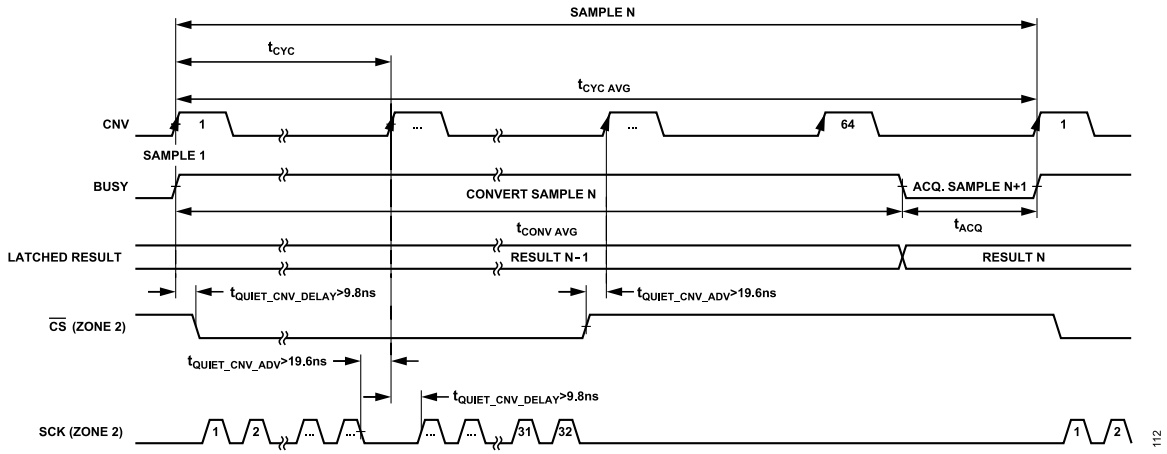


Figure 112. Example of Zone 2 in Averaging Mode (N Bits per Cycle)

SERIAL INTERFACE

SPI Clocking Mode Timing Diagrams

1-Lane, SDR Mode

Figure 6 shows a conversion cycle for 1-lane data output, SDR mode (1-bit per clock cycle).

2-Lane, SDR Mode

Figure 113 shows a conversion cycle for 2-lane data output using SDR clocking mode. For more details, see the 2-Lane Output Data Clocking Mode section.

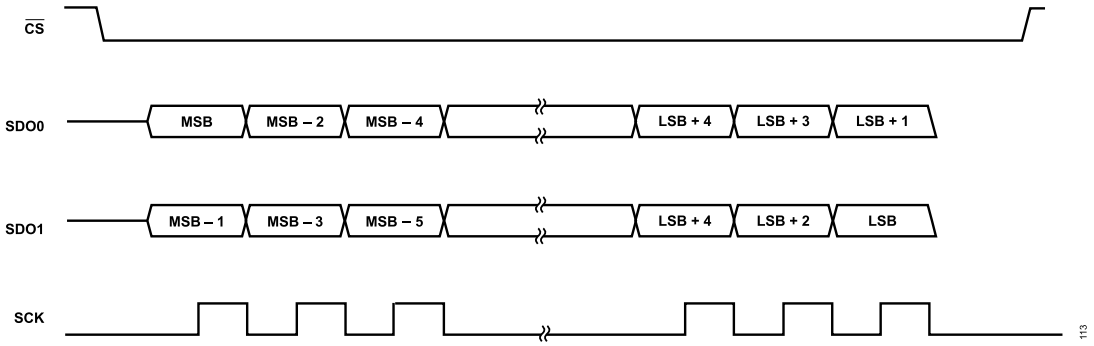


Figure 113. 2-Lane Mode, SDR Timing Diagram

SERIAL INTERFACE

4-Lane, SDR Mode

Figure 114 shows a conversion cycle for 4-lane data output using SDR clocking mode. For more details, see the 4-Lane Output Data Clocking Mode section.

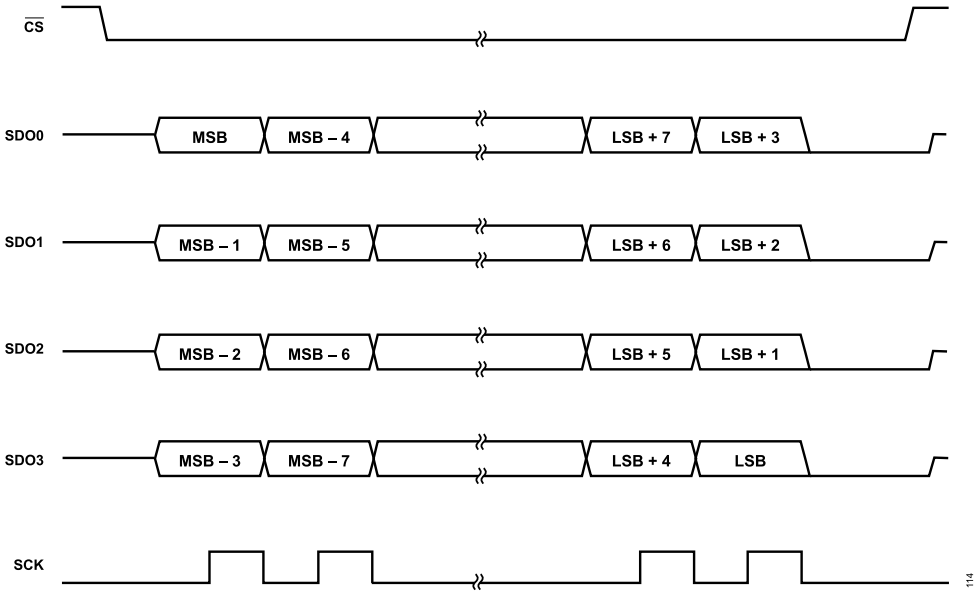


Figure 114. 4-Lane, SDR Timing Diagram

SERIAL INTERFACE

Echo Clock Timing Diagrams

1-Lane, SDR Mode, Echo Clock Mode

Figure 7 shows the timing relationships for SDR mode (1-bit per SCK period) in 1-lane echo clock mode. The timing relationships between the signals apply to both 16-bit and 32-bit sample word formats.

SCKOUT is a delayed version of the incoming SCK. The delay (t_{DSDO}) has a maximum value of 5.6ns (at V_{IO} > 1.71V). Changes in SDOx logic states are aligned to the rising edges of SCKOUT. The clock and data edge alignments are the same for 1-lane, 2-lane, and 4-lane output data modes.

1-Lane, DDR Mode, Echo Clock Mode

Figure 8 shows the timing relationships for DDR mode (2-bit transitions per SCKOUT period) in 1-lane mode echo clock mode. The timing relationships between the signals apply to both 16-bit and 32-bit sample word formats.

Similar to SDR mode, SCKOUT is a delayed version of the incoming SCK. Changes in SDOx logic states are aligned to both rising and falling edges of SCKOUT.

Host Clock Mode Timing

1-Lane, Host Clock Mode, SDR

Figure 9 shows the timing relationships for host clock mode when using SDR mode and 1-lane mode. Similar to echo clock mode, the clock rising edges are aligned to the data bit transitions. The frequency of SCKOUT signal is controlled by the OSC_DIV value programmed in the internal oscillator register (for more details, see the Internal Oscillator Register section). Note that when the output data format is 16-bit differential (OUT_DATA_MD = 000 in the Modes Register), each 16-bit sample is padded with eight zeros, which makes the total word length to 24 bits. The host processor discards these bits when processing the data.

1-Lane, Host Clock Mode, DDR

Figure 10 shows the timing relationships for host clock mode when using DDR. Similar to echo clock mode, the rising and falling clock edges are aligned to the data bit transitions. The frequency of SCKOUT signal is controlled by the OSC_DIV value programmed in the internal oscillator register (for more details, see the Internal Oscillator Register section). Note that when the output data format is 16-bit differential (OUT_DATA_MD = 000 in the Modes Register), each 16-bit sample is padded with eight zeros, which makes the total word length to 24 bits. The host processor discards these bits when processing the data.

LAYOUT GUIDELINES

The following layout guidelines are recommended to achieve maximum performance of the ADAQ4216:

- The ADAQ4216 contains internal 1µF bypass capacitors for VDD_5V and VDD_1.8V, and VIO contains an internal 0.2µF capacitor, so no external bypass capacitors are required. This saves board space, bill of materials count, and reduces layout sensitivity.
- It is recommended to have all the analog signals flow in from the left side of the ADAQ4216 and all the digital signals to flow in and out from the right side of the ADAQ4216 because this helps isolate analog signals from digital signals.
- Use a solid ground plane under the ADAQ4216 and connect all the analog ground (GND) pins and digital ground (IOGND) pins to the shared ground plane to avoid formation of ground loops.
- Traces routed to the REFIN pin must be isolated and shielded from other signals. Avoid routing signals beneath the reference trace (REFIN). If a noise reduction filter is placed between the output of the reference (or buffer) and the chosen reference input, it must be placed as close as possible to the ADAQ4216.

REGISTERS

The ADAQ4216 has programmable user registers that are used to configure the device. These registers can be accessed while the ADAQ4216 is in register configuration mode. Table 16 shows the complete list of the ADAQ4216 user registers and bit fields in the registers. The Register Details section contains details about the functions of each of the bit fields. The access mode specifies whether the register is comprised only of read-only bits (R) or a mix of read-only and read/write bits (R/W). Read-only bits cannot be overwritten by an SPI write transaction, but read/write bits can.

Table 16. ADAQ4216 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	INTERFACE_CONFIG_A	[7:0]	SW_RESET	RESERVED	ADDR_ASCENSION	SDO_ENABLE	RESERVED			SW_RESETX	0x10	R/W
0x01	INTERFACE_CONFIG_B	[7:0]	SINGLE_INST	STALLING	RESERVED		SHORT_INSTRUCTION	RESERVED			0x00	R/W
0x02	DEVICE_CONFIG	[7:0]	RESERVED						OPERATING_MODES		0x00	R/W
0x03	CHIP_TYPE	[7:0]	RESERVED				CHIP_TYPE				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x00	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x20	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x00	R
0x0A	SCRATCH_PAD	[7:0]	SCRATCH_VALUE								0x00	R/W
0x0B	SPI_REVISION	[7:0]	SPI_TYPE		VERSION						0x81	R
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x0E	STREAM_MODE	[7:0]	LOOP_COUNT								0x00	R/W
0x11	INTERFACE_STATUS_A	[7:0]	RESERVED		CLOCK_COUNT_ERR	RESERVED					0x00	R/W
0x14	EXIT_CFG_MD	[7:0]	RESERVED							EXIT_CONFIG_MD	0x00	R/W
0x15	AVG	[7:0]	AVG_SYNC	RESERVED	AVG_VAL						0x00	R/W
0x16	RESERVED	[7:0]	RESERVED								0x00	R/W
0x17	OFFSET_LB	[7:0]	USER_OFFSET[7:0]								0x00	R/W
0x18	OFFSET_HB	[7:0]	USER_OFFSET[15:8]								0x00	R/W
0x19	UNUSED1_LB	[7:0]	UNUSED1[7:0]								0x00	R/W
0x1A	UNUSED1_MB	[7:0]	UNUSED1[15:8]								0x00	R/W
0x1B	UNUSED1_HB	[7:0]	UNUSED1[23:16]								0x00	R/W
0x1C	GAIN_LB	[7:0]	USER_GAIN[7:0]								0x00	R/W
0x1D	GAIN_HB	[7:0]	USER_GAIN[15:8]								0x80	R/W
0x1E	UNUSED2_LB	[7:0]	UNUSED2[7:0]								0x00	R/W
0x1F	UNUSED2_HB	[7:0]	UNUSED2[15:8]								0x80	R/W
0x20	MODES	[7:0]	LANE_MD		CLK_MD		DDR_MD	OUT_DATA_MD			0x00	R/W
0x21	OSCILLATOR	[7:0]	OSC_LIMIT				OSC_DIV				0x00	R/W
0x22	IO	[7:0]	RESERVED							IO2X	0x00	R/W
0x23	TEST_PAT_BYTE0	[7:0]	TEST_DATA_PAT[7:0]								0x0F	R/W
0x24	TEST_PAT_BYTE1	[7:0]	TEST_DATA_PAT[15:8]								0x0F	R/W
0x25	TEST_PAT_BYTE2	[7:0]	TEST_DATA_PAT[23:16]								0x5A	R/W
0x26	TEST_PAT_BYTE3	[7:0]	TEST_DATA_PAT[31:24]								0x5A	R/W
0x34	DIG_DIAG	[7:0]	POWERUP_COMPLETED	RESET_OCCURRED	RESERVED					FUSE_CRC_EN	0x40	R/W
0x35	DIG_ERR	[7:0]	RESERVED							FUSE_CRC_ERR	0x00	R/W

REGISTER DETAILS

INTERFACE CONFIGURATION A REGISTER

Address: 0x00, Reset: 0x10, Name: INTERFACE_CONFIG_A

Interface configuration settings.

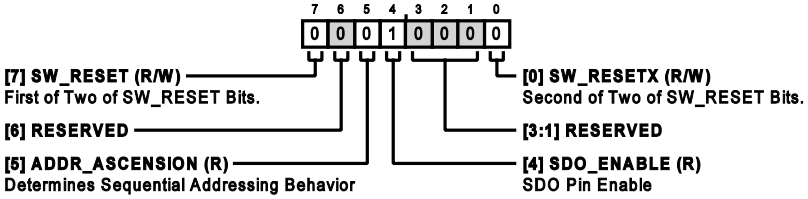


Table 17. Bit Descriptions for INTERFACE_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RESET	One of two of SW_RESET bits. This bit appears in two locations in this register. Both locations must be written at the same time to trigger a software reset of the part. All registers except for this register are reset to their default values.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
5	ADDR_ASCENSION	Determines sequential addressing behavior.	0x0	R
		0: Address accessed is decremented by one for each data byte when streaming.		
		1: Not a valid option.		
4	SDO_ENABLE	SDO Pin Enable.	0x1	R
[3:1]	RESERVED	Reserved.	0x0	R
0	SW_RESETX	Two of two of SW_RESET bits. This bit appears in two locations in this register. Both locations must be written at the same time to trigger a software reset of the part. All registers except for this register are reset to their default values.	0x0	R/W

INTERFACE CONFIGURATION B REGISTER

Address: 0x01, Reset: 0x00, Name: INTERFACE_CONFIG_B

Additional interface configuration settings.

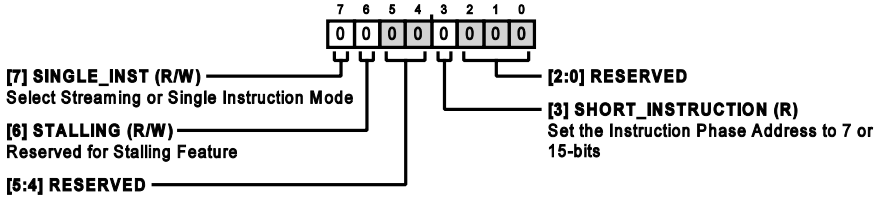


Table 18. Bit Descriptions for INTERFACE_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INST	Select streaming or single instruction mode. 0: Streaming mode is enabled. The address decrements as successive data bytes are received. 1: Single instruction mode is enabled.	0x0	R/W
6	STALLING	Reserved for Stalling Feature.	0x0	R/W
[5:4]	RESERVED	Reserved.	0x0	R
3	SHORT_INSTRUCTION	Set the instruction phase address to 7 bits or 15 bits. 0: 15-bit addressing. 1: 7-bit addressing.	0x0	R
[2:0]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

DEVICE CONFIGURATION REGISTER

Address: 0x02, Reset: 0x00, Name: DEVICE_CONFIG

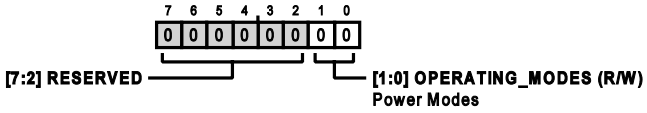


Table 19. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	OPERATING_MODES	Power modes. 00: Normal operating mode. 11: Shutdown mode.	0x0	R/W

CHIP TYPE REGISTER

Address: 0x03, Reset: 0x07, Name: CHIP_TYPE

The chip type is used to identify the family of Analog Devices products a given device belongs to. Use the chip type with the product ID to uniquely identify a given product.

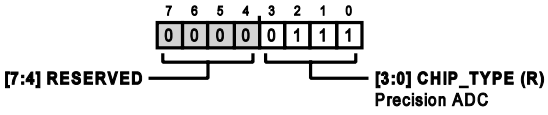


Table 20. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Precision ADC.	0x7	R

PRODUCT ID LOW REGISTER

Address: 0x04, Reset: 0x00, Name: PRODUCT_ID_L

Low byte of the product ID.

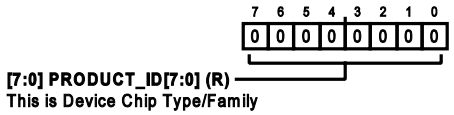


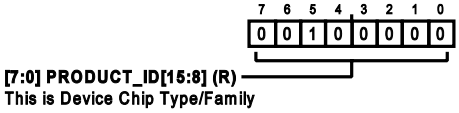
Table 21. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	This is the device chip type/family. Use the product ID with the chip type to identify a product.	0x0	R

PRODUCT ID HIGH REGISTER

Address: 0x05, Reset: 0x20, Name: PRODUCT_ID_H

High byte of the product ID.



REGISTER DETAILS

Table 22. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	This is the device chip type/family. Use the product ID with the chip type to identify a product.	0x20	R

CHIP GRADE REGISTER

Address: 0x06, Reset: 0x81, Name: CHIP_GRADE

Identifies product variations and device revisions.

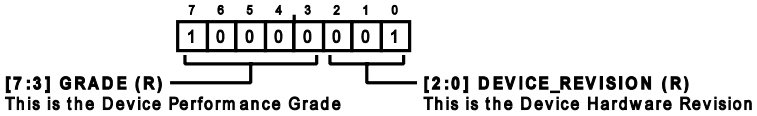


Table 23. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:3]	GRADE	This is the device performance grade. ADAQ4216: 0b11110.	0x1E	R
[2:0]	DEVICE_REVISION	This is the device hardware revision.	0x1	R

SCRATCH PAD REGISTER

Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

This register can be used to test writes and reads.

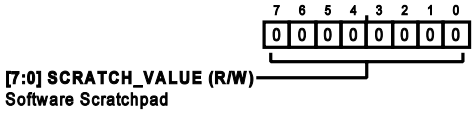


Table 24. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_VALUE	Software Scratchpad. Software can write to and read from this location without any device side effects.	0x0	R/W

SPI REVISION REGISTER

Address: 0x0B, Reset: 0x81, Name: SPI_REVISION

Indicates the SPI revision.

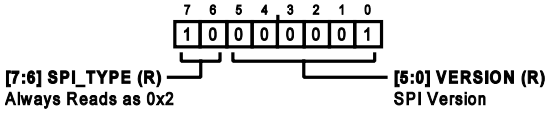


Table 25. Bit Descriptions for SPI_REVISION

Bits	Bit Name	Description	Reset	Access
[7:6]	SPI_TYPE	Always reads as 0x2.	0x2	R
[5:0]	VERSION	SPI Version.	0x1	R

REGISTER DETAILS

VENDOR ID LOW REGISTER

Address: 0x0C, Reset: 0x56, Name: VENDOR_L

Low byte of the vendor ID.

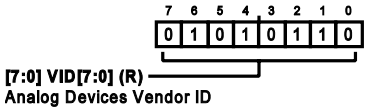


Table 26. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Analog Devices Vendor ID.	0x56	R

VENDOR ID HIGH REGISTER

Address: 0x0D, Reset: 0x04, Name: VENDOR_H

High byte of the vendor ID.

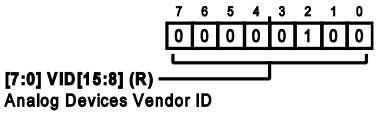


Table 27. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Analog Devices Vendor ID.	0x4	R

STREAM MODE REGISTER

Address: 0x0E, Reset: 0x00, Name: STREAM_MODE

Defines the length of the loop when streaming data.

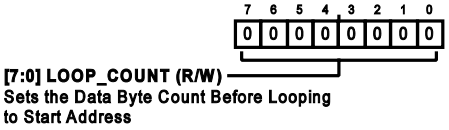


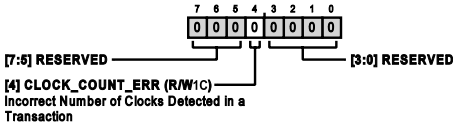
Table 28. Bit Descriptions for STREAM_MODE

Bits	Bit Name	Description	Reset	Access
[7:0]	LOOP_COUNT	Sets the data byte count before looping to start address. Not enabled in the ADAQ4216.	0x0	R/W

INTERFACE STATUS A REGISTER

Address: 0x11, Reset: 0x00, Name: INTERFACE_STATUS_A

Status bits are set to 1 to indicate an active condition. The status bits can be cleared by writing a 1 to the corresponding bit location.



REGISTER DETAILS

Table 29. Bit Descriptions for INTERFACE_STATUS_A

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	CLOCK_COUNT_ERR	0 = No error. 1 = Incorrect Number of Clocks Detected in a Transaction. Write 1 to clear.	0x0	R/W1C
[3:0]	RESERVED	Reserved.	0x0	R

EXIT CONFIGURATION MODE REGISTER

Address: 0x14, Reset: 0x00, Name: EXIT_CFG_MD

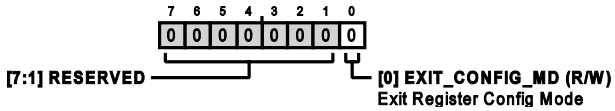


Table 30. Bit Descriptions for EXIT_CFG_MD

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	EXIT_CONFIG_MD	Exit Register Config Mode. Write 1 to exit register config mode. Self clearing upon $\overline{CS}$ = 1.	0x0	R/W

AVERAGING MODE REGISTER

Address: 0x15, Reset: 0x00, Name: AVG

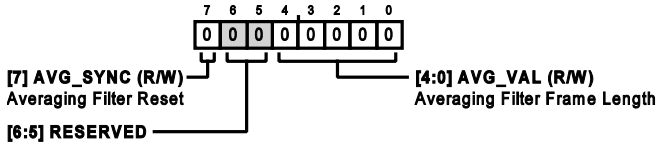
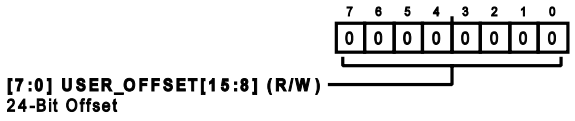


Table 31. Bit Descriptions for AVG

Bits	Bit Name	Description	Reset	Access
7	AVG_SYNC	Averaging Filter Reset. 1 = Reset, self clearing.	0x0	R/W
[6:5]	RESERVED	Reserved.	0x0	R
[4:0]	AVG_VAL	Averaging Filter Block Length, 2^N. 0x00 = No averaging. Use only 0x01 through 0x10 for averaging mode. 0x01 = 2^1 samples. 0x02 = 2^2 samples. 0x03 = 2^3 samples. 0x04 = 2^4 samples. 0x05 = 2^5 samples. … 0x0F = 2^{15} samples. 0x10 = 2^{16} samples. 0x11 through 0x1F = invalid.	0x0	R/W

OFFSET REGISTERS

Address: 0x17, Reset: 0x00, Name: OFFSET_MB



REGISTER DETAILS

Table 32. Bit Descriptions for OFFSET_LB

Bits	Bit Name	Description	Reset	Access
[7:0]	USER_OFFSET[7:0]	16-Bit Offset. Twos complement (signed). $1LSB = \frac{V_{REF}}{2^{15}} / GAIN.$	0x0	R/W

Address: 0x18, Reset: 0x00, Name: OFFSET_HB

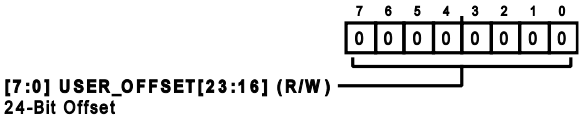


Table 33. Bit Descriptions for OFFSET_HB

Bits	Bit Name	Description	Reset	Access
[7:0]	USER_OFFSET[15:8]	16-Bit Offset. Twos complement (signed). $1LSB = \frac{V_{REF}}{2^{15}} / GAIN.$	0x0	R/W

GAIN REGISTERS

Address: 0x1C, Reset: 0x00, Name: GAIN_LB

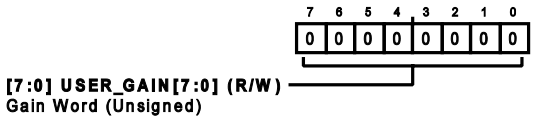


Table 34. Bit Descriptions for GAIN_LB

Bits	Bit Name	Description	Reset	Access
[7:0]	USER_GAIN[7:0]	Gain Word (Unsigned). Multiplier output = input × gain word/0x8000. Maximum effective gain = 0xFFFF/0x8000 = 1.99997.	0x0	R/W

Address: 0x1D, Reset: 0x80, Name: GAIN_HB

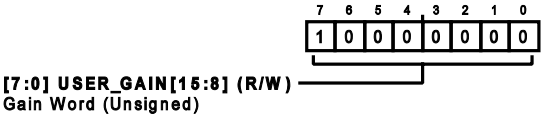
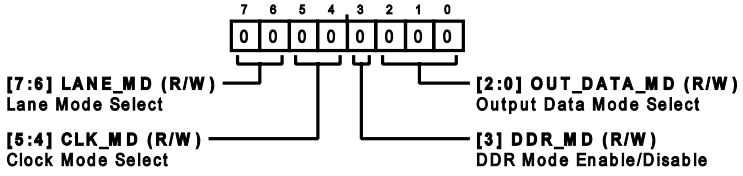


Table 35. Bit Descriptions for GAIN_HB

Bits	Bit Name	Description	Reset	Access
[7:0]	USER_GAIN[15:8]	Gain Word (Unsigned). Multiplier output = input × gain word/0x8000. Maximum effective gain = 0xFFFF/0x8000 = 1.99997.	0x80	R/W

MODES REGISTER

Address: 0x20, Reset: 0x00, Name: MODES



REGISTER DETAILS

Table 36. Bit Descriptions for MODES

Bits	Bit Name	Description	Reset	Access
[7:6]	LANE_MD	Lane Mode Select. 00 = One lane. 01 = Two lanes. 10 = Four lanes. 11 = Invalid setting.	0x0	R/W
[5:4]	CLK_MD	Clock Mode Select. 00 = SPI clocking mode. 01 = Echo clock mode. 10 = Host clock mode. 11 = Invalid setting.	0x0	R/W
3	DDR_MD	DDR Mode Enable/Disable. 0 = SDR. 1 = DDR (only valid for echo clock mode and host clock mode).	0x0	R/W
[2:0]	OUT_DATA_MD	Output Data Mode Select. 000 = 16-bit differential data. 001 = 16-bit differential data + 8-bit common-mode data. 010 = Unused. 011 = 30-bit averaged differential data + OR bit + SYNC bit. 100 = 32-bit test data pattern (TEST_DATA_PAT).	0x0	R/W

INTERNAL OSCILLATOR REGISTER

Address: 0x21, Reset: 0x00, Name: OSCILLATOR

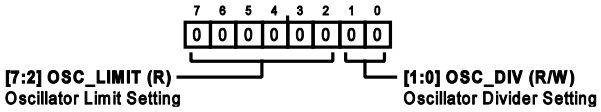


Table 37. Bit Descriptions for OSCILLATOR

Bits	Bit Name	Description	Reset	Access
[7:2]	OSC_LIMIT	Oscillator Limit Setting. Oscillator is limited to this number of clock pulses plus one. Automatically calculated by the ADAQ4216 based on the data word size, number of active SDO lanes, and data rate mode (SDR or DDR).	0x0	R
[1:0]	OSC_DIV	Oscillator Frequency Divider Setting. 00 = No divide (divide by 1). 01 = Divide by 2. 10 = Divide by 4. 11 = Invalid setting.	0x0	R/W

OUTPUT DRIVER REGISTER

Address: 0x22, Reset: 0x00, Name: IO

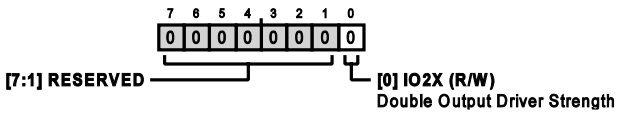


Table 38. Bit Descriptions for IO

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 38. Bit Descriptions for IO (Continued)

Bits	Bit Name	Description	Reset	Access
0	IO2X	Double Output Driver Strength. 1 = Double output driver strength. 0 = Normal output driver strength.	0x0	R/W

TEST PATTERN REGISTERS

Address: 0x23, Reset: 0x0F, Name: TEST_PAT_BYTE0

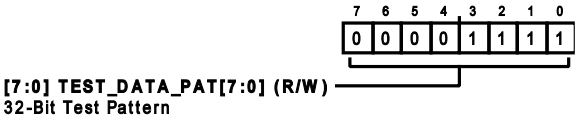


Table 39. Bit Descriptions for TEST_PAT_BYTE0

Bits	Bit Name	Description	Reset	Access
[7:0]	TEST_DATA_PAT[7:0]	32-Bit Test Pattern. Applied when OUT_DATA_MD = 4.	0xF	R/W

Address: 0x24, Reset: 0x0F, Name: TEST_PAT_BYTE1

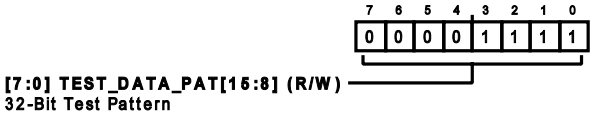


Table 40. Bit Descriptions for TEST_PAT_BYTE1

Bits	Bit Name	Description	Reset	Access
[7:0]	TEST_DATA_PAT[15:8]	32-Bit Test Pattern. Applied when OUT_DATA_MD = 4.	0xF	R/W

Address: 0x25, Reset: 0x5A, Name: TEST_PAT_BYTE2

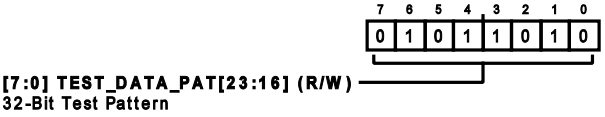


Table 41. Bit Descriptions for TEST_PAT_BYTE2

Bits	Bit Name	Description	Reset	Access
[7:0]	TEST_DATA_PAT[23:16]	32-Bit Test Pattern. Applied when OUT_DATA_MD = 4.	0x5A	R/W

Address: 0x26, Reset: 0x5A, Name: TEST_PAT_BYTE3

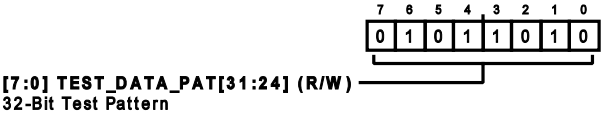


Table 42. Bit Descriptions for TEST_PAT_BYTE3

Bits	Bit Name	Description	Reset	Access
[7:0]	TEST_DATA_PAT[31:24]	32-Bit Test Pattern. Applied when OUT_DATA_MD = 4.	0x5A	R/W

REGISTER DETAILS

DIGITAL DIAGNOSTICS REGISTER

Address: 0x34, Reset: 0x40, Name: DIG_DIAG

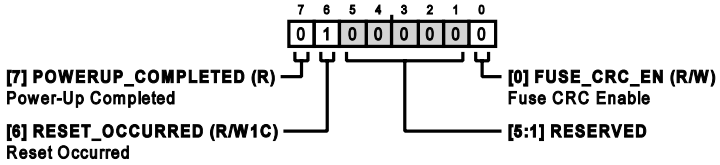


Table 43. Bit Descriptions for DIG_DIAG

Bits	Bit Name	Description	Reset	Access
7	POWERUP_COMPLETED	1 = Power-Up Completed. Self clearing.	0x0	R
6	RESET_OCCURRED	Reset Occurred. This bit is set to 1 upon a reset event. Write 1 to clear (useful for detecting brownouts).	0x1	R/W1C
[5:1]	RESERVED	Reserved.	0x0	R
0	FUSE_CRC_EN	Fuse CRC Enable. Write a 1 to force recheck of CRC.	0x0	R/W

DIGITAL ERRORS REGISTER

Address: 0x35, Reset: 0x00, Name: DIG_ERR

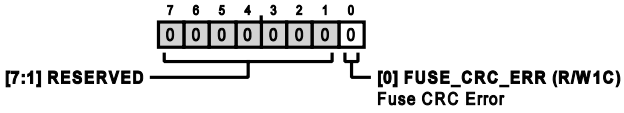


Table 44. Bit Descriptions for DIG_ERR

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	FUSE_CRC_ERR	Fuse CRC Error. This bit is set to 1 upon a fuse CRC error. Write 1 to clear.	0x0	R/W1C

OUTLINE DIMENSIONS

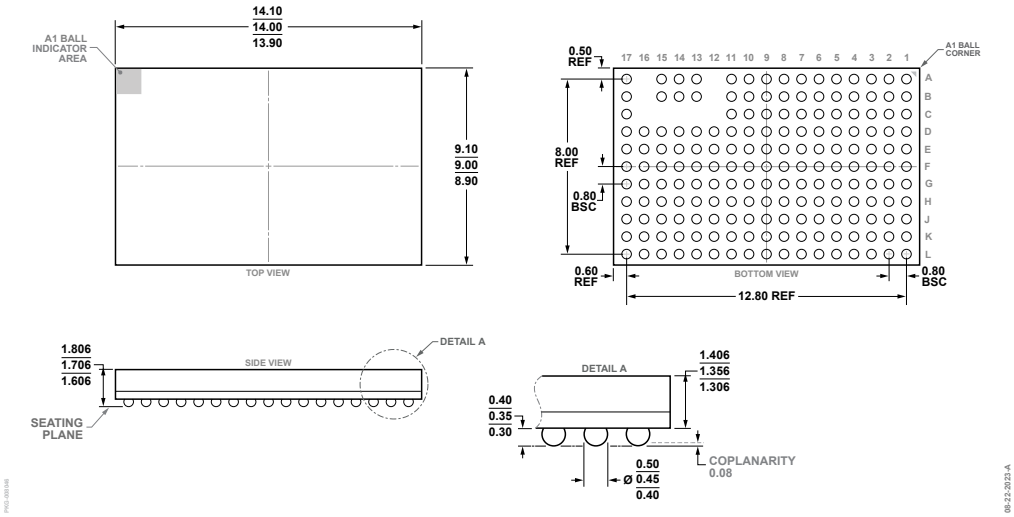


Figure 115. 178-Ball Chip-Scale Package, Ball Grid Array
(BC-178-2)
Dimensions Shown in millimeters

Updated: January 13, 2025

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADAQ4216BBCZ	−40°C to +105°C	178-Lead, BGA (14mm × 9mm × 0.8mm)	Tray, 0	BC-178-2

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Evaluation Board[1]	Description
EVAL-ADAQ4216-FMCZ	Evaluation Board

[1] Z = RoHS-Compliant Part.