

36 V, 18 MHz, Low Noise, Fast Settling Single Supply, RRO, JFET Op Amp

**FEATURES**

- ▶ Wide gain bandwidth product: 18 MHz typical
- ▶ High slew rate: 48 V/μs typical
- ▶ Low voltage noise density: 3.3 nV/√Hz typical at 1 kHz
- ▶ Low peak-to-peak noise: 0.15 μV p-p, 0.1 Hz to 10 Hz
- ▶ Low input bias current: ±15 pA typical at T<sub>A</sub> = 25°C
- ▶ Low offset voltage: ±80 μV maximum at T<sub>A</sub> = 25°C
- ▶ Offset voltage drift: ±1.2 μV/°C maximum at T<sub>A</sub> = -40°C to 85°C
- ▶ Fast settling: 0.01% in 700 ns typical
- ▶ Wide range of operating voltages
  - ▶ Dual-supply operation: ±2.5 V to ±18 V
  - ▶ Single-supply operation: 5 V to 36 V
- ▶ Input voltage range includes V-
- ▶ Rail-to-rail output
- ▶ High capacitive load drive capability
- ▶ Output short-circuit current: ±46 mA
- ▶ No phase reversal
- ▶ Unity-gain stable

**APPLICATIONS**

- ▶ PLL filter amplifiers
- ▶ Transimpedance amplifiers
- ▶ Photodiode sensor interfaces
- ▶ Low noise charge amplifiers

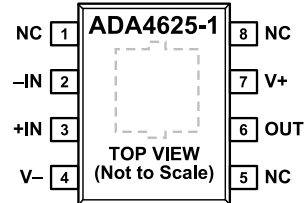
**GENERAL DESCRIPTION**

The ADA4625-1/ADA4625-2 build on Analog Devices, Inc., high voltage, single-supply, rail-to-rail output (RRO), precision junction field effect transistor (JFET) input op amps, taking that product type to a level of speed and low noise that has not been made available to the market previously.

The ADA4625-1/ADA4625-2 provide optimal performance in high voltage, high gain, and low noise applications. The input common-mode voltage range includes the negative supply, and the output swings rail to rail. This enables the user to maximize dynamic input range in low voltage, single supply applications without the need for a separate negative voltage power supply for ground sense.

The combination of wide bandwidth, low noise, and low input bias current makes the ADA4625-1/ADA4625-2 especially suitable for phase-locked loop (PLL), active filter amplifiers and for high tuning voltage (V<sub>TUNE</sub>), voltage controlled oscillators (VCOs) and preamplifiers where low level signals require an amplifier that provides both high amplification and wide bandwidth.

**PIN CONFIGURATION**



- NOTES**
1. NC = NO CONNECTION. DO NOT CONNECT TO THIS PIN.
  2. EXPOSED PAD. CONNECT THE EXPOSED PAD TO GND, V+ OR V- PLANE, OR LEAVE IT FLOATING.

Figure 1.

001

The ADA4625-1/ADA4625-2 are unity-gain stable, and there is no phase reversal when input range exceeds either supply rail by 200 mV. The output is capable of driving loads up to 1000 pF and/or 600 Ω loads.

The ADA4625-1/ADA4625-2 are specified for operation over the extended industrial temperature range of -40°C to +125°C and operates from +5 V to +36 V (±2.5 V to ±18 V) with specifications at +5 V and ±18 V. The devices are available in an 8-lead SOIC package with an exposed pad (EPAD).

Table 1. Related Precision JFET Operational Amplifiers

Single	Dual	Quad
Not applicable	AD823A	Not applicable
AD8510	AD8512	AD8513
AD8610	AD8620	Not applicable
ADA4610-1	ADA4610-2	ADA4610-4
ADA4622-1	ADA4622-2	ADA4622-4
ADA4627-1/ADA4637-1	Not applicable	Not applicable

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**REVISION HISTORY****2/2025—Rev. A to Rev. B**

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## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—±18 V OPERATION

Supply voltage ( $V_{SY}$ ) = ±18 V, common-mode voltage ( $V_{CM}$ ) = output voltage ( $V_{OUT}$ ) = 0 V,  $T_A$  = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$	ADA4625-1		±15	±80	μV
		ADA4625-2			±100	μV
		-40°C < $T_A$ < +125°C			±250	μV
Offset Voltage Drift	$TCV_{OS}$	-40°C < $T_A$ < +85°C		±0.2	±1.2	μV/°C
		-40°C < $T_A$ < +125°C		±0.5	±2.1	μV/°C
Input Bias Current	$I_B$	ADA4625-1, -40°C < $T_A$ < +125°C		±15	±75	pA
		ADA4625-2, -40°C < $T_A$ < +125°C			±5.5	nA
Input Offset Current	$I_{OS}$	ADA4625-1, -40°C < $T_A$ < +125°C			±7	nA
		ADA4625-2, -40°C < $T_A$ < +125°C		±2	±50	pA
		ADA4625-1, -40°C < $T_A$ < +125°C				±0.4
Input Voltage Range	IVR	ADA4625-2, -40°C < $T_A$ < +125°C			±0.7	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM}$ = -18.2 V to +14.5 V	-18.2		+14.5	V
		-40°C < $T_A$ < +125°C	97	115		dB
		$V_{CM}$ = -18.2 V to +12 V	94			dB
		-40°C < $T_A$ < +125°C	115	130		dB
Large Signal Voltage Gain	$A_{VO}$	Load resistance ( $R_L$ ) = 2 kΩ, $V_{OUT}$ = -17.5 V to +17.5 V	110			dB
		-40°C < $T_A$ < +125°C	140	150		dB
		$R_L$ = 600 Ω, $V_{OUT}$ = -15 V to +15 V	135			dB
		-40°C < $T_A$ < +125°C	130	135		dB
		ADA4625-1, -40°C < $T_A$ < +125°C	115			dB
		ADA4625-2, -40°C < $T_A$ < +125°C	100			dB
Input Capacitance	$C_{DM}$	Differential Mode		8.6		pF
		ADA4625-2		13.8		pF
Common Mode	$C_{CM}$	ADA4625-1		11.3		pF
		ADA4625-2		13.3		pF
Input Resistance	$R_{DM}$	Differential mode		$10^{12}$		Ω
	$R_{CM}$	Common mode, $V_{CM}$ from -18 V to +12 V		$10^{12}$		Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$R_L$ = 2 kΩ	17.65	17.72		V
		-40°C < $T_A$ < +125°C	17.5			V
		$R_L$ = 600 Ω	17.0	17.28		V
		-40°C < $T_A$ < +125°C	16.75			V
Output Voltage Low	$V_{OL}$	$R_L$ = 2 kΩ		-17.74	-17.70	V
		-40°C < $T_A$ < +125°C			-17.5	V
		$R_L$ = 600 Ω		-17.4	-17.0	V
		-40°C < $T_A$ < +125°C			-16.85	V
Output Current	$I_{OUT}$	Dropout voltage ( $V_{DROPOUT}$ ) < 1 V		±33		mA
Short-Circuit Current	$I_{SC}$			±46		mA
Closed-Loop Output Impedance	$Z_{OUT}$	f = 1 MHz, closed-loop gain ( $A_V$ ) = +1		2		Ω
		$A_V$ = +10		18		Ω
		$A_V$ = +100		29		Ω

## SPECIFICATIONS

Table 2. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 5 \text{ V to } \pm 18 \text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	105	120		dB
Supply Current per Amplifier	$I_{SY}$	$V_{OUT} = 0 \text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		4.0	4.5	mA
					5	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$V_{OUT} = \pm 10 \text{ V}$ , $R_L = 2 \text{ k}\Omega$ , $A_V = -1$ $V_{OUT} = \pm 10 \text{ V}$ , $R_L = 2 \text{ k}\Omega$ , $A_V = -5$		48		V/ $\mu\text{s}$
Gain Bandwidth Product	GBP	$A_V = 100$		18		MHz
Unity-Gain Crossover	UGC	$A_V = 1$		12.4		MHz
-3 dB Bandwidth	-3 dB	$A_V = 1$		16		MHz
Phase Margin	$\Phi_M$	ADA4625-1		88		Degrees
		ADA4625-2		75		Degrees
Channel Separation	CS	$V_{IN} = 15 \text{ V p-p}$ , $f = 1 \text{ kHz}$ , $R_L = 2 \text{ k}\Omega$ , $A_V = 100$ $V_{IN} = 15 \text{ V p-p}$ , $f = 10 \text{ kHz}$ , $R_L = 2 \text{ k}\Omega$ , $A_V = 100$		108		dB
Settling Time	$t_s$			88		dB
ADA4625-1		To 0.1%, input voltage ( $V_{IN}$ ) = 10 V step, $R_L = 2 \text{ k}\Omega$ , load capacitance ( $C_L$ ) = 15 pF, $A_V = -1$		500		ns
		To 0.01%, $V_{IN} = 10 \text{ V step}$ , $R_L = 2 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , $A_V = -1$		700		ns
ADA4625-2		To 0.1%, $V_{IN} = 10 \text{ V step}$ , $R_L = 2 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , $A_V = -1$		700		ns
		To 0.01%, $V_{IN} = 10 \text{ V step}$ , $R_L = 2 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$ , $A_V = -1$		1200		ns
<b>ELECTROMAGNETIC INTERFERENCE (EMI) REJECTION RATIO</b>						
$f = 1000 \text{ MHz}$	EMIRR	ADA4625-1/ADA4625-2		56		dB
$f = 2400 \text{ MHz}$		ADA4625-1		93		dB
		ADA4625-2		73		dB
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_N$ p-p	0.1 Hz to 10 Hz		0.15		$\mu\text{V p-p}$
Voltage Noise Density	$e_N$	$f = 10 \text{ Hz}$		5.5		nV/ $\sqrt{\text{Hz}}$
		$f = 100 \text{ Hz}$		3.6		nV/ $\sqrt{\text{Hz}}$
		$f = 1 \text{ kHz}$		3.3		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_N$	$f = 1 \text{ kHz}$		4.5		fA/ $\sqrt{\text{Hz}}$
Total Harmonic Distortion + Noise	THD + N	$A_V = 1$ , $f = 10 \text{ Hz to } 20 \text{ kHz}$ , $R_L = 2 \text{ k}\Omega$ , $V_{IN} = 6 \text{ V}_{RMS}$ at 1 kHz				
Bandwidth = 80 kHz				0.0003		%
				-109		dB
Bandwidth = 500 kHz				0.0007		%
				-103		dB



## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—5 V OPERATION

$V_{SY} = 5\text{ V}$ ,  $V_{CM} = 1.5\text{ V}$ ,  $V_{OUT} = V_{SY}/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		$\pm 0.1$	$\pm 0.6$	mV
Offset Voltage Drift	$TCV_{OS}$	ADA4625-1, $-40^\circ\text{C} < T_A < +85^\circ\text{C}$		$\pm 0.4$	$\pm 1.0$	mV
		ADA4625-2, $-40^\circ\text{C} < T_A < +85^\circ\text{C}$			$\pm 2.6$	$\mu\text{V}/^\circ\text{C}$
		ADA4625-1, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		$\pm 0.7$	$\pm 3.6$	$\mu\text{V}/^\circ\text{C}$
		ADA4625-2, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			$\pm 4.5$	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	ADA4625-1, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		$\pm 15$	$\pm 50$	pA
		ADA4625-2, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			$\pm 3.5$	nA
Input Offset Current	$I_{OS}$	ADA4625-1, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		$\pm 2$	$\pm 50$	pA
		ADA4625-2, $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			$\pm 150$	pA
Input Voltage Range	IVR		-0.2		+1.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 1.5\text{ V}$	74	90		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	70			dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ to $V^-$ , $V_{OUT} = 0.35\text{ V to } 4.65\text{ V}$	130	145		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120			dB
		$R_L = 600\ \Omega$ to $V^-$ , $V_{OUT} = 0.5\text{ V to } 4.5\text{ V}$	120	130		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	110			dB
Input Capacitance	$C_{DM}$	ADA4625-1		12.1		pF
		ADA4625-2		12.7		pF
Common Mode	$C_{CM}$	ADA4625-1		16.3		pF
		ADA4625-2		18.4		pF
Input Resistance	$R_{DM}$	Differential mode		$10^{12}$		$\Omega$
	$R_{CM}$	Common mode, $V_{CM}$ from 0 V to 1.5 V		$10^{12}$		$\Omega$
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$R_L = 2\text{ k}\Omega$ to $V^-$	4.75	4.82		V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.7			V
		$R_L = 600\ \Omega$ to $V^-$	4.65	4.74		V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.55			V
Output Voltage Low	$V_{OL}$	$R_L = 2\text{ k}\Omega$ to $V^+$		0.17	0.22	V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			0.3	V
		$R_L = 600\ \Omega$ to $V^+$		0.25	0.3	V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			0.45	V
Output Current	$I_{OUT}$	$V_{DROPOUT} < 1\text{ V}$		$\pm 33$		mA
Short-Circuit Current	$I_{SC}$			$\pm 46$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = +1$		2		$\Omega$
		$A_V = +10$		18		$\Omega$
		$A_V = +100$		29		$\Omega$
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 4.5\text{ V to } 10\text{ V}$	80	97		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	75			dB
Supply Current per Amplifier	$I_{SY}$	$V_{OUT} = 0\text{ V}$		3.9	4.3	mA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			4.8	mA

## SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit	
<b>DYNAMIC PERFORMANCE</b>							
Slew Rate	SR	$V_{OUT} = 0.5 \text{ V to } 4.5 \text{ V}, R_L = 2 \text{ k}\Omega, A_V = -1$		32		V/ $\mu$ s	
		$V_{OUT} = 0.5 \text{ V to } 4.5 \text{ V}, R_L = 2 \text{ k}\Omega, A_V = -5$		27		V/ $\mu$ s	
Gain Bandwidth Product	GBP	$A_V = 100$		16		MHz	
Unity-Gain Crossover	UGC	$A_V = 1$		11.2		MHz	
-3 dB Bandwidth	-3 dB	$A_V = 1$		16		MHz	
Phase Margin	$\Phi_M$	ADA4625-1		86		Degrees	
		ADA4625-2		71		Degrees	
Channel Separation	CS	$V_{IN} = 15 \text{ V p-p}, f = 1 \text{ kHz}, R_L = 2 \text{ k}\Omega, A_V = 100$		108		dB	
		$V_{IN} = 15 \text{ V p-p}, f = 100 \text{ kHz}, R_L = 2 \text{ k}\Omega, A_V = 100$		88		dB	
Settling Time	$t_s$	To 0.1%, $V_{IN} = 4 \text{ V step}, R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}, A_V = -1$		600		ns	
		To 0.01%, $V_{IN} = 4 \text{ V step}, R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}, A_V = -1$		950		ns	
		To 0.1%, $V_{IN} = 4 \text{ V step}, R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}, A_V = -1$		1250		ns	
		To 0.01%, $V_{IN} = 4 \text{ V step}, R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}, A_V = -1$		1350		ns	
<b>EMI REJECTION RATIO</b>							
f = 1000 MHz	EMIRR	ADA4625-1/ADA4625-2		56		dB	
f = 2400 MHz		ADA4625-1		87		dB	
		ADA4625-2		79		dB	
<b>NOISE PERFORMANCE</b>							
Peak-to-Peak Noise	$e_N \text{ p-p}$	0.1 Hz to 10 Hz		0.15		$\mu$ V p-p	
Voltage Noise Density	$e_N$	f = 10 Hz		5.5		nV/ $\sqrt{\text{Hz}}$	
		f = 100 Hz		3.6		nV/ $\sqrt{\text{Hz}}$	
		f = 1 kHz		3.3		nV/ $\sqrt{\text{Hz}}$	
Current Noise Density	$i_N$	f = 1 kHz		4.5		fA/ $\sqrt{\text{Hz}}$	
Total Harmonic Distortion + Noise	THD + N	$A_V = 1, f = 10 \text{ Hz to } 20 \text{ kHz}, R_L = 2 \text{ k}\Omega, V_{IN} = 0.6 V_{RMS} \text{ at } 1 \text{ kHz}$	ADA4625-1	0.0003		%	
				-109		dB	
			ADA4625-2	0.002		%	
				-93		dB	
			Bandwidth = 80 kHz	ADA4625-1	0.0007		%
				-103		dB	
Bandwidth = 500 kHz			ADA4625-1	0.004		%	
			ADA4625-2	-89		dB	

## ABSOLUTE MAXIMUM RATINGS

**Table 4.**

Parameter	Rating
Supply Voltage	40 V
Input Voltage	(V-) - 0.2 V to (V+) + 0.2 V
Differential Input Voltage	(V-) - 0.2 V to (V+) + 0.2 V
Input Current <sup>1</sup>	±20 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C
Electrostatic Discharge (ESD)	
Human Body Model (HBM) <sup>2</sup>	
ADA4625-1	1.25 kV
ADA4625-2	1.5 kV
Field Induced Charge Device Model (FICDM) <sup>3</sup>	
ADA4625-1	1.25 kV
ADA4625-2	1.25 kV

<sup>1</sup> The input pins have clamp diodes connected to the power supply pins. Limit the input current to 20 mA or less whenever input signals exceed the power supply rail by 0.3 V.

<sup>2</sup> ESDA/JEDEC JS-001-2011 applicable standard.

<sup>3</sup> JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

**Table 5. Thermal Resistance**

Package Type <sup>1, 2</sup>	$\theta_{JA}$ <sup>3</sup>	$\theta_{JC}$	Unit
RD-8-4	52.8	5.7	°C/W

<sup>1</sup> Values were obtained per JEDEC standard JESD-51.

<sup>2</sup> Although the exposed pad can be left floating, it must be connected to the GND, or the V+ or V- plane for proper thermal management.

<sup>3</sup> Board layout impacts thermal characteristics such as  $\theta_{JA}$ . When proper thermal management techniques are used, a better  $\theta_{JA}$  can be achieved. Refer to the [Thermal Management](#) section for additional information.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS**

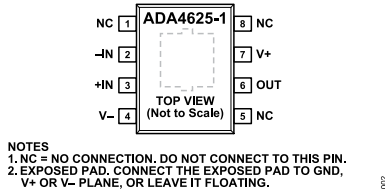


Figure 2. ADA4625-1 Pin Configuration

Table 6. Pin Function Descriptions, ADA4625-1

Pin No.	Mnemonic	Description
1, 5, 8	NC	No Connection. Do not connect to these pins.
2	-IN	Inverting Input Pin.
3	+IN	Noninverting Input Pin.
4	V-	Negative Supply Voltage Pin.
6	OUT	Output Pin.
7	V+	Positive Supply Voltage Pin.
	EPAD	Exposed Pad. Connect the exposed pad to GND, V+ or V- plane, or leave it floating.

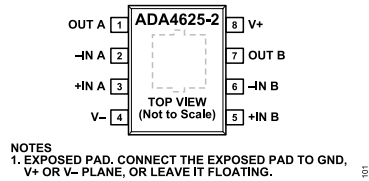


Figure 3. ADA4625-2 Pin Configuration

Table 7. Pin Function Descriptions, ADA4625-2

Pin No.	Mnemonic	Description
1	OUT A	Output Pin for Channel A.
2	-IN A	Inverting Input Pin for Channel A.
3	+IN A	Noninverting Input Pin for Channel A.
4	V-	Negative Supply Voltage Pin.
5	+IN B	Noninverting Input Pin for Channel B.
6	-IN B	Inverting Input Pin for Channel B.
7	OUT B	Output Pin for Channel B.
8	V+	Positive Supply Voltage Pin.
	EPAD	Exposed Pad. Connect the exposed pad to GND, V+ or V- plane, or leave it floating.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{CM} = 0\text{ V}$ , unless otherwise noted.

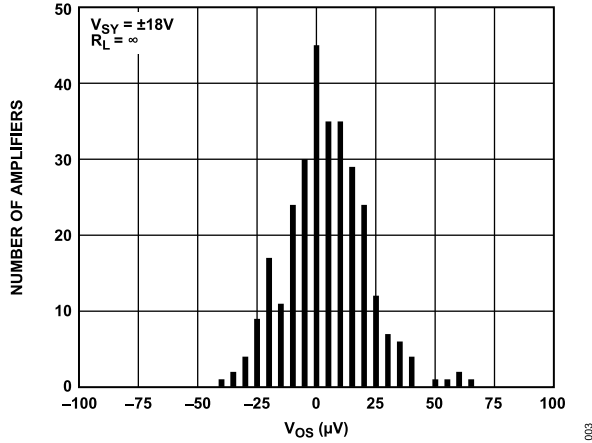


Figure 4. Input Offset Voltage ( $V_{OS}$ ) Distribution, Supply Voltage ( $V_{SY}$ ) =  $\pm 18\text{ V}$

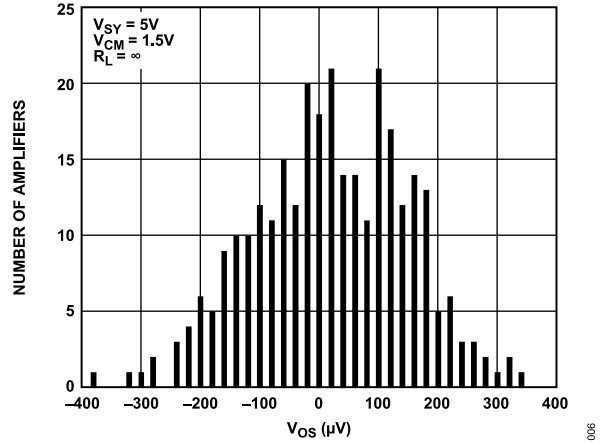


Figure 7.  $V_{OS}$  Distribution,  $V_{SY} = 5\text{ V}$

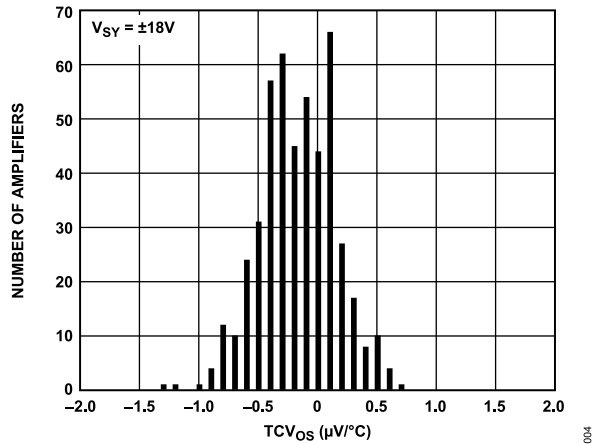


Figure 5. Input Offset Voltage Drift ( $TCV_{OS}$ ) Distribution ( $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{SY} = \pm 18\text{ V}$

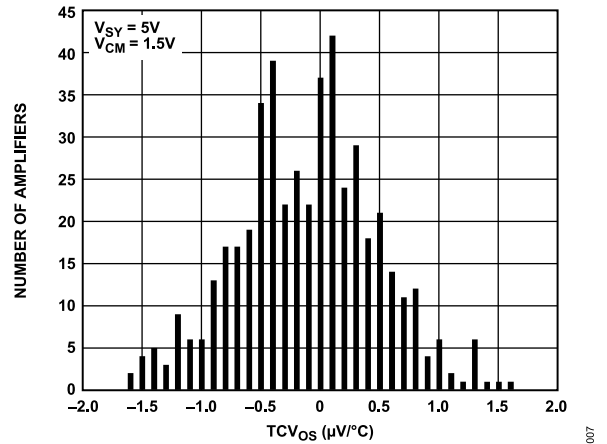


Figure 8.  $TCV_{OS}$  Distribution ( $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{SY} = 5\text{ V}$

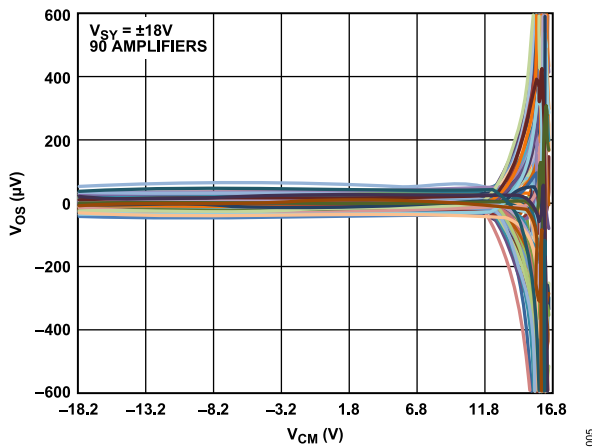


Figure 6.  $V_{OS}$  vs. Common-Mode Voltage ( $V_{CM}$ ),  $V_{SY} = \pm 18\text{ V}$

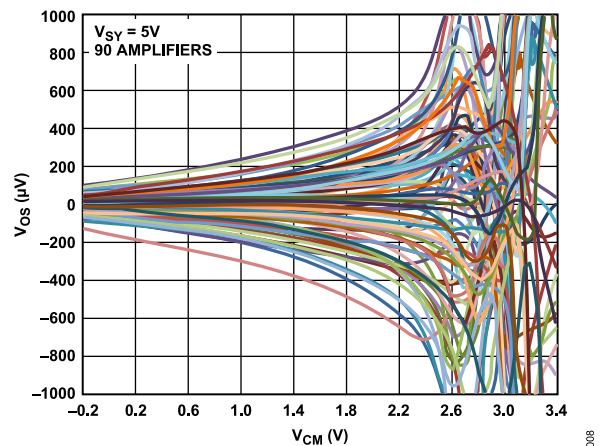


Figure 9.  $V_{OS}$  vs.  $V_{CM}$ ,  $V_{SY} = 5\text{ V}$

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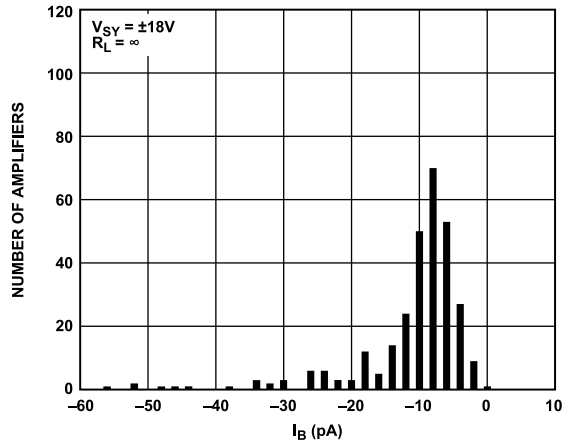


Figure 10. Input Bias Current ( $I_B$ ) Distribution,  $V_{SY} = \pm 18 V$

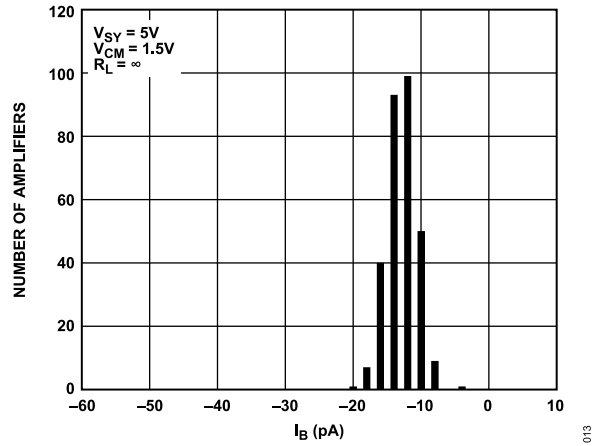


Figure 13.  $I_B$  Distribution,  $V_{SY} = 5 V$

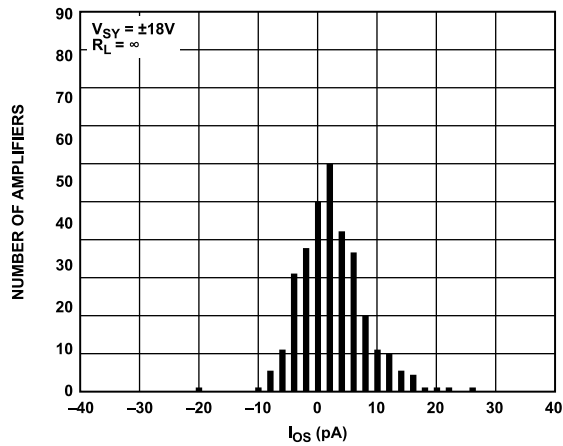


Figure 11. Input Offset Current ( $I_{OS}$ ) Distribution,  $V_{SY} = \pm 18 V$

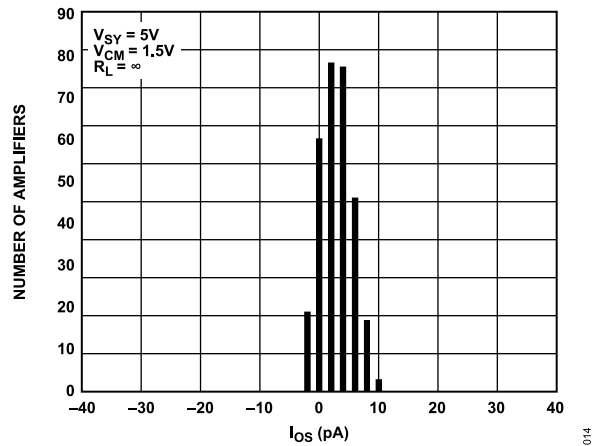


Figure 14.  $I_{OS}$  Distribution,  $V_{SY} = 5 V$

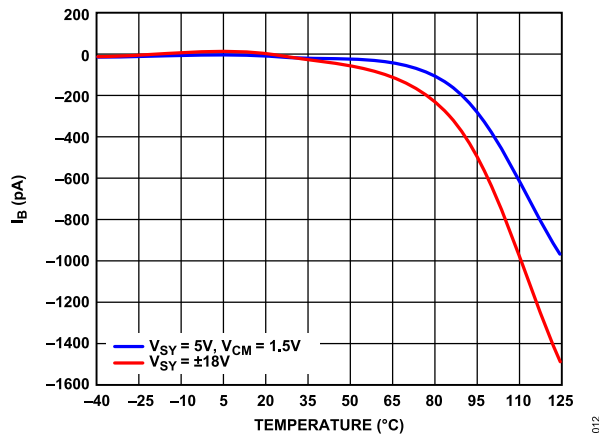


Figure 12. ADA4625-1  $I_B$  vs. Temperature

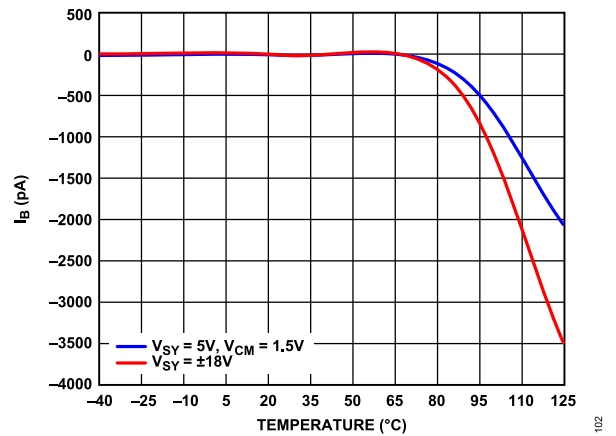


Figure 15. ADA4625-2  $I_B$  vs. Temperature

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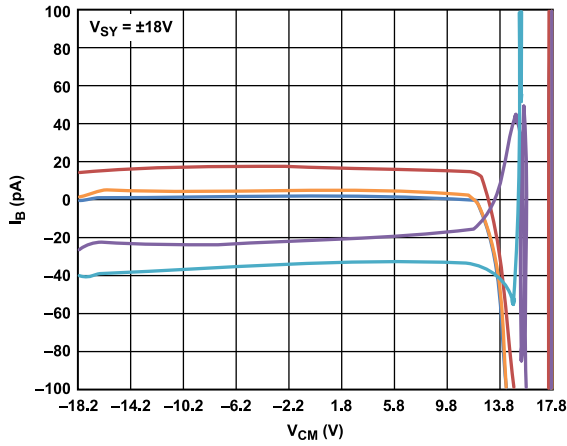


Figure 16.  $I_B$  vs.  $V_{CM}$ ,  $V_{SY} = \pm 18 V$

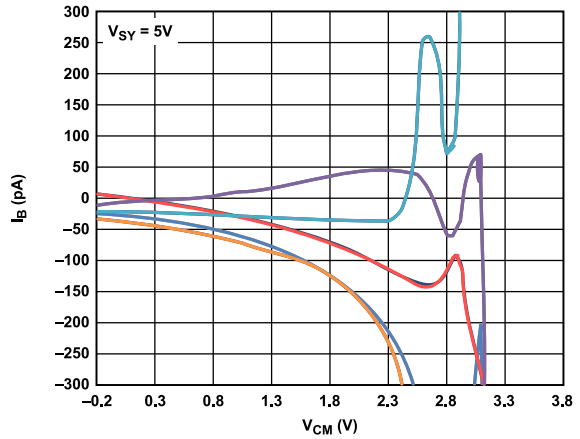


Figure 19.  $I_B$  vs.  $V_{CM}$ ,  $V_{SY} = 5 V$

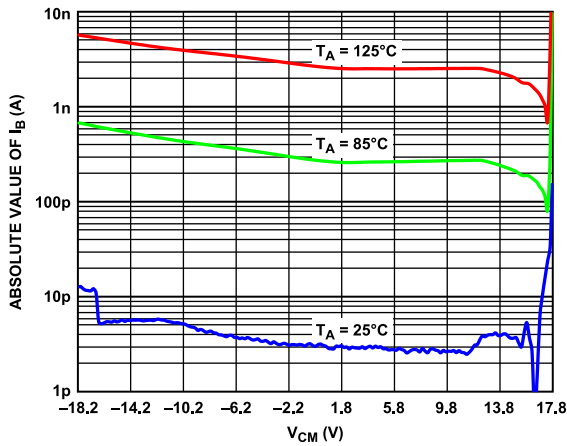


Figure 17. Absolute Value of  $I_B$  vs.  $V_{CM}$  for Various Temperatures,  $V_{SY} = \pm 18 V$

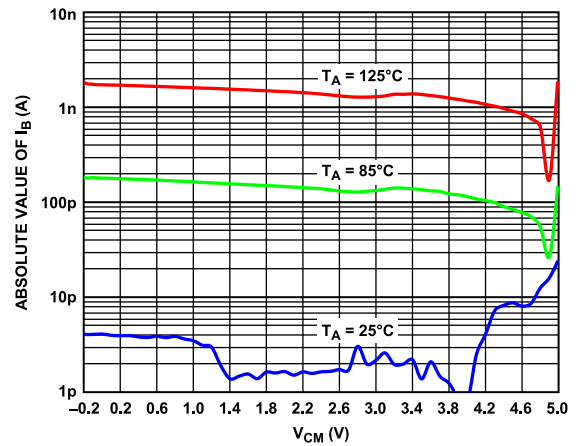


Figure 20. Absolute Value of  $I_B$  vs.  $V_{CM}$  for Various Temperature,  $V_{SY} = 5 V$

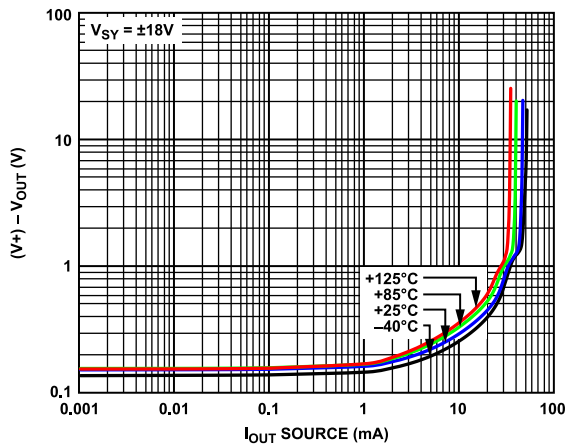


Figure 18. Dropout Voltage  $(V^+ - V_{OUT})$  vs. Output Current  $(I_{OUT})$  Source for Various Temperatures,  $V_{SY} = \pm 18 V$

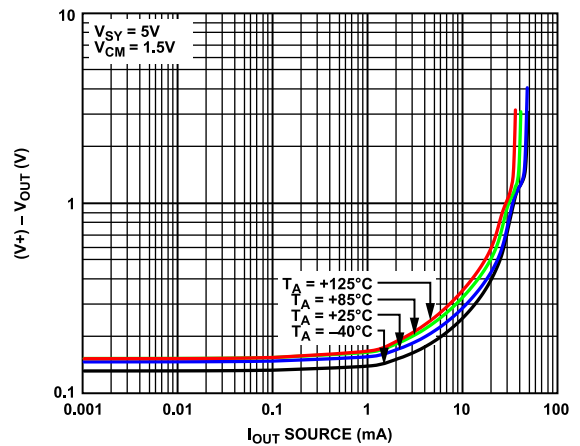


Figure 21.  $(V^+ - V_{OUT})$  vs.  $I_{OUT}$  Source for Various Temperatures,  $V_{SY} = 5 V$

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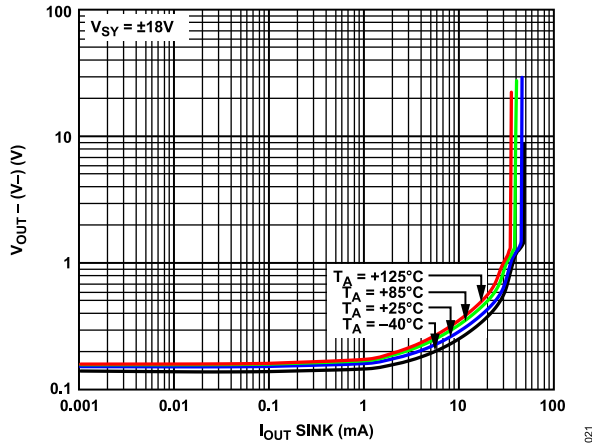


Figure 22. Dropout Voltage ( $V_{OUT} - (V-)$ ) vs.  $I_{OUT}$  Sink for Various Temperatures,  $V_{SY} = \pm 18\text{ V}$

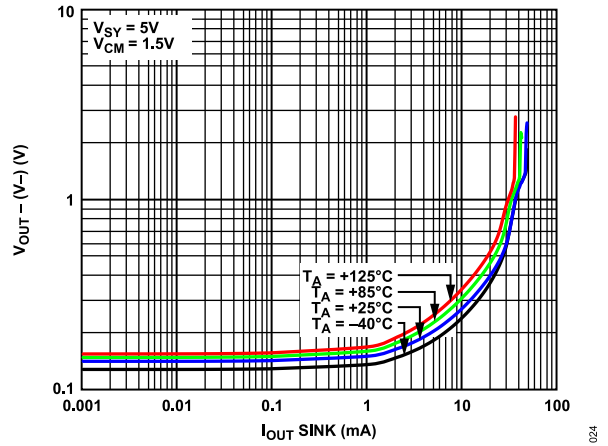


Figure 25. ( $V_{OUT} - (V-)$ ) vs.  $I_{OUT}$  Sink for Various Temperatures,  $V_{SY} = 5\text{ V}$

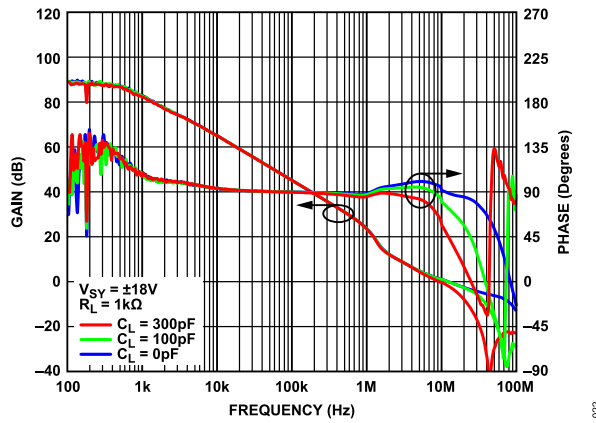


Figure 23. ADA4625-1 Open-Loop Gain and Phase vs. Frequency,  $V_{SY} = \pm 18\text{ V}$

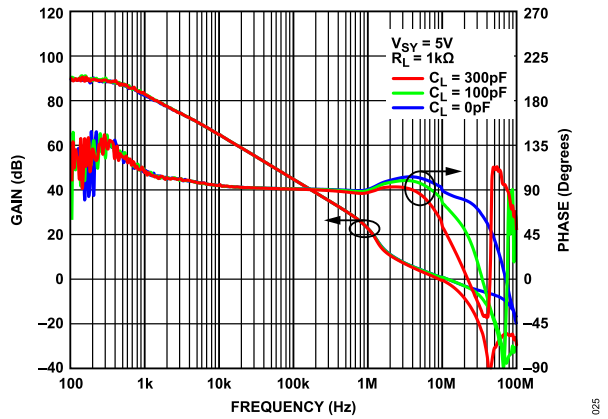


Figure 26. ADA4625-1 Open-Loop Gain and Phase vs. Frequency,  $V_{SY} = 5\text{ V}$

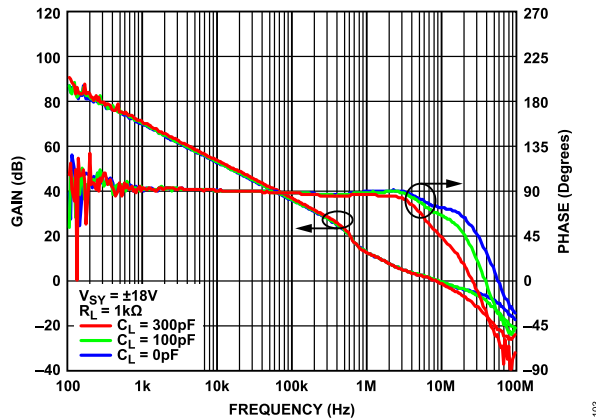


Figure 24. ADA4625-2 Open-Loop Gain and Phase vs. Frequency,  $V_{SY} = \pm 18\text{ V}$

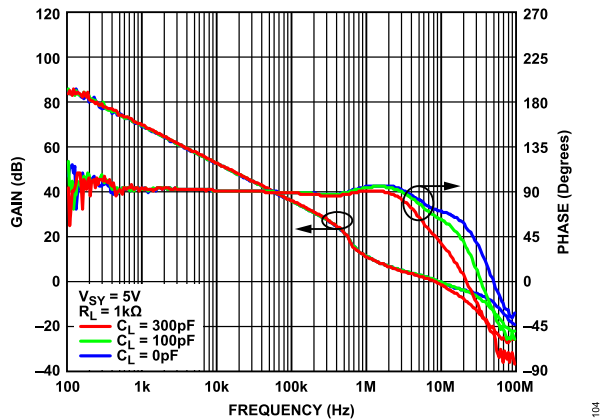


Figure 27. ADA4625-2 Open-Loop Gain and Phase vs. Frequency,  $V_{SY} = 5\text{ V}$



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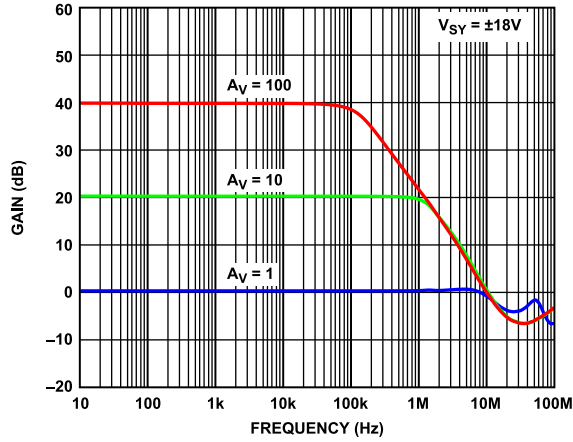


Figure 28. Gain vs. Frequency for Various Closed-Loop Gains,  $V_{SY} = \pm 18\text{ V}$

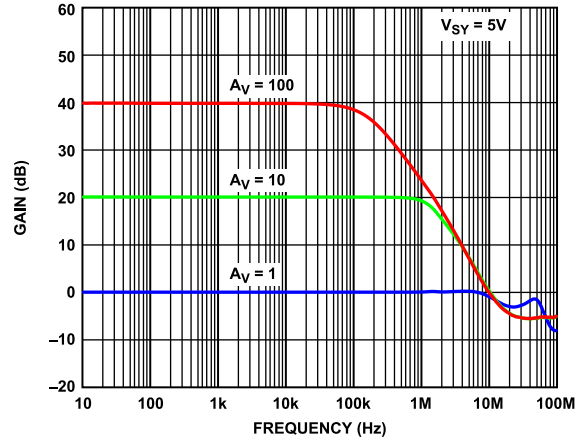


Figure 31. Gain vs. Frequency for Various Closed-Loop Gains,  $V_{SY} = 5\text{ V}$

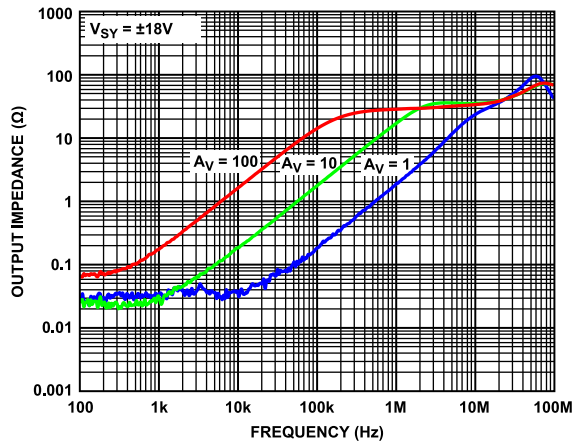


Figure 29. Output Impedance ( $Z_{OUT}$ ) vs. Frequency,  $V_{SY} = \pm 18\text{ V}$

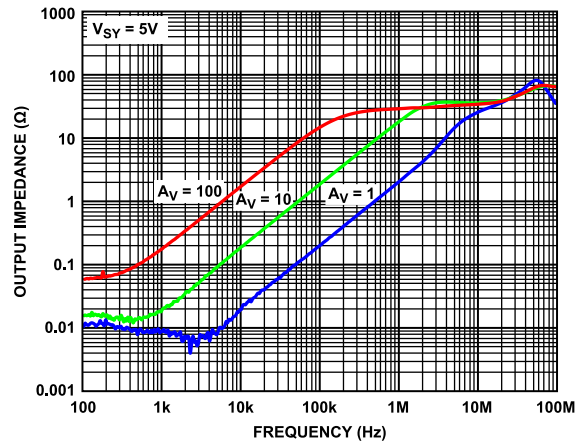


Figure 32.  $Z_{OUT}$  vs. Frequency,  $V_{SY} = 5\text{ V}$

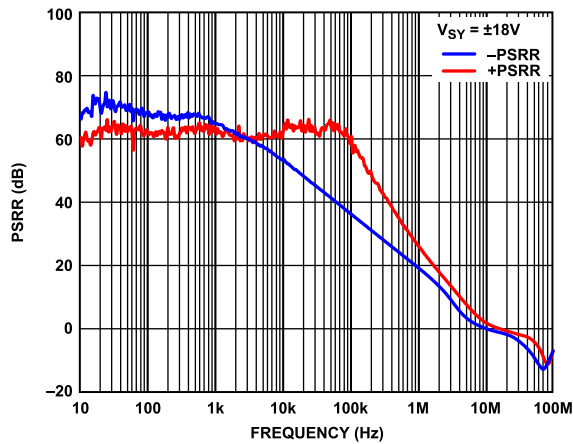


Figure 30. Power Supply Rejection Ratio (PSRR) vs. Frequency,  $V_{SY} = \pm 18\text{ V}$

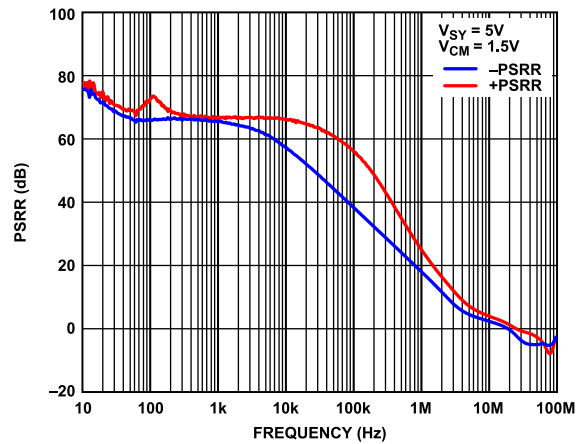


Figure 33. PSRR vs. Frequency,  $V_{SY} = 5\text{ V}$

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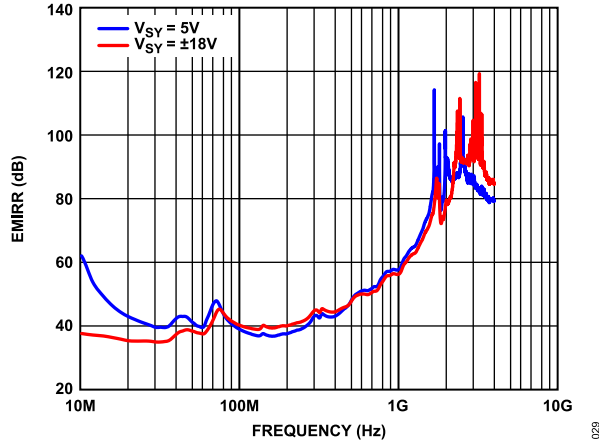


Figure 34. ADA4625-1 EMI Rejection Ratio (EMIRR) vs. Frequency

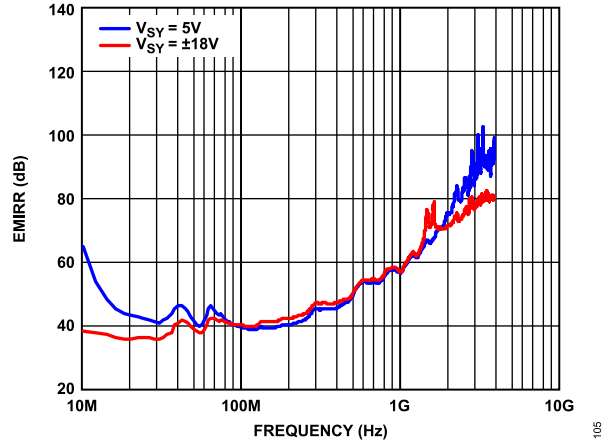


Figure 37. ADA4625-2 EMIRR vs. Frequency

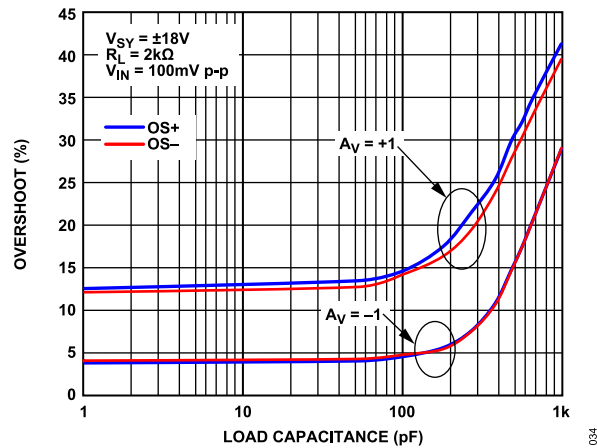


Figure 35. ADA4625-1 Small Signal Overshoot (OS±) vs. Load Capacitance,  $V_{SY} = \pm 18 V$

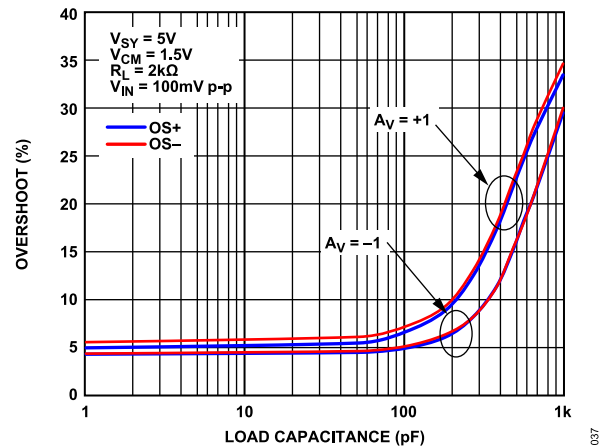


Figure 38. ADA4625-1 OS± vs. Load Capacitance,  $V_{SY} = 5 V$

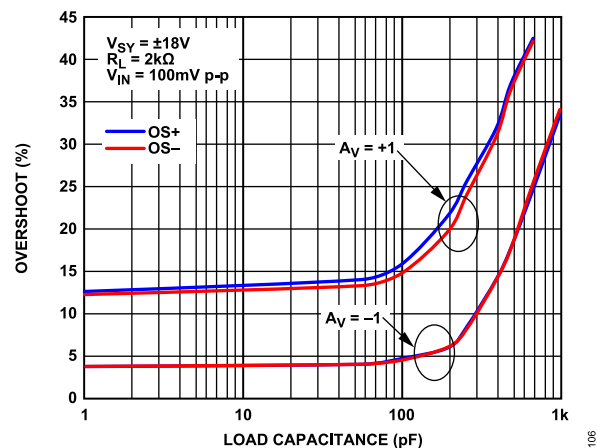


Figure 36. ADA4625-2 OS± vs. Load Capacitance,  $V_{SY} = \pm 18 V$

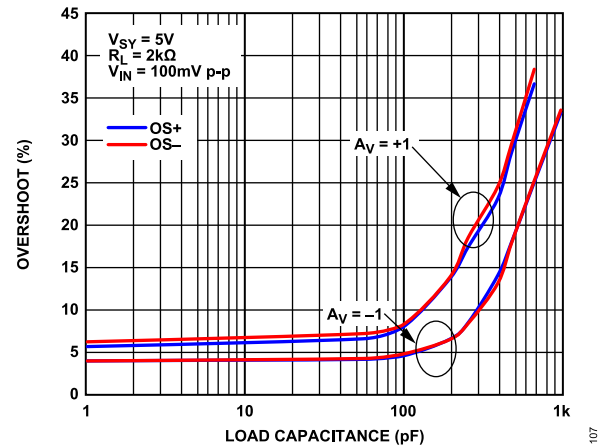


Figure 39. ADA4625-2 OS± vs. Load Capacitance,  $V_{SY} = 5 V$

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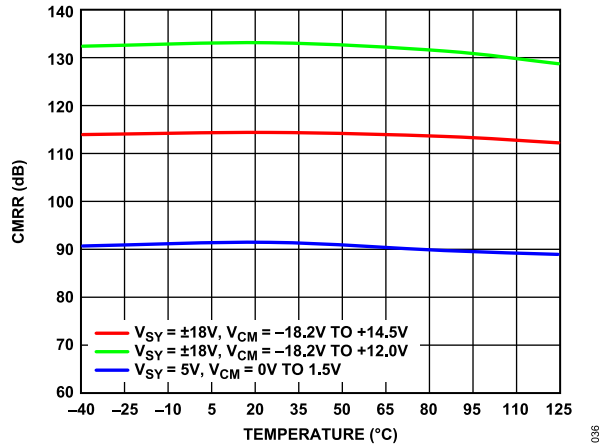


Figure 40. CMRR vs. Temperature

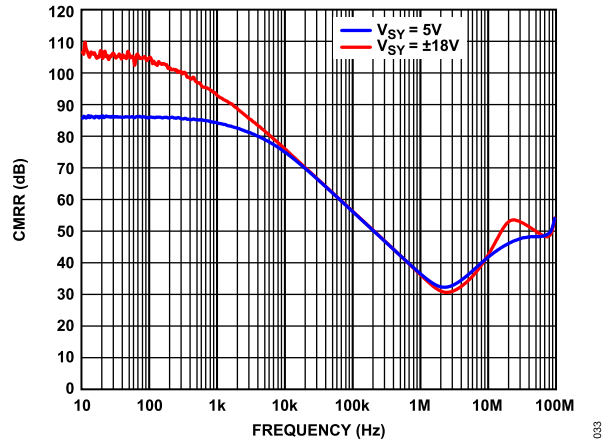


Figure 43. CMRR vs. Frequency

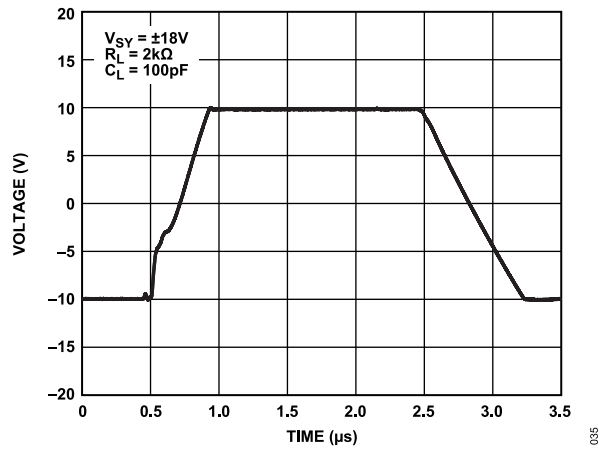


Figure 41. Large Signal Transient Response,  $A_V = +1$ ,  $V_{SY} = \pm 18$  V

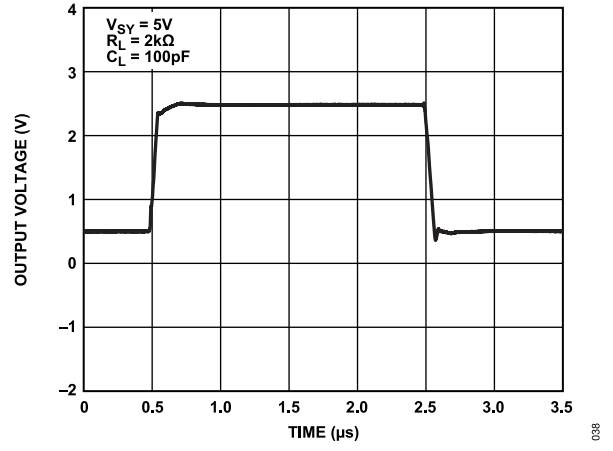


Figure 44. Large Signal Transient Response,  $A_V = +1$ ,  $V_{SY} = 5$  V

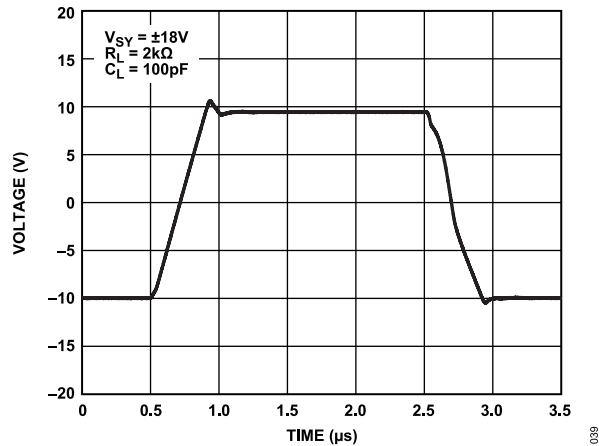


Figure 42. Large Signal Transient Response,  $A_V = -1$ ,  $V_{SY} = \pm 18$  V

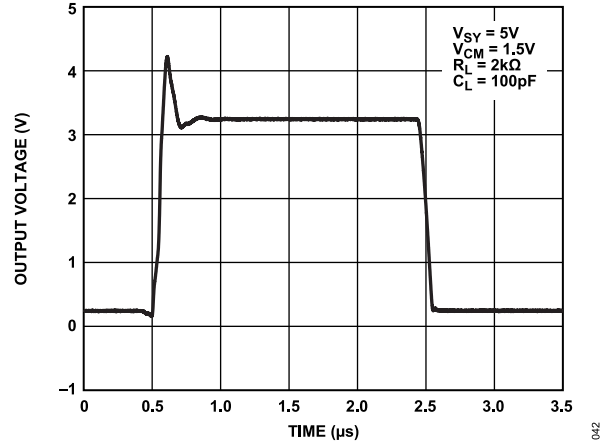


Figure 45. Large Signal Transient Response,  $A_V = -1$ ,  $V_{SY} = 5$  V

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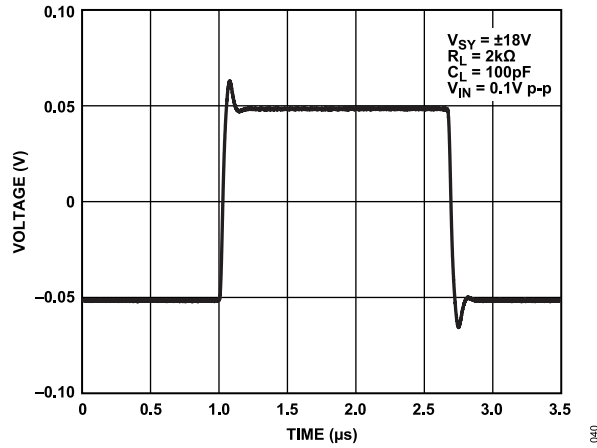


Figure 46. Small Signal Transient Response,  $A_V = 1$ ,  $V_{SY} = \pm 18 V$

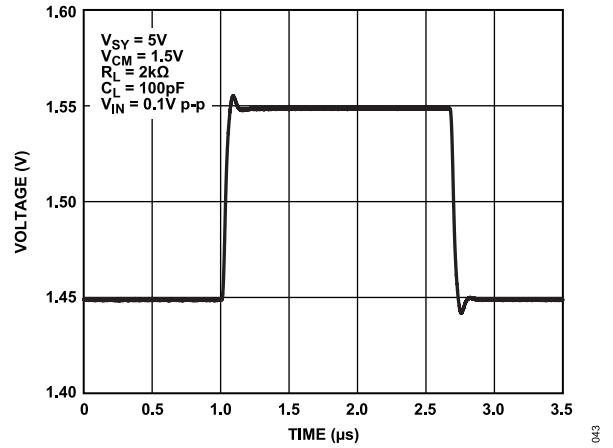


Figure 49. Small Signal Transient Response,  $A_V = 1$ ,  $V_{SY} = 5 V$

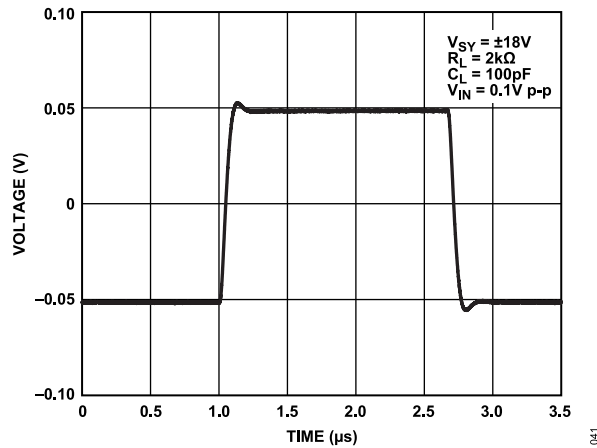


Figure 47. Small Signal Transient Response,  $A_V = -1$ ,  $V_{SY} = \pm 18 V$

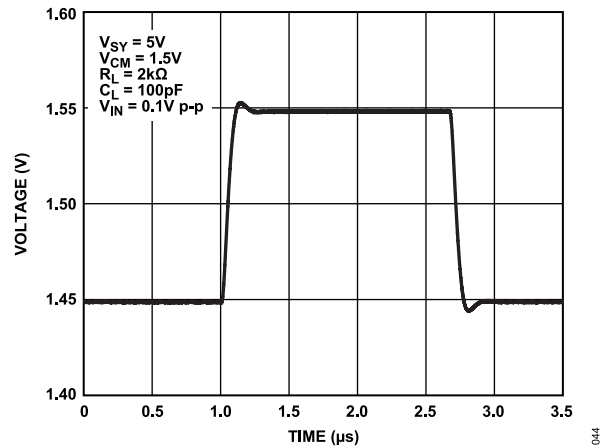


Figure 50. Small Signal Transient Response,  $A_V = -1$ ,  $V_{SY} = 5 V$

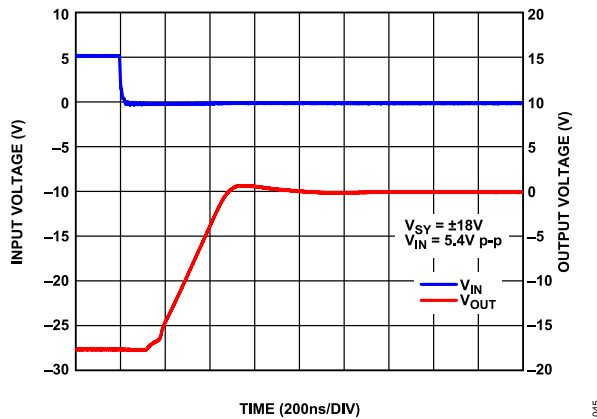


Figure 48. Negative Overload Recovery,  $A_V = -10$ ,  $V_{SY} = \pm 18 V$

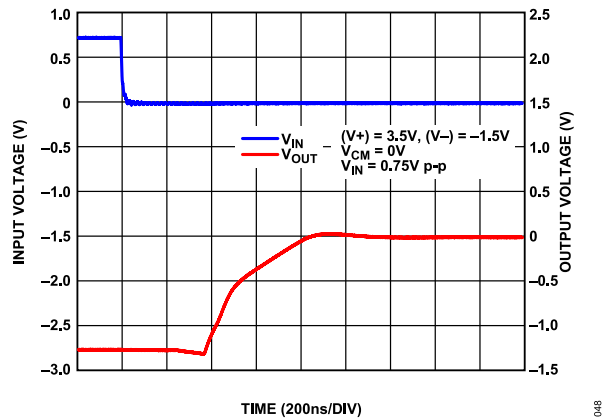


Figure 51. Negative Overload Recovery,  $A_V = -10$ ,  $V_{SY} = 5 V$

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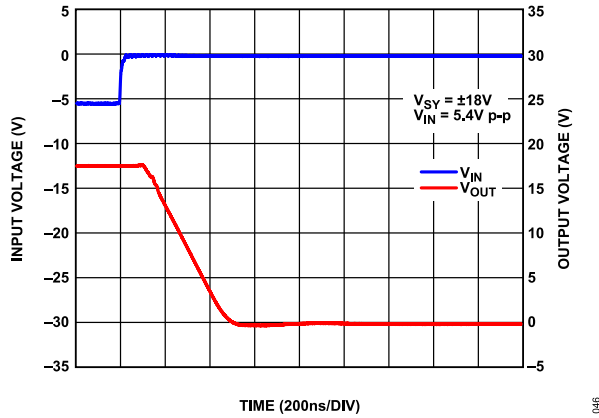


Figure 52. Positive Overload Recovery,  $A_V = -10$ ,  $V_{SY} = \pm 18 V$

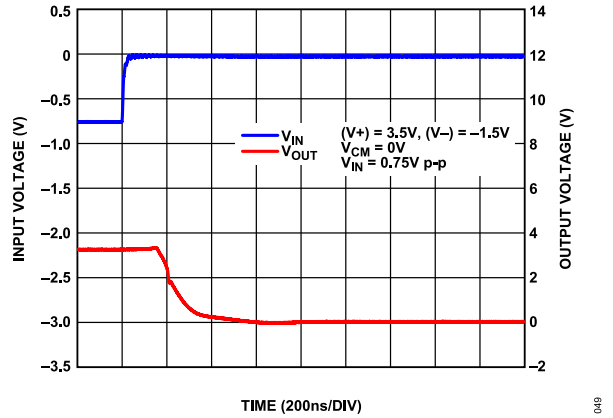


Figure 55. Positive Overload Recovery,  $A_V = -10$ ,  $V_{SY} = 5 V$

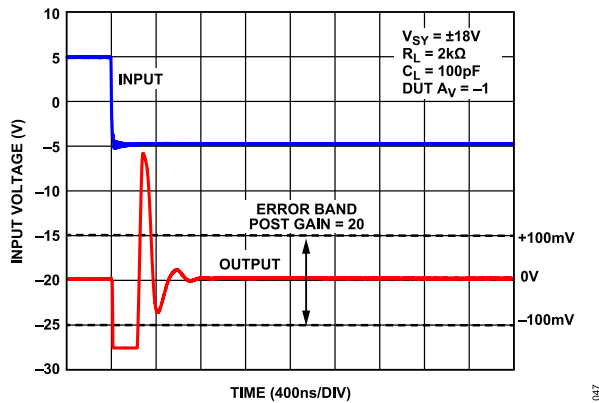


Figure 53. ADA4625-1 Negative Settling Time to 0.1%,  $V_{SY} = \pm 18 V$

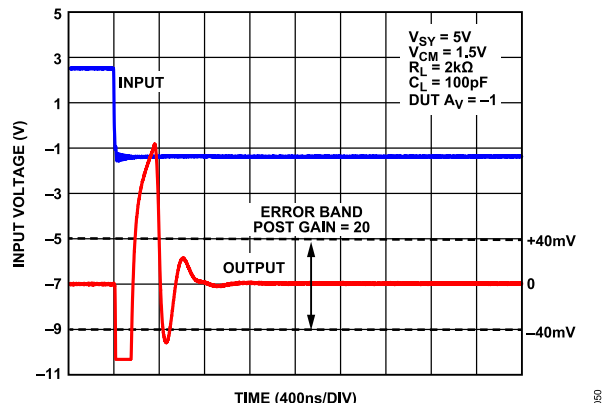


Figure 56. ADA4625-1 Negative Settling Time to 0.1%,  $V_{SY} = 5 V$

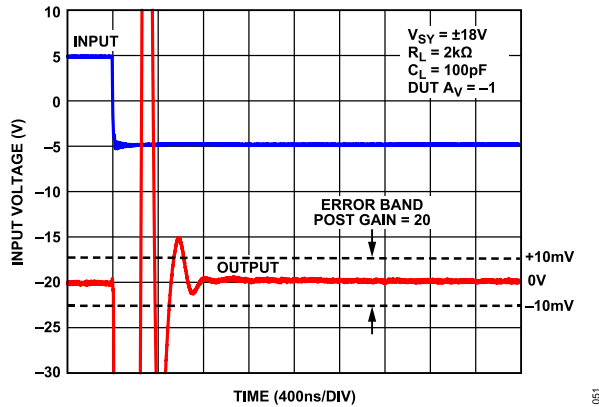


Figure 54. ADA4625-1 Negative Settling Time to 0.01%,  $V_{SY} = \pm 18 V$

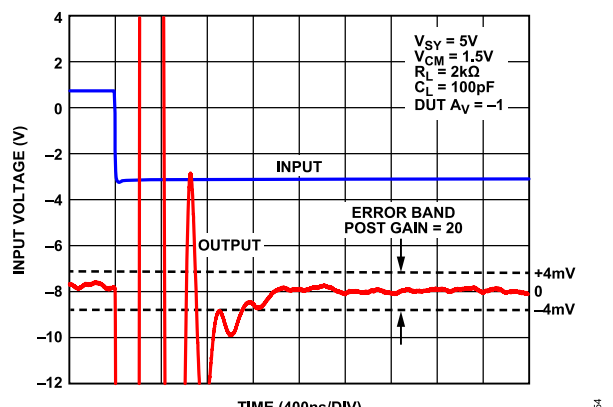


Figure 57. ADA4625-1 Negative Settling Time to 0.01%,  $V_{SY} = 5 V$

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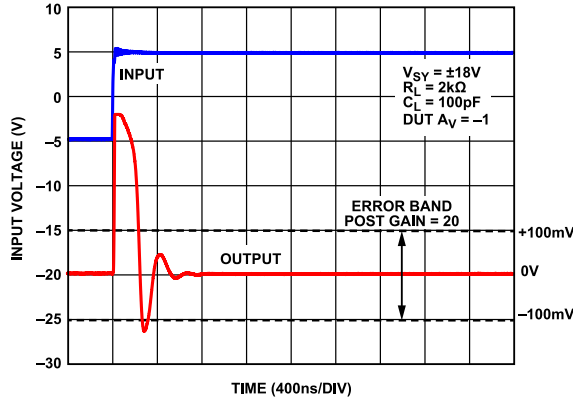


Figure 58. ADA4625-1 Positive Settling Time to 0.1%,  $V_{SY} = \pm 18 V$

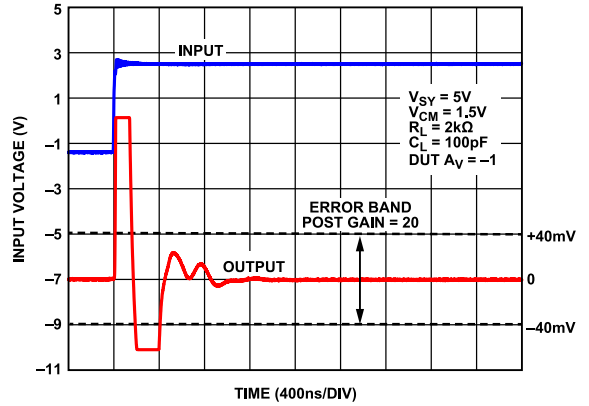


Figure 61. ADA4625-1 Positive Settling Time to 0.1%,  $V_{SY} = 5 V$

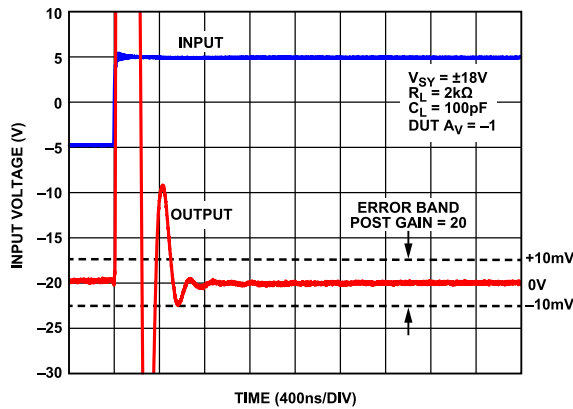


Figure 59. ADA4625-1 Positive Settling Time to 0.01%,  $V_{SY} = \pm 18 V$

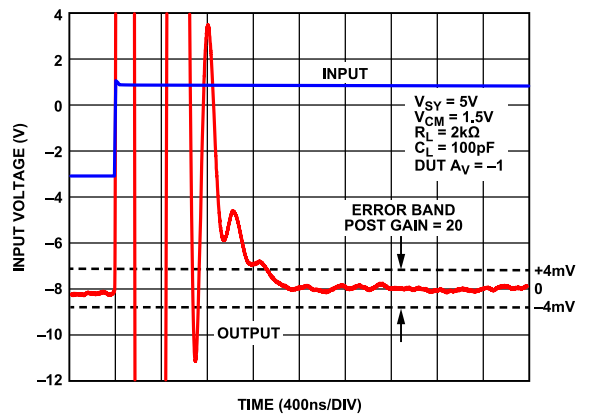


Figure 62. ADA4625-1 Positive Settling Time to 0.01%,  $V_{SY} = 5 V$

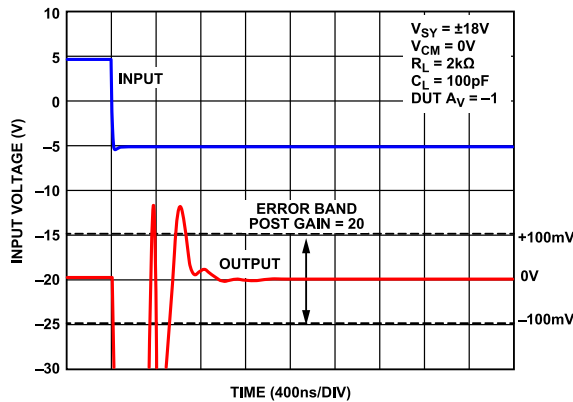


Figure 60. ADA4625-2 Negative Settling Time to 0.1%,  $V_{SY} = \pm 18 V$

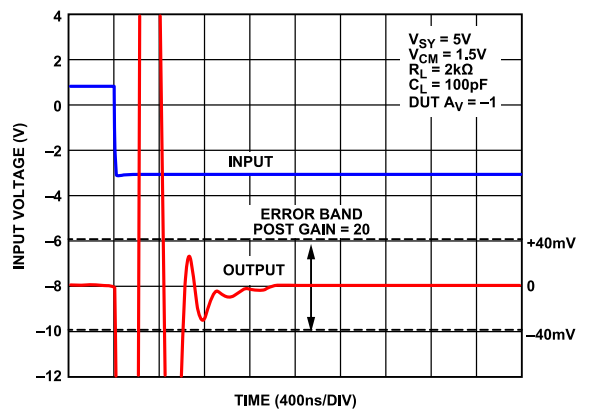


Figure 63. ADA4625-2 Negative Settling Time to 0.1%,  $V_{SY} = 5 V$

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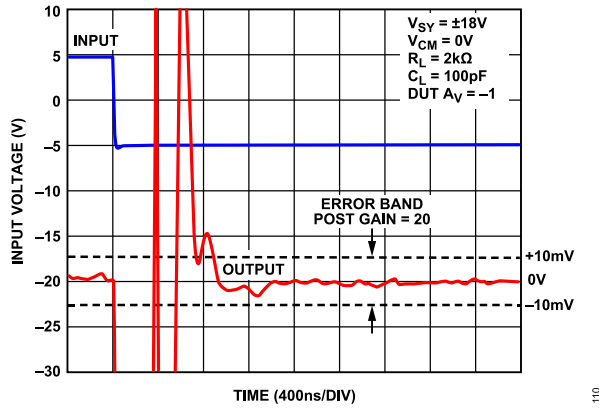


Figure 64. ADA4625-2 Negative Settling Time to 0.01%,  $V_{SY} = \pm 18\text{ V}$

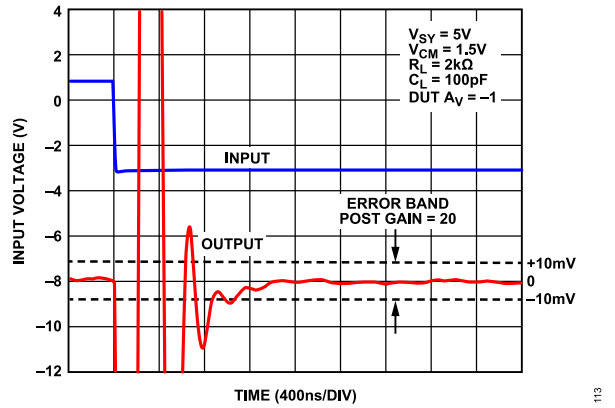


Figure 67. ADA4625-2 Negative Settling Time to 0.01%,  $V_{SY} = 5\text{ V}$

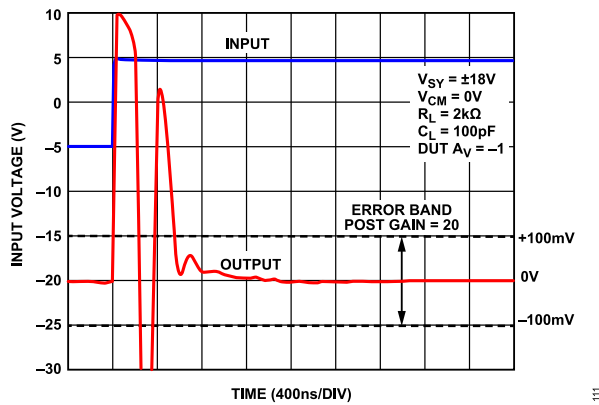


Figure 65. ADA4625-2 Positive Settling Time to 0.1%,  $V_{SY} = \pm 18\text{ V}$

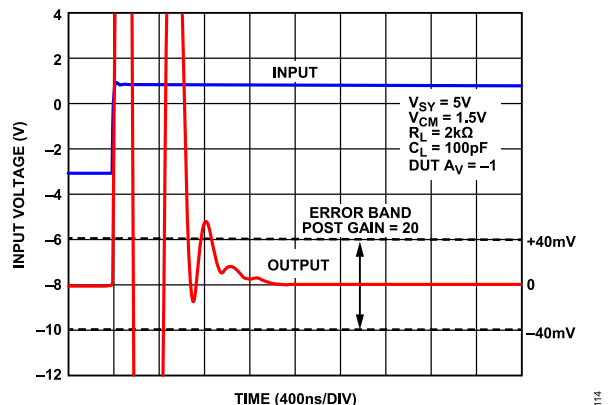


Figure 68. ADA4625-2 Positive Settling Time to 0.1%,  $V_{SY} = 5\text{ V}$

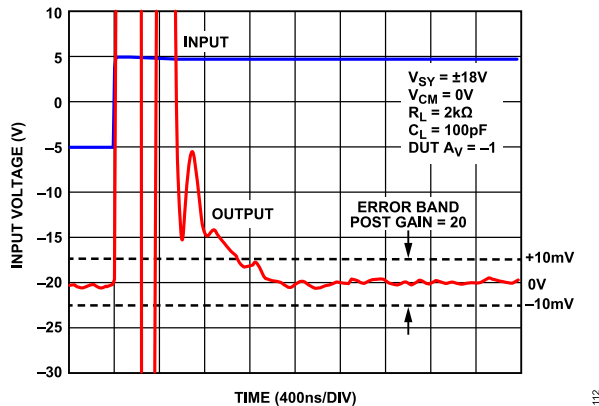


Figure 66. ADA4625-2 Positive Settling Time to 0.01%,  $V_{SY} = \pm 18\text{ V}$

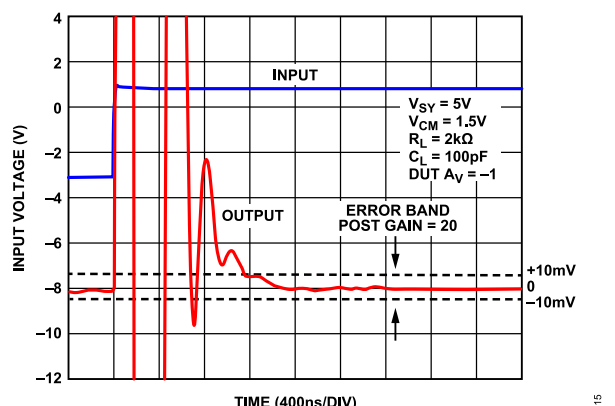


Figure 69. ADA4625-2 Positive Settling Time to 0.01%,  $V_{SY} = 5\text{ V}$

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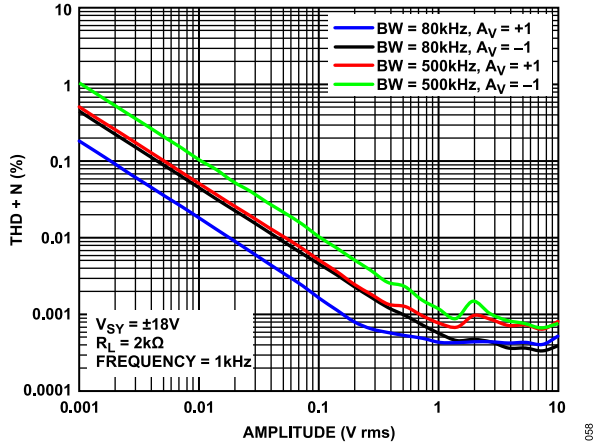


Figure 70. ADA4625-1 Total Harmonic Distortion + Noise (THD + N) vs. Amplitude,  $V_{SY} = \pm 18\text{ V}$  (BW Means Bandwidth)

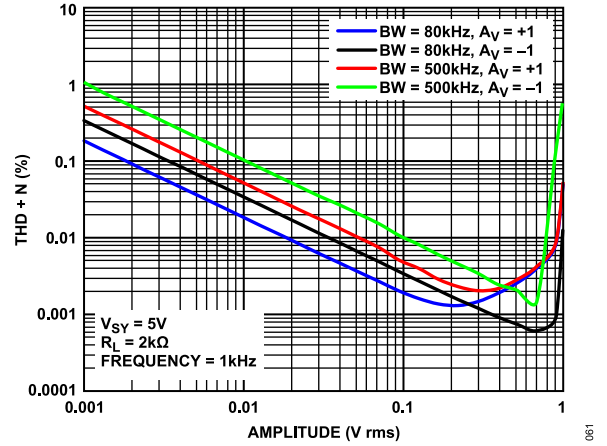


Figure 73. ADA4625-1 THD + N vs. Amplitude,  $V_{SY} = 5\text{ V}$

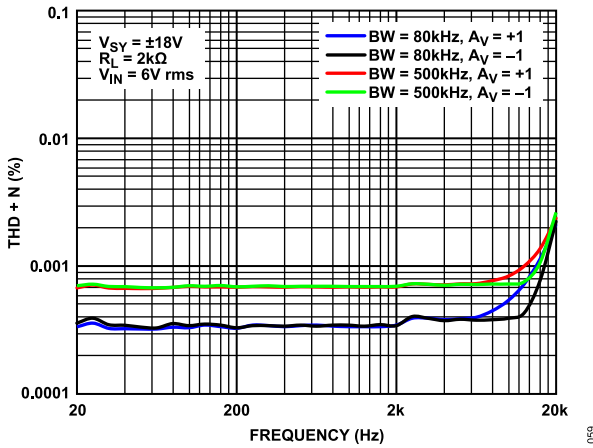


Figure 71. ADA4625-1 THD + N vs. Frequency,  $V_{SY} = \pm 18\text{ V}$

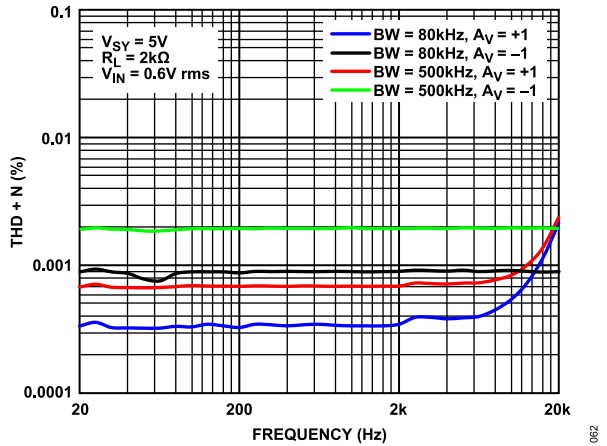


Figure 74. ADA4625-1 THD + N vs. Frequency,  $V_{SY} = 5\text{ V}$

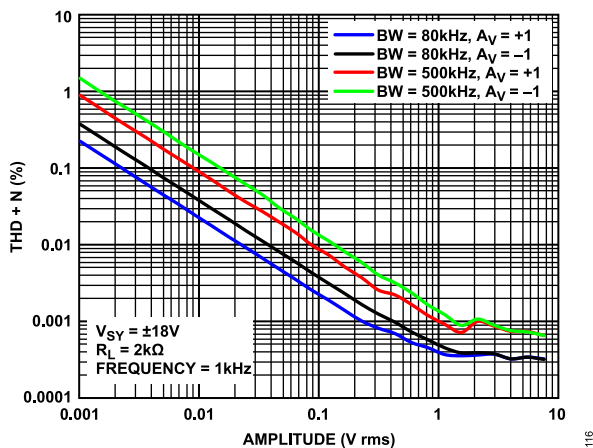


Figure 72. ADA4625-2 THD + N vs. Amplitude,  $V_{SY} = \pm 18\text{ V}$

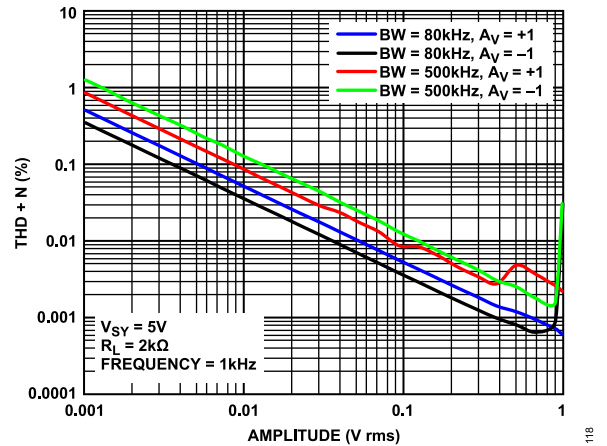


Figure 75. ADA4625-2 THD + N vs. Amplitude,  $V_{SY} = 5\text{ V}$



TYPICAL PERFORMANCE CHARACTERISTICS

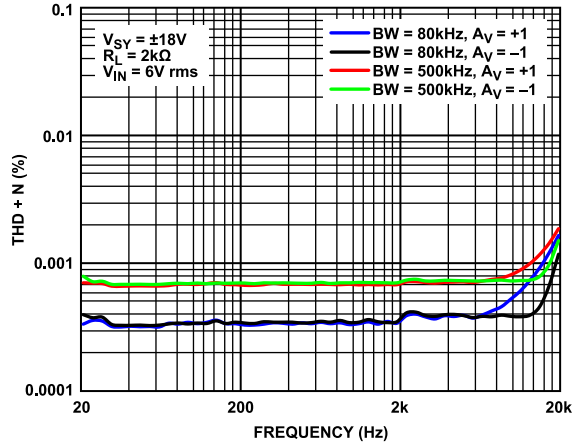


Figure 76. ADA4625-2 THD + N vs. Frequency,  $V_{SY} = \pm 18\text{ V}$

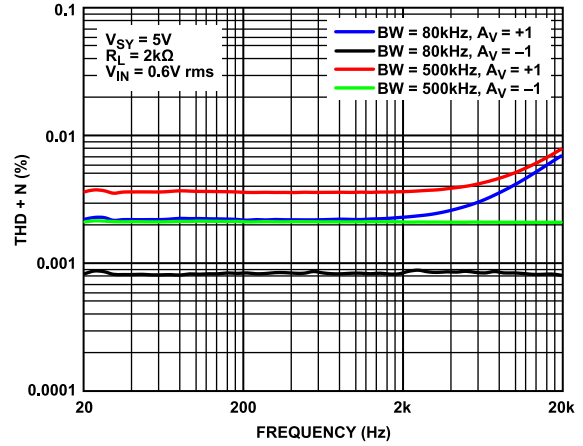


Figure 79. ADA4625-2 THD + N vs. Frequency,  $V_{SY} = 5\text{ V}$

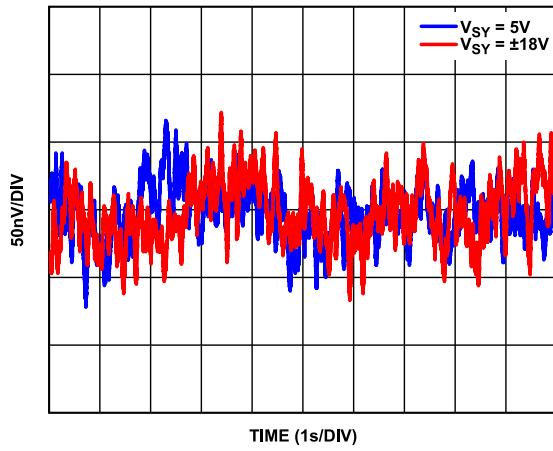


Figure 77. 0.1 Hz to 10 Hz Noise

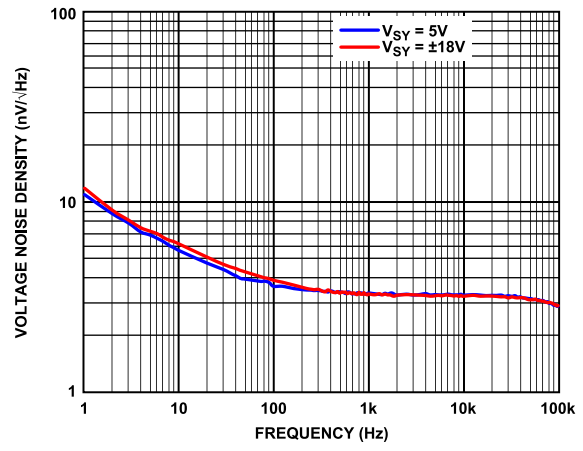


Figure 80. Voltage Noise Density vs. Frequency

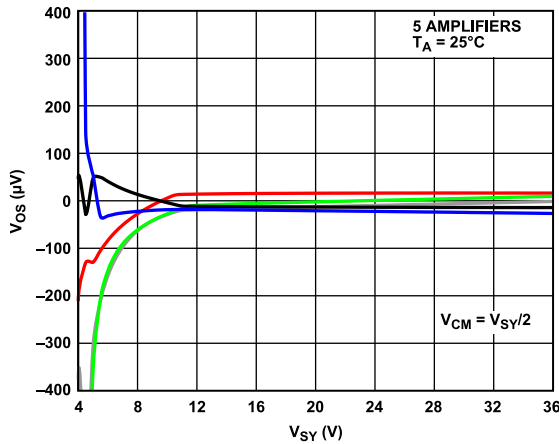


Figure 78.  $V_{OS}$  vs.  $V_{SY}$

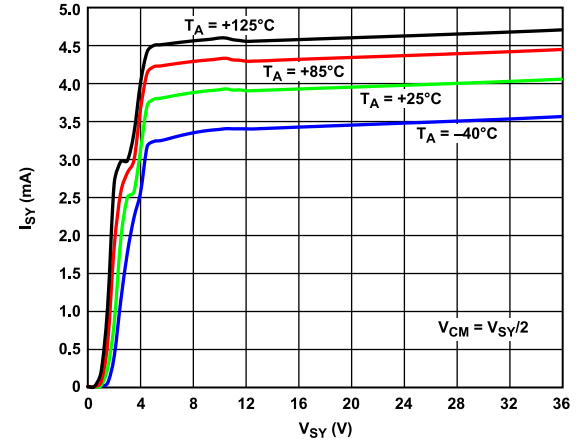


Figure 81. Supply Current ( $I_{SY}$ ) vs.  $V_{SY}$  for Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

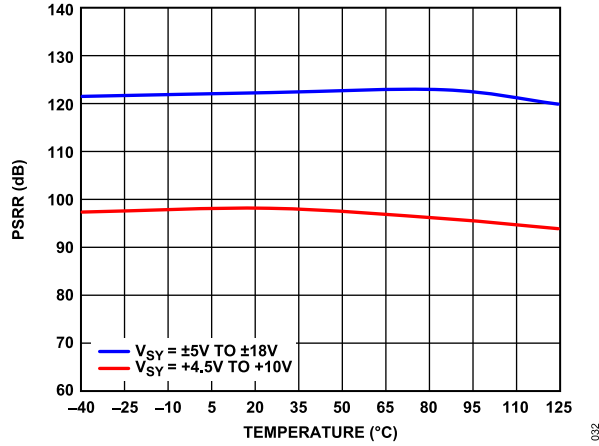


Figure 82. PSRR vs. Temperature

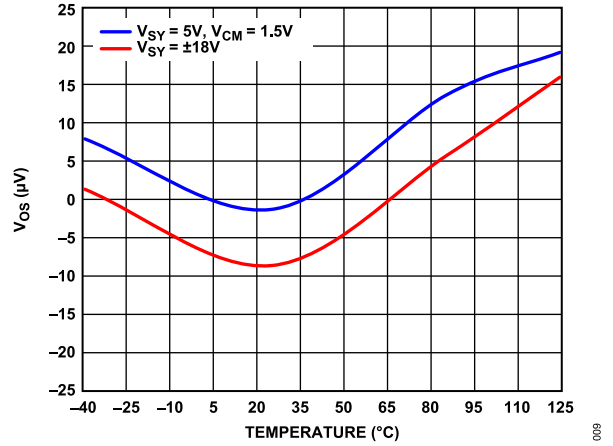


Figure 84.  $V_{OS}$  vs. Temperature

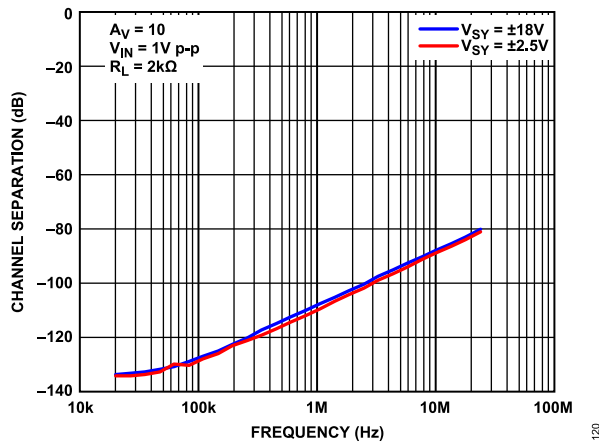


Figure 83. Channel Separation vs. Frequency

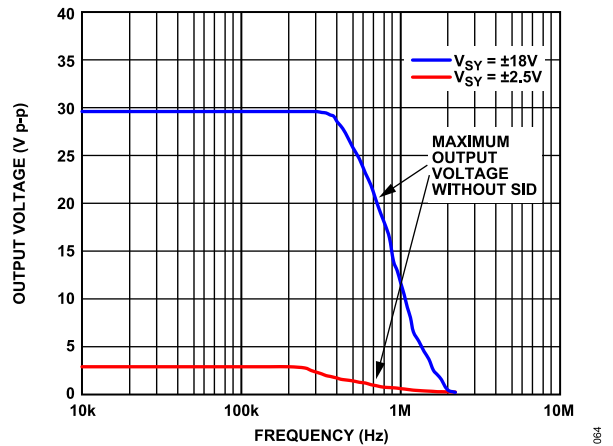


Figure 85. Maximum Peak-to-Peak Output Voltage Without Slew Rate Induced Distortion (SID) vs. Frequency

## THEORY OF OPERATION

Figure 86 shows the simplified circuit diagram for the ADA4625-1/ADA4625-2. The JFET input stage architecture offers the advantages of low input bias current, high bandwidth, high gain, low noise, and no phase reversal when the applied input signal exceeds the common-mode voltage range. The output stage is rail to rail with high drive characteristics and low dropout voltage for both sinking and sourcing currents.

### INPUT AND GAIN STAGES

To achieve high input impedance, low noise, low offset, and low offset drift, the ADA4625-1/ADA4625-2 uses large input N channel JFETs (M1 and M2). These JFETs operate with the S source at about 1.2 V above the G gate. In the worst case, the source is only 0.9 V above the gate. By design, the normal operation of the input tail current ( $I_{TAIL}$ ) extends down to 0.6 V above  $V_-$ , which gives the ADA4625-1/ADA4625-2 an input common-mode range down to 0.2 V below  $V_-$  with margin. Resistive loads keep the noise low. The BUFF1 buffer drives the top of the input load resistors (R1 and R2), keeping the voltage drop across M1 and M2 nearly constant, making a virtual cascode. The differences of the input

voltages of +IN and -IN steer  $I_{TAIL}$  through M1 and M2 to R1 and R2, generating a differential voltage. The first voltage to current gain block (GM1) translates that differential voltage into differential currents ( $I1$  and  $I2$ ) that drive the current mirror (Q1 and Q2), which generates a differential voltage between the reference node and gain node. JFET inputs of the second voltage to current gain block (GM2) maximizes the gain node impedance, giving the ADA4625-1/ADA4625-2 a high gain.

### OUTPUT STAGE

The GM2 gain block generates two pairs of differential currents. One pair drives the bottom current mirror (Q3 and Q4) and the NPN output transistor (Q7), and the second pair drives the top current mirror (Q5 and Q6) and the output PNP transistor (Q8). The common emitter output transistors (Q7 and Q8) source and sink current rail to rail. GM2 also senses the base voltages of Q7 and Q8 and adjusts the  $I4$  and  $I6$  currents; with no output load, Q7 and Q8 collector currents are 0.6 mA. In addition, GM2 clamps the base voltages of Q7 and Q8 so neither completely turns off.

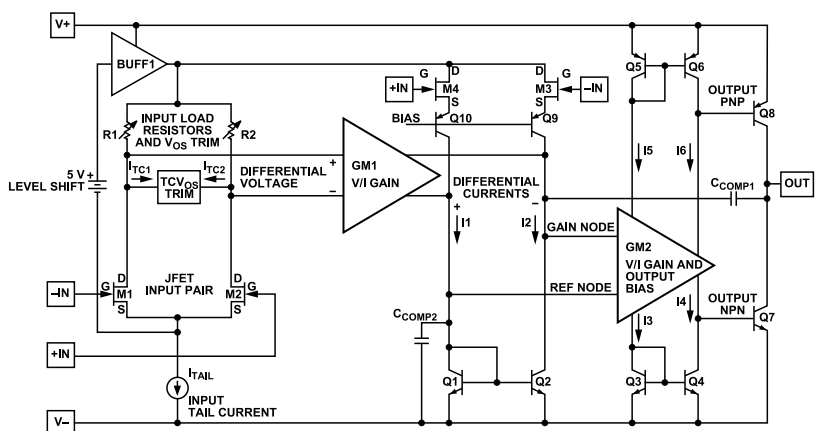


Figure 86. Simplified Circuit Diagram

**THEORY OF OPERATION**

**NO PHASE INVERSION**

Rail-to-rail output (RRO) amplifiers without rail-to-rail input (RRI) are prone to phase inversion because the output can drive the input outside of the normal common-mode range, causing the output to go in the wrong direction and latch up. To prevent phase inversion, the input must control the input at all times. Even though the RRO of the ADA4625-1/ADA4625-2 input stage (M1, M2, R1, and R2) operates correctly down to 0.2 V below  $V_-$ , it does not operate correctly within 2.5 V of  $V_+$ . The ADA4625-1/ADA4625-2 guarantees no phase inversion by implementing an input pair (M3 and M4) to extend the common-mode range to 0.2 V above  $V_+$ , with reduced performance. M3 and M4 are not active in the normal common-mode range. Figure 87 shows that the input voltage exceeds both supplies by 200 mV with no phase inversion at the output.

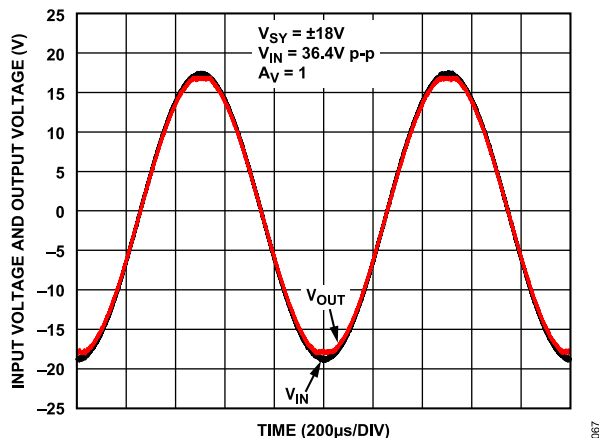


Figure 87. No Phase Reversal if the Input Range Exceeds the Power Supply by 200 mV

**SUPPLY CURRENT**

The supply current ( $I_{SY}$ ) is the quiescent current drawn by the op amp with no load. Figure 88 and Figure 89 show that the quiescent current varies with the common-mode input voltage. The shape of  $I_{SY}$  vs.  $V_{CM}$  at higher  $V_{CM}$  shows saturation of BUFF1 and the  $I_{TAIL}$  turn off.

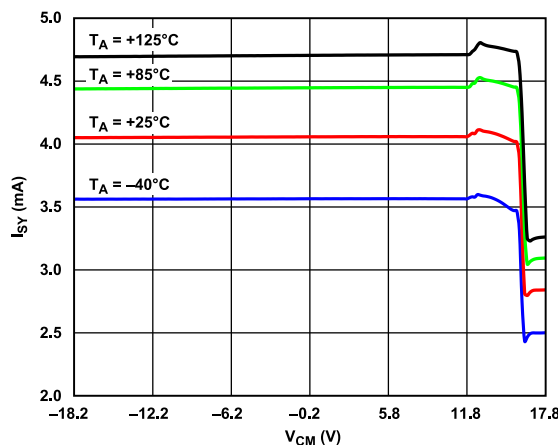


Figure 88.  $I_{SY}$  vs.  $V_{CM}$ ,  $V_{SY} = \pm 18$  V

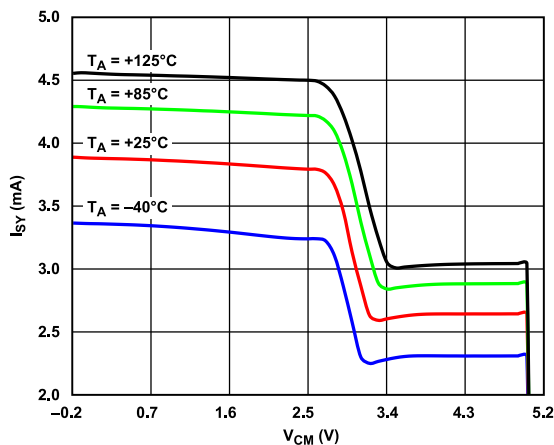


Figure 89.  $I_{SY}$  vs.  $V_{CM}$ ,  $V_{SY} = 5$  V

APPLICATIONS INFORMATION

ACTIVE LOOP PLL FILTER FOR PHASE-LOCKED LOOPS (PLLs)

PLL Basic

A PLL is a feedback system that combines a phase detector (PD), a loop filter, and a voltage controlled oscillator (VCO) that is so connected that the oscillator maintains a constant frequency (or phase angle) relative to the reference signal. The functional block diagram of a basic PLL is shown in Figure 90.

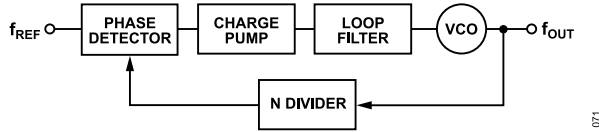


Figure 90. Basic PLL

The phase detector detects the phase difference between the input reference signal and the feedback signal. The resulting error signal is proportional to the relative phase of the input and the feedback signals. The charge pump converts the PD error signal into current pulses. A loop filter circuit is typically required to integrate and smooth the source and sink current pulses from the charge pump into a voltage, which in turn drives the VCO. The VCO outputs a range of frequencies depending on the voltage level at its tuning port. By making the frequency N divider programmable, the VCO frequency can be tuned in either integer steps or fractional amounts characterizing the PLL as either an integer-N PLL or a fractional-N PLL. Because a PLL is a negative feedback loop, the output of the VCO adjusts as necessary until the frequency error signal is zero and the PLL is in lock. The output frequency is given by  $f_{OUT} = N \times f_{REF}$ .

Figure 91 shows the block diagram of the basic PLL model in the Laplace transform format, where  $f_{REF}$  is the frequency of the input signal, and  $f_{OUT}$  is the frequency of the VCO output signal. Because the phase difference is the integral of the frequency difference, there is a  $1/s$  term in the PLL loop.

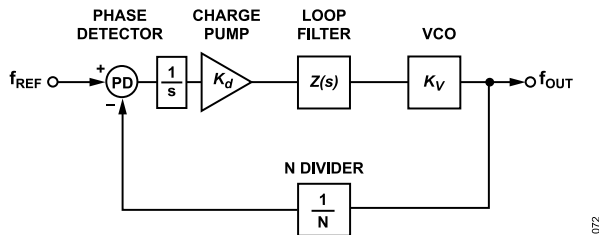


Figure 91. Basic PLL Model

Loop Filter

The loop filter, which smooths out the error signal, is a critical part of the system. For applications that require low phase noise and a wide tuning range, design the VCO with a low gain and a large input voltage range to satisfy these requirements. When the required VCO tuning voltage is higher than the maximum voltage the charge pump can supply, implement an active loop filter comprising of an op amp with gain to accommodate the higher tuning voltages. Figure 92 and Figure 93 illustrate the typical active loop filters in inverting and noninverting topologies, respectively, with prefiltering.

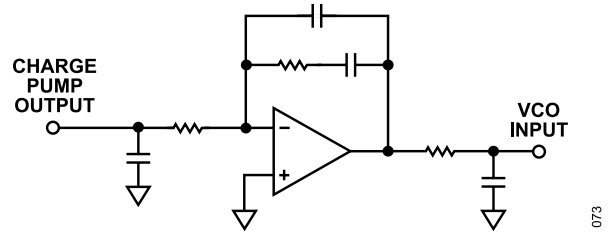


Figure 92. Typical Active Loop Filter—Inverting Topology

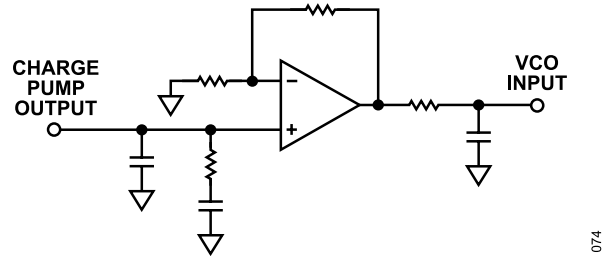


Figure 93. Typical Active Loop Filter—Noninverting Topology

The inverting topology has the advantage of biasing the charge pump output at a fixed voltage, typically one-half the charge pump voltage ( $V_P/2$ ), which is optimal for spur performance. When using the inverting topology, ensure that the PLL IC allows the phase detector polarity to be inverted for the correct polarity voltage at the output of the op amp for driving the VCO.

APPLICATIONS INFORMATION

ADA4625-1 ADVANTAGES AND DESIGN EXAMPLE

The op amp choice for an active filter affects the key performance parameters of the PLLs: frequency range, phase noise, spurious frequencies, and lock time. The output of the filter directly affects the generated frequency and phase. Low noise is essential because any voltage noise applied to the tuning port of the VCO is amplified by the VCO gain and translated into phase noise. Low input bias current is also recommended because the op amp bias current must be sourced from the PLL phase detector/ charge pump, and any mismatch or leakage at the output of the phase detector between the up and down currents causes ripples and reference spurs.

With 18 MHz gain bandwidth product (GBP), low input bias currents ( $\pm 15$  pA), low voltage noise density (3.3 nV/ $\sqrt{\text{Hz}}$ ), ultralow current noise density, and low 1/f corner frequency, the ADA4625-1 is an ideal op amp for using in a PLL active loop filter. The ADA4625-1 does not require a negative voltage supply because of its ground sensing input. The rail-to-rail output stage is beneficial in terms of increasing the flexibility in biasing the op amp so that the output range of the PLL is mapped efficiently onto the input range of the VCO. In addition, the wide 5 V to 36 V operating supply range makes the ADA4625-1 a versatile choice for the design of a wide variety of active loop filters.

Figure 95 shows the ADA4625-1 as the loop filter for the ADF4159, a 13 GHz fractional-N synthesizer. The phase detector polarity of the ADF4159 is programmed to negative because the ADA4625-1

is used in an inverting active loop filter configuration. The VCO is set up to feedback the VCO/2 output to the ADF4159. The loop filter has a 900 kHz loop bandwidth (LBW) and a phase margin of 58° with 2.5 mA charge pump current. Lowering the bandwidth further improves phase noise at the expense of increased PLL lock time.

Figure 94 shows the PLL loop filter transfer function. Capacitor C1 and Resistor R1 change the phase detector current pulses into a continuous time voltage waveform. At frequencies lower than the R2C2 zero, the amplifier and R1C2 form an integrator. Between the R2C2 zero and the R2C3 pole, the gain is constant at the value set by R2/R1. Above the R2C3 pole, the amplifier is an integrator until R1C3 becomes a feedforward noninverting zero path around the amplifier. Resistor R3 and Capacitor C4 add an additional pole in the loop filter signal path. Setting the R3C4 pole below the R2C3 pole reduces the effect of the R1C3 feedforward zero.

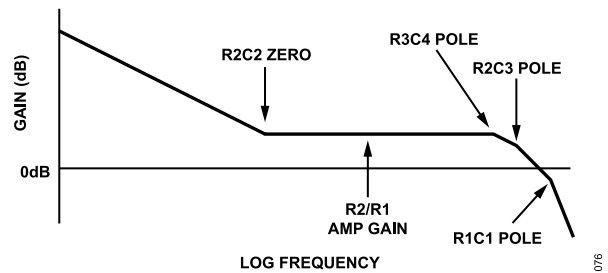


Figure 94. PLL Loop Filter Transfer Function

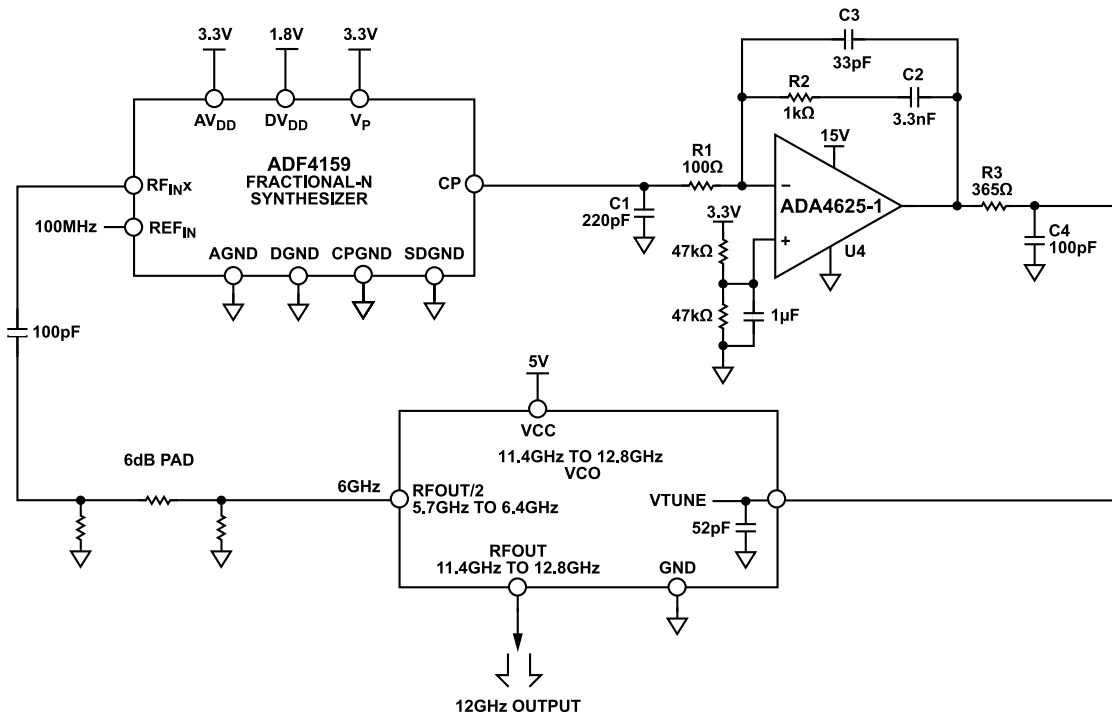


Figure 95. Block Diagram of ADA4625-1 Active Loop Filter for ADF4159

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PLLs in which the loop gain passes through 0 dB above the R2C2 zero and below the R2C3 pole and R3C4 pole are stable. At low charge pump currents, the loop gain passes through zero above R2C2 zero. At high charge pump currents, the loop gain passes through zero below the R2C3 pole and R3C4 pole (see Figure 96).

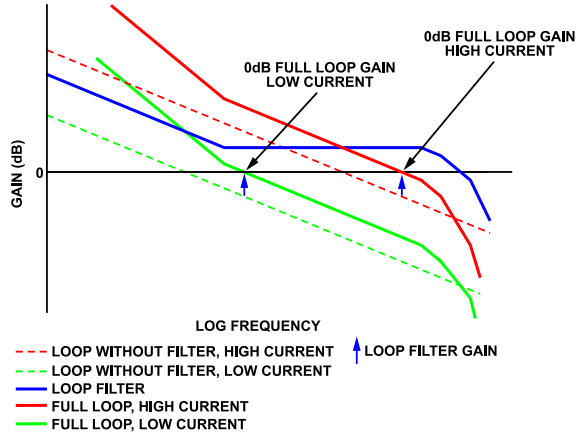


Figure 96. Gain vs. Frequency of PLL and Loop Filter

Figure 97 shows the measured phase noise vs. frequency offset from 12 GHz carrier for different charge pump currents ( $I_{CP}$ ). Generally, most operations have a charge pump current of 2.5 mA and below. Refer to the UG-383 User Guide for details on running these tests and setting up the software required.

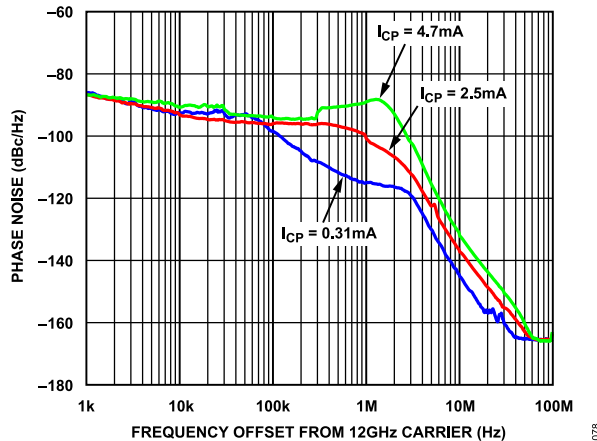


Figure 97. Phase Noise vs. Frequency Offset from 12 GHz Carrier for Different Charge Pump Currents ( $I_{CP}$ )

The Analog Devices simulation tool, ADIsimPLL, allows the design and simulation of PLL loop filter topologies and has a library of Analog Devices op amps built in. The simulation tool accurately predicts PLL closed-loop phase noise and is able to model the effect of op amp noise along with the noise of the other PLL loop components. For more information about the ADIsimPLL design tools, refer to [www.analog.com/ADIsimPLL](http://www.analog.com/ADIsimPLL).

TRANSIMPEDANCE AMPLIFIER

The ADA4625-1 is an excellent choice for low noise transimpedance amplifier (TIA) applications. While its low voltage and current noise maximize signal-to-noise ratio (SNR), its low voltage offset and input bias current minimize the dc error at the amplifier output. Having a true ground sense capability, the ADA4625-1 is ideal for single-supply operation. In addition, its rail-to-rail output swing allows the detection and amplification of a wide range of input current signals. Figure 98 shows the ADA4625-1 as a current to voltage (I-V) converter with an electrical model of a photodiode.

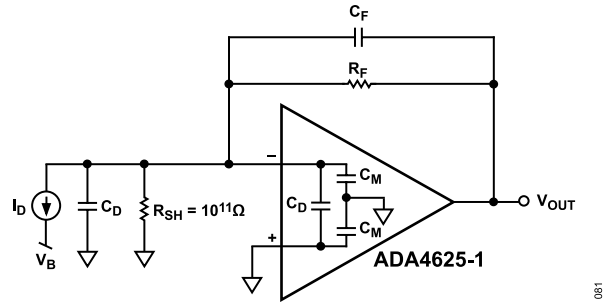


Figure 98. Equivalent TIA Circuit

Photodiodes can operate in either photovoltaic mode (zero bias) or photoconductive mode (with an applied reverse-bias across the diode). Mode selection depends on the speed and dark current requirements of the application and the choice of photodiode. In photovoltaic mode, the dark current is at a minimum and is preferred for low frequency and/or low light level applications (that is, PN photodiodes). Photoconductive mode is better for applications that required faster and linear responses (that is, PIN photodiodes); however, the tradeoffs include increases in dark and noise currents.

The following transfer function describes the transimpedance gain of Figure 98:

$$V_{OUT} = \frac{I_D R_F}{1 + s C_F R_F} \tag{1}$$

where:

$V_{OUT}$  is the desired output dc voltage of the op amp.

$I_D$  is the output current of the photodiode.

$R_F$  and  $C_F$  are the feedback resistor and capacitor. The parallel combination of  $R_F$  and  $C_F$  sets the signal bandwidth.

$s$  is the s plane.

Set  $R_F$  such that the maximum attainable output voltage corresponds to the maximum diode output current. Because signal levels increase directly with  $R_F$ , while the noise due to  $R_F$  increases with the square root of the resistor value, employing the full output swing maximizes the SNR.

It is important to distinguish between the signal gain and the noise gain (NG) because the noise gain characteristics determine the net circuit stability. The noise gain has the same transfer function as the noninverting signal gain, which follows:



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$$NG = \left(1 + \frac{R_F}{R_{SH}}\right) \times \frac{1 + s(R_F // R_{SH})(C_{IN} + C_F)}{1 + sR_F C_F} \quad (2)$$

where:

$R_{SH}$  is the diode shunt resistance.

$C_{IN}$  is the total input capacitance consisting of the sum of the diode shunt capacitance ( $C_D$ ), the input capacitance of the amplifier ( $C_{DM} + C_{CM}$ ), and the external stray capacitance.

$C_{IN}$  and  $R_F$  produce a zero in the noise gain transfer function and the zero frequency ( $f_z$ ) is as follows:

$$f_z = \frac{1}{2\pi(R_F // R_{SH})(C_{IN} + C_F)} \quad (3)$$

Because the photodiode shunt resistance  $R_{SH} \gg R_F$ , the circuit behavior is not impacted by the effect of the junction resistance, and  $f_z$  simplifies to

$$f_z = \frac{1}{2\pi R_F (C_{IN} + C_F)} \quad (4)$$

Figure 99 shows the TIA noise gain superimposed upon the open loop gain of the amplifier. For the system to be stable, the noise gain curve must intersect with the open loop response with a net slope of less than 20 dB/decade. In Figure 99, the dotted line shows an uncompensated noise gain ( $C_F = 0$  pF) intersecting with the open loop gain at the frequency ( $f_x$ ) with a slope of 20 dB/decade, indicating an unstable condition.

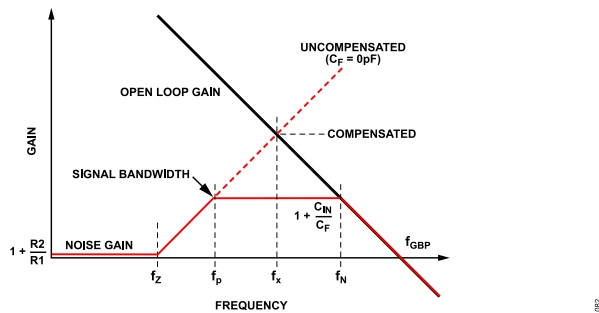


Figure 99. Generalized TIA Noise Gain and Transfer Function

The instability caused by  $C_{IN}$  can be compensated by adding  $C_F$  to introduce a pole at a frequency equal to or lower than  $f_x$ . The pole frequency is as follows:

$$f_p = \frac{1}{2\pi R_F C_F} \quad (5)$$

Setting the pole at the  $f_x$  frequency maximizes the signal bandwidth with a 45° phase margin but is marginal for stability, as indicated by the dashed line. Because  $f_x$  is the geometric mean of  $f_z$  and the gain bandwidth product frequency ( $f_{GBP}$ ) of the amplifier, calculate  $f_x$  by

$$f_x = \sqrt{f_z f_{GBP}} \quad (6)$$

Substituting Equation 4 and Equation 5 into Equation 6, the  $C_F$  value that produces  $f_x$  is

$$C_F = \frac{1 + \sqrt{1 + 8\pi R_F C_{IN} f_{GBP}}}{4\pi R_F f_{GBP}} \quad (7)$$

If  $8\pi \times R_F \times C_{IN} \times f_{GBP} \gg 1$ , Equation 7 simplifies to

$$C_F = \sqrt{\frac{C_{IN}}{2\pi R_F f_{GBP}}} \quad (8)$$

Adding  $C_F$  also sets the signal bandwidth at  $f_p$ . Substitute Equation 8 into Equation 5 and rearrange the equation for the signal bandwidth in terms of  $f_{GBP}$ ,  $R_F$ , and  $C_{IN}$ :

$$f_p = \sqrt{\frac{f_{GBP}}{2\pi R_F C_{IN}}} \quad (9)$$

Notice the attainable signal bandwidth is a function of the time constant  $R_F C_{IN}$  and the  $f_{GBP}$  of the amplifier. To maximize the signal bandwidth, choose an op amp with high bandwidth and low input capacitance, and operate the photodiode in reverse bias to reduce its junction capacitance.

Because the input current noise of the FET input op amp is negligible, and the shot noise of the photodiode is negligible due to the filtering effect of the shunt capacitance, the dominant sources of output noise in the wideband photodiode TIA circuit are the input voltage noise of the amplifier  $e_N$  and the thermal noise generated by  $R_F$ .

At low frequencies, the circuit noise gain is  $1 + R_F/R_{SH}$ . At frequencies equal to or greater than  $f_z$ , the noise gain begins to increase and plateau when the gain is  $1 + C_{IN}/C_F$  (see Figure 99). In addition, the noise bandwidth frequency,  $f_N$  (where the compensated noise gain intersecting the open loop gain), can be estimated by

$$f_N = \frac{C_F}{(C_{IN} + C_F)} f_{GBP} \quad (10)$$

Design Example

As a design example, Figure 100 shows the ADA4625-1 configured as a TIA amplifier in a photodiode preamp application. Assuming the photodiode has a  $C_D$  of 5 pF and an  $I_D$  of 200  $\mu$ A, and the desired full-scale  $V_{OUT}$  is 10 V, and using Equation 1,  $R_F$  is 50 k $\Omega$ .



APPLICATIONS INFORMATION

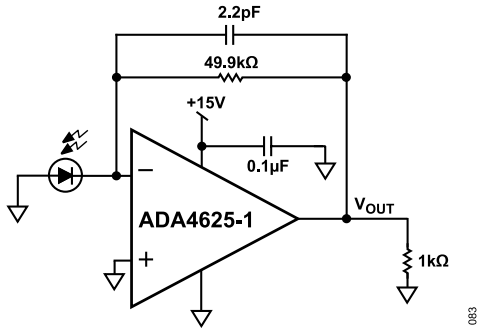


Figure 100. Single-Supply TIA Circuit Using the ADA4625-1

The ADA4625-1 input capacitance ( $C_{CM} + C_{DM}$ ) is 19.9 pF; therefore, the total input capacitance ( $C_{IN}$ ) is 24.9 pF. By substituting  $C_{IN} = 24.9$  pF,  $R_F = 50$  kΩ, and  $f_{GBP} = 18$  MHz into Equation 7 and Equation 9, the resulting feedback capacitor value ( $C_F$ ) and the -3 dB signal bandwidth ( $f_p$ ) are 2.2 pF and 1.45 MHz, respectively.

Figure 101 and Figure 102 show the compensations of the TIA circuit. The system has a bandwidth of 1.45 MHz when it is maximized for a signal bandwidth with  $C_F = 2.2$  pF. Increasing  $C_F$  to 3.9 pF reduces the bandwidth to 0.82 MHz; however, it greatly reduces the overshoot (see Figure 103). In practice, an optimum  $C_F$  value is determined experimentally by varying it slightly to optimize the output pulse response.

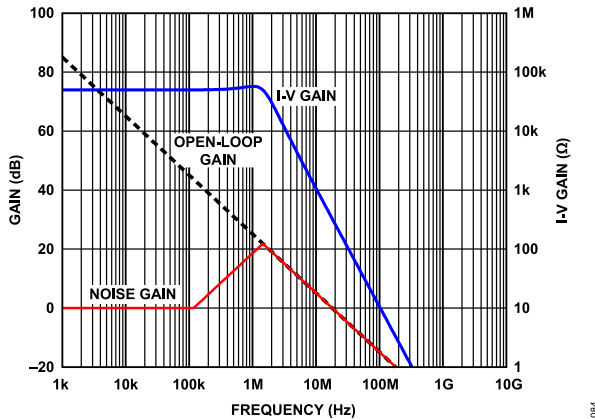


Figure 101. Compensating the TIA,  $C_F = 2.2$  pF

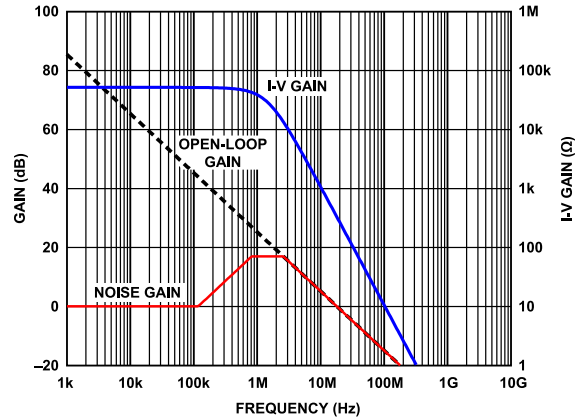


Figure 102. Compensating the TIA,  $C_F = 3.9$  pF

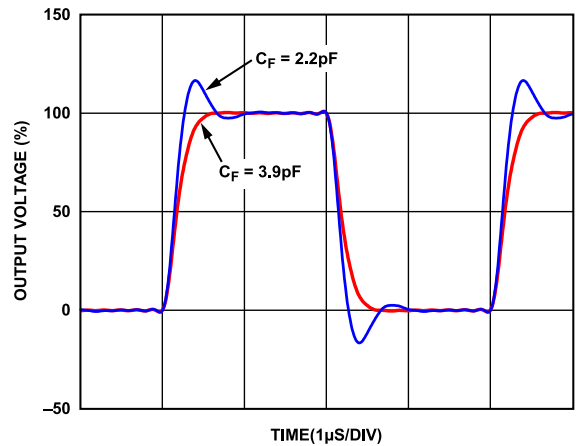


Figure 103. Pulse Response vs.  $C_F$

Table 8 shows the noise sources and estimated total output noise for the photodiode amplifier with  $C_F = 2.2$  pF and  $C_F = 3.9$  pF, respectively.

Use the Analog Devices [Analog Photodiode Wizard](#) to design a transimpedance amplifier circuit to interface with a photodiode.

Table 8. RMS Noise Contributions of the Photodiode Preamplifier

Noise Contributor	Expression	RMS Noise ( $\mu V$ ) <sup>1</sup>	
		$C_F = 2.2$ pF	$C_F = 3.9$ pF
$R_F$	$\sqrt{4kTR_F \left( \frac{\pi}{2} f_p \right)}$ <p>where:  <math>k</math> is Boltzmann's constant (<math>1.38 \times 10^{-23}</math> J/K).  <math>T</math> is the temperature in Kelvin (K).</p>	(11) 43.2	32.5
Current Noise, $V_{ni, AMP}$	$i_N R_F \sqrt{\frac{\pi}{2} f_p}$	(12) 0.34	0.25

## APPLICATIONS INFORMATION

Table 8. RMS Noise Contributions of the Photodiode Preamplifier (Continued)

Noise Contributor	Expression	RMS Noise ( $\mu\text{V}$ ) <sup>1</sup>	
		$C_F = 2.2 \text{ pF}$	$C_F = 3.9 \text{ pF}$
Voltage Noise, $V_{nv, AMP}$	$e_N \sqrt{\left(1 + \frac{C_{IN}}{C_F}\right) \frac{\pi}{2} f_{GBP}} \quad (13)$	61.6	47.7
Total Noise	$\sqrt{V_{nv, AMP}^2 + V_{nv, AMP}^2 + V_{R_F}^2} \quad (14)$	75.2	57.7

<sup>1</sup> RMS noise with  $R_F = 49.9 \text{ k}\Omega$ ,  $C_{IN} = C_{CM} + C_{DM} = 19.9 \text{ pF}$ ,  $C_D = 5 \text{ pF}$ ,  $i_N = 4.5 \text{ fA}/\sqrt{\text{Hz}}$ , and  $e_N = 3.3 \text{ nV}/\sqrt{\text{Hz}}$ .

APPLICATIONS INFORMATION

DAC OUTPUT DRIVER

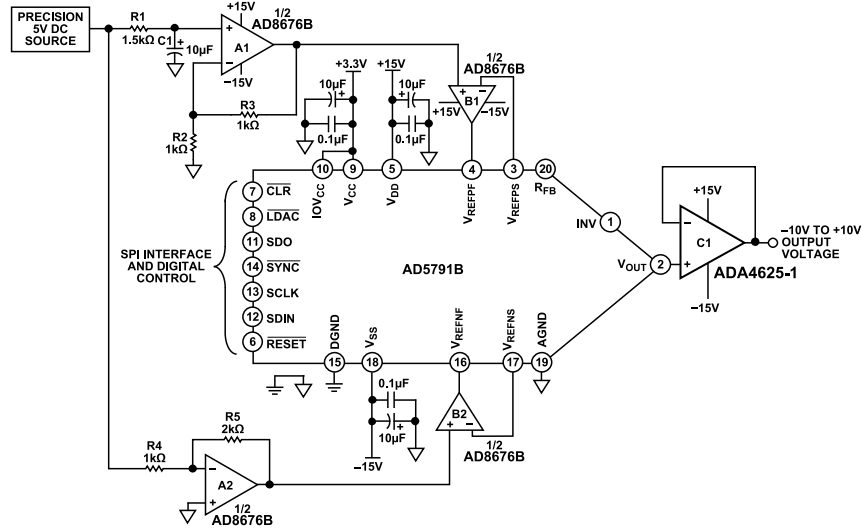


Figure 104. 20-Bit Accurate, ±10 V Voltage Source (Simplified Schematic: All Connections and Decoupling Not Shown)

ADA4625-1 can be used as an output buffer for 20-bit accurate, ±10 V voltage source with the AD5791 and the LTC6655. The low voltage noise, low drift output drive capability of the ADA4625-1, as well as dynamic parameters such as fast settling time and slew rate make the device an ideal DAC output buffer. It is recommended to provide supplies of ±15 V to obtain the full potential of the ADA4625-1 in this application due to the input  $V_{CM}$  range of the device.

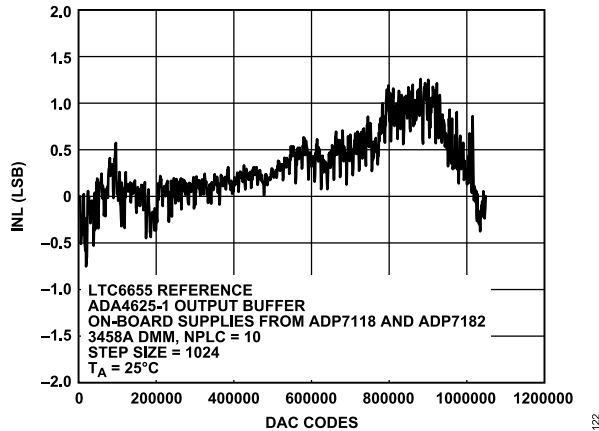


Figure 105. AD5791 with LTC6655 and ADA4625-1 as Output Buffer INL Performance

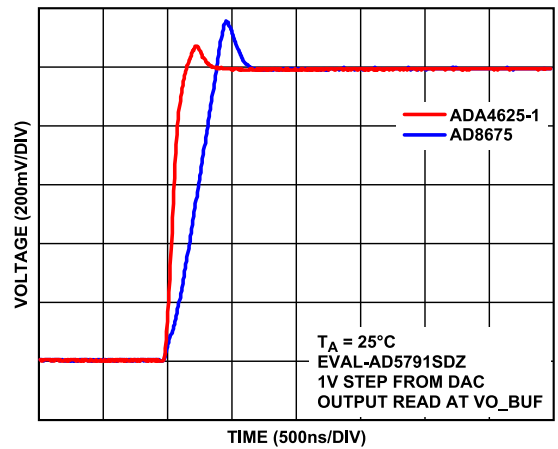


Figure 106. Step Response with ADA4625-1 and AD8675 Output Buffers

Figure 105 and Figure 106 show the INL response with the EVAL-AD5791SDZ and the step response of the ADA4625-1 in comparison to the AD8675, respectively.

## APPLICATIONS INFORMATION

### RECOMMENDED POWER SOLUTION

Analog Devices has a wide range of power management products to meet the requirements of most high performance signal chains.

For a dual-supply application, the ADA4625-1 typically needs a  $\pm 15$  V supply. Low dropout (LDO) linear regulators such as the [ADP7118](#) or the [ADP7142](#) for the positive supply and the [ADP7182](#) for the negative supply help improve the PSRR at high frequency and generate a low noise power rail. In addition, if a negative supply is not available, the [ADP5070](#) can generate the negative supply from a positive supply. [Figure 107](#) shows an example of this power solution configuration for the ADA4625-1.

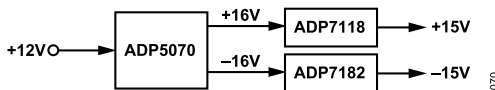


Figure 107. Power Solution Configuration for the ADA4625-1

Table 9. Recommended Power Management Devices

Product	Description
ADP5070	DC-to-dc switching regulator with independent positive and negative outputs
ADP7118	20 V, 200 mA, low noise, CMOS LDO linear regulator
ADP7142	40 V, 200 mA, low noise, CMOS LDO linear regulator
ADP7182	-28 V, -200 mA, low noise, linear regulator

It is recommended to use a low ESR, 0.1  $\mu$ F bypass capacitor close to each power supply pins of the ADA4625-1 and ground to reduce errors coupling in from the power supplies. For noisy power supplies, place an additional 10  $\mu$ F capacitor in parallel with the 0.1  $\mu$ F for better performance.

### INPUT OVERVOLTAGE PROTECTION

The ADA4625-1 has internal protective circuitry that allows voltages as high as 0.2 V beyond the supplies to be applied at the input of either terminal without causing damage. For higher input voltages, a series resistor is necessary to limit the input current. Determine the resistor value by

$$(V_{IN} - V_S)/R_S \leq 20 \text{ mA} \quad (15)$$

where:  $V_{IN}$  is the input voltage.  $V_S$  is the voltage of either V+ or V-.  $R_S$  is the series resistor.

With a very low bias current of <5.5 nA up to 125°C, higher resistor values can be used in series with the inputs. A 500  $\Omega$  resistor protects the inputs from voltages as high as 10 V beyond the supplies and adds less than 2.75  $\mu$ V to the offset. However, note that the added series resistor ( $R_S$ ) may increase the overall noise and lower the bandwidth due to the addition of a pole introduced by  $R_S$  and the input capacitor of the amplifier.

### DRIVING CAPACITIVE LOADS

The inherent output resistance of the op amp combined with a capacitive load forms an additional pole in the transfer function

of the amplifier. Adding capacitance to the output of any op amp results in additional phase lag. This lag reduces stability and leads to overshoot or oscillation, which is a common situation when an amplifier is used to drive the input of switched capacitor analog-to-digital converters (ADCs).

The ADA4625-1 has a high phase margin and low output impedance and is capable of directly driving a capacitive load up to 1 nF with no external compensation at unity-gain without oscillation.

For other considerations and various circuit solutions, see the [Ask the Applications Engineer-25, Op Amps Driving Capacitive Loads](#) Analog Dialogue article.

### THERMAL MANAGEMENT

The ADA4625-1 can operate with up to a 36 V supply voltage with a typical 4 mA quiescent current. Heavy loads increase power dissipation and raise the chip junction temperature.

The maximum safe power dissipation for the ADA4625-1 is limited by the associated rise in junction temperature ( $T_J$ ) on the die. Two conditions affect  $T_J$ : power dissipation ( $P_D$ ) of the device and ambient temperature ( $T_A$ ) surrounding the package. This relationship is shown in [Equation 16](#).

$$T_J = P_D \times \theta_{JA} + T_A \quad (16)$$

where  $\theta_{JA}$  is the thermal resistance between the die and the ambient environment. The total power dissipation in the amplifier is the sum of the power dissipated in the output stage plus the quiescent power. Power dissipation for the sourcing current is shown in [Equation 17](#), where  $V_{SY}$  is the total supply voltage (V+ – V-).

$$P_D = V_{SY} \times I_{SY} + ((V+) - V_{OUT})I_{OUT} \quad (17)$$

Replace  $((V+) - V_{OUT})$  in [Equation 17](#) with  $((V-) - V_{OUT})$  when sinking current.

For symmetrical supplies with a ground referenced load, use the following equation to calculate the average power for the amplifier processing sine signal.

$$P_{AVG, SINE} = (V_{SY} \times I_{SY}) + \left( \frac{2}{\pi} \times \frac{(V+) \times V_{PEAK}}{R_L} \right) - \left( \frac{V_{PEAK}^2}{2 \times R_L} \right) \quad (18)$$

where  $V_{PEAK}$  is the peak value of a sine wave output voltage.

The specified thermal resistance  $\theta_{JA}$  of the ADA4625-1/ADA4625-2 is 52.8°C/W. A good PCB layout and an external heat sink can improve thermal performance by reducing junction to ambient temperature.

The ADA4625-1/ADA4625-2 features an exposed pad that floats internally to provide the maximum flexibility and ease of use. Solder the exposed pad to the PCB board GND, or the V+ or V- plane for

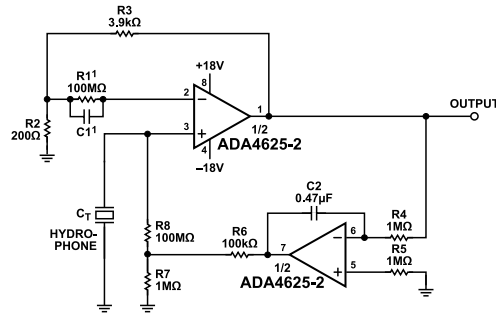
**APPLICATIONS INFORMATION**

best thermal transfer. Where thermal heating is not an issue, the exposed pad can be left floating.

Incorporate the use of thermal vias or heat pipes into the design of the mounting pad for the exposed pad to lower the overall  $\theta_{JA}$ .

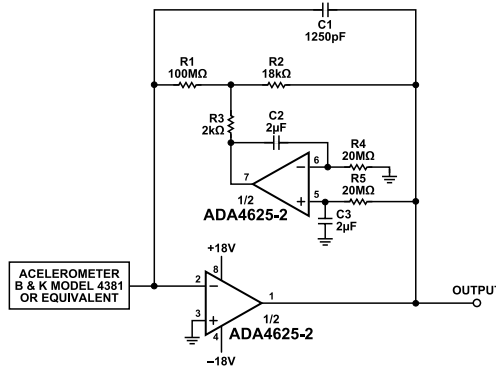
APPLICATIONS INFORMATION

TYPICAL APPLICATIONS



<sup>1</sup>OPTIONAL  
 DC OUTPUT  $\leq 750\mu\text{V}$  FOR  $T_A < 125^\circ\text{C}$ .  
 OUTPUT VOLTAGE NOISE =  $128\text{nV}/\sqrt{\text{Hz}}$  AT  $1\text{kHz}$  (GAIN = 20).  
 $C_1 = C_T = 100\text{pF}$  TO  $5000\text{pF}$ ;  $R_4 \times C_2 > R_8 \times C_T$ .

Figure 108. Low Noise Hydrophone Amplifier with DC Servo



$R_4 \times C_2 = R_5 \times C_3 > R_1 (1 + R_2/R_3) C_1$ .  
 OUTPUT =  $0.8\text{mV}/\text{pC} = 80\text{mV}/\text{g}$ .  
 DC OUTPUT  $\leq 1\text{mV}$  FOR  $T_A < 25^\circ\text{C}$ .  
 OUTPUT NOISE =  $6.6\text{nV}/\sqrt{\text{Hz}}$  AT  $1\text{kHz}$ .

Figure 109. Accelerometer Amplifier with DC Servo

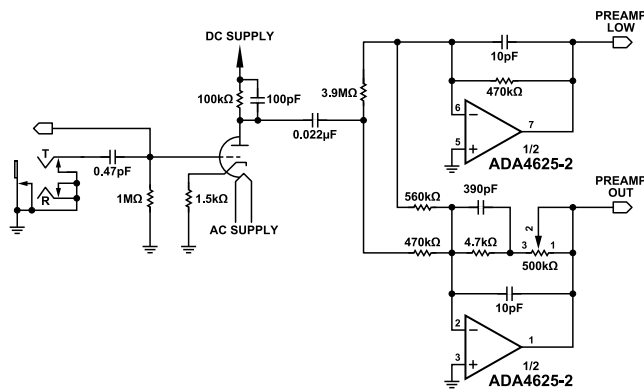
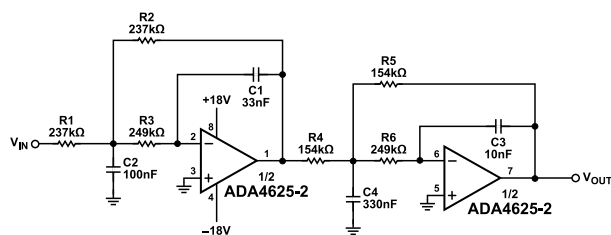


Figure 110. Guitar Preamp

## APPLICATIONS INFORMATION



TYPICAL OFFSET  $\approx 30\mu\text{V}$ .

1% TOLERANCES

$V_{\text{IN}} = 10\text{V p-p}$ ,  $V_{\text{OUT}} = -110\text{dB}$  AT  $f > 300\text{Hz}$

$V_{\text{OUT}} = -6\text{dB}$  AT  $f = 10\text{Hz}$

THE LOW INPUT BIAS CURRENTS ALLOW THE USE OF HIGH RESISTOR VALUES.

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Figure 111. 10 Hz Fourth-Order Chebyshev Low-Pass Filter (0.01 dB Ripple)

## OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RD-8-4	SOIC_N_EP	16-Lead Standard Small Outline Package

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADA4625-1ARDZ	-40°C to +125°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-4
ADA4625-1ARDZ-R7	-40°C to +125°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-4
ADA4625-1ARDZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-4
ADA4625-2ARDZ	-40°C to +125°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-4
ADA4625-2ARDZ-R7	-40°C to +125°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-4
ADA4625-2ARDZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-4

<sup>1</sup> Z = RoHS Compliant Part.

## EVALUATION BOARDS

Model <sup>1</sup>	Description
EVAL-ADA4625-1ARDZ	Evaluation Board
EVAL-ADA4625-2ARDZ	Evaluation Board

<sup>1</sup> Z = RoHS Compliant Part.