−2V to 50V Wide Input Voltage Range, 1.8MHz High Bandwidth, Current-Sense Amplifier with PWM Rejection and Gain 10V/V

FEATURES

- 1.8MHz small signal, −3dB bandwidth
- In-package Trim Core (DigiTrim™)
  - Precision without chopping and/or autozero
  - Typical ±0.30µV/°C offset drift
  - Maximum ±200µV voltage-offset over temperature range
  - Typical DC CMRR: 131dB
  - Typical AC CMRR at 50kHz: 97dB
- Wide common-mode input voltage range
  - −2V to +50V, continuous operation
  - −20V to +85V, continuous survival
- Initial gain: 10V/V
- Wide operating temperature range: −40°C to +125°C
- Bidirectional operation
- 2.9V to 5.5V power-supply operating range
- Available in an 8-lead MSOP package

APPLICATIONS

- In-phase or high-side current sensing in:
  - Motor control in BLDC motors, low-inductance motors
  - Bidirectional 48V to 12V DC to DC converters
  - Solenoid controls
  - Power rail monitoring
- Low-side current sensing

TYPICAL APPLICATION CIRCUIT

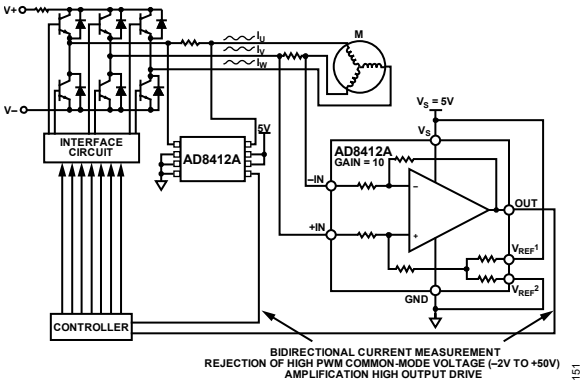

Figure 1. AD8412A in BLDC Motor Control Application

GENERAL DESCRIPTION

The AD8412A is a high voltage, high bandwidth current-sense amplifier. The device features an initial gain of 10V/V, with a 1.8MHz bandwidth with a maximum ±0.11% gain error over the entire temperature range. The buffered output voltage directly interfaces with any typical converter. The AD8412A has a minimum DC common-mode rejection ratio (CMRR) of 110dB from −2V to +50V. The AD8412A performs bidirectional current measurements across a shunt resistor in a variety of industrial and automotive applications.

The AD8412A offers breakthrough performance throughout the −40°C to +125°C temperature range. The device features an in-package trim core, which leads to a typical offset drift of ±0.30µV/°C (based on box method, as in *Figure 56*) throughout the operating temperature range and the common-mode voltage range without the need for chopping and autozero clocks (which can lead to intermodulation in the application). The device includes circuitry to achieve a wide input common-mode range and balanced input bias currents, regardless of input differential voltage or common-mode voltage, and circuitry to achieve ultralow CMRR drift. The device also includes circuitry to enable output accuracy in the presence of pulse-width modulation (PWM) type input common-mode voltages. The AD8412A is available in an 8-lead, MSOP package.

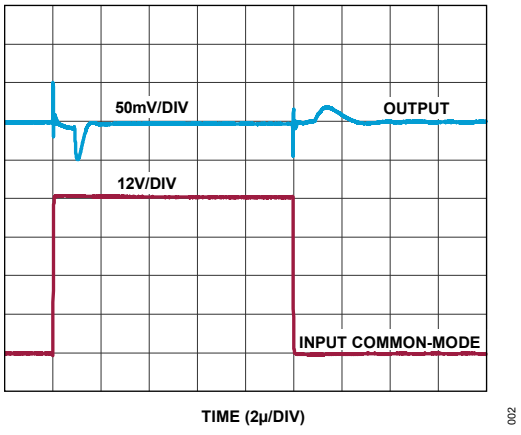

Figure 2. Input Common-Mode Step Response (0V to 48V), V_S = 5V, Inputs Shorted

−2V to 50V Wide Input Voltage Range, 1.8MHz High Bandwidth, Current-Sense Amplifier with PWM Rejection and Gain 10V/V

FUNCTIONAL BLOCK DIAGRAM

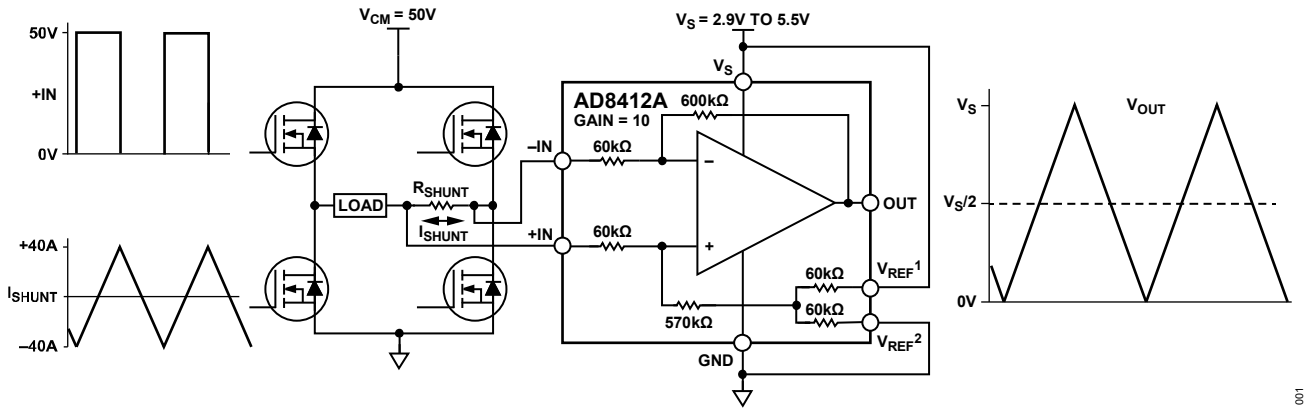

Figure 3. Functional Block Diagram

REVISION HISTORY

Initial release – Rev. 0; 01/25

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = −40°C to +125°C (operating temperature range), supply voltage (V_S) = 5V, ground (GND) = 0V, input common-mode voltage (V_{CM}) = −IN, +IN = 12V, and $V_{REF}1 = V_{REF}2$ = 2.5V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GAIN					
Initial			10		V/V
Error Over Temperature	Specified temperature range			0.11	%
Initial Gain vs. Temperature				±2.7	ppm/°C
VOLTAGE OFFSET, Referred to Input (RTI)					
Over Temperature	Specified temperature range[1]			±200	µV
Offset Drift	Box method (see *Figure 56*)		±0.30	±0.87	µV/°C
	Bowtie method (-40°C to 25°C) (see *Figure 57*)			±2.07	µV/°C
	Bowtie method (25°C to 125°C) (see *Figure 57*)			±1.68	µV/°C
INPUT					
Total Input-Bias Current[2]	+IN = −IN = 0V, $V_S = V_{REF}1$ = 5V, $V_{REF}2$ = 0V	−10.0			µA
	+IN = −IN = 12V, $V_S = V_{REF}1 = V_{REF}2$ = 0V, T_A = 25°C		47		µA
	+IN = −IN = 12V, $V_S = V_{REF}1$ = 5V, $V_{REF}2$ = 0V			350	µA
	+IN = −IN = 50V, $V_S = V_{REF}1 = V_{REF}2$ = 0V, T_A = 25°C		196		µA
	+IN = −IN = 50V, $V_S = V_{REF}1$ = 5V, $V_{REF}2$ = 0V			484	µA
Input Offset Current	+IN = −IN = 0V			1.0	µA
	+IN = −IN = 12V			2.5	µA
	+IN = −IN = 50V			2.7	µA
Input Voltage Range	Common-mode, continuous	−2		+50	V
Common-Mode Rejection Ratio (CMRR)	Specified temperature range, DC, V_{CM} = −2V to +50V	110	131		dB
	T_A = 25°C, frequency = 10kHz		111		dB
	T_A = 25°C, frequency = 50kHz		97		dB
OUTPUT					
Voltage Swing to GND (OUT - GND)	Load resistance (R_L) = 10kΩ			5	mV
Voltage Swing to V_S (V_S − OUT)	Load resistance (R_L) = 10kΩ			16	mV

(T_A = −40°C to +125°C (operating temperature range), supply voltage (V_S) = 5V, ground (GND) = 0V, input common-mode voltage (V_{CM}) = −IN, +IN = 12V, and V_{REF}^1 = V_{REF}^2 = 2.5V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Resistance	T_A = 25°C		0.2		Ω
Maximum Capacitive-Load	No continuous oscillation, T_A = 25°C		4.7		nF
DYNAMIC RESPONSE					
Small Signal, −3dB Bandwidth	T_A = 25°C		1.8		MHz
Slew Rate	T_A = 25°C		6		V/µs
NOISE					
0.1Hz to 10Hz (RTI)	T_A = 25°C		10		µV p-p
Spectral Density, 1kHz (RTI)	T_A = 25°C		64		nV/√Hz
Spectral Density, 10kHz (RTI)	T_A = 25°C		52		nV/√Hz
OFFSET ADJUSTMENT					
Ratiometric Accuracy[3]	V_{REF} pins divider to supply	0.499		0.501	V/V
Accuracy, Referred to the Output (RTO)	V_{REF} error when using an external reference of 2.5V applied to V_{REF}^1 and V_{REF}^2 in parallel.			±1	mV/V
V_{REF}^1 Input Voltage Range		GND		V_S	V
V_{REF}^2 Divider Resistor Values			60		kΩ
POWER SUPPLY					
Operating Voltage Range		2.9		5.5	V
Quiescent Current	Output voltage (V_{OUT}) = 2.5V DC, T_A = 25°C		7.8		mA
	V_{OUT} = 2.5V DC			10.8	mA
Power Supply Rejection Ratio (PSRR)	V_S from 3V to 5V, specified temperature range	87	106		dB
TEMPERATURE RANGE					
For Specified Performance	Operating temperature range	−40		+125	°C

1 Guaranteed by test and characterization

2 To see input bias current per pin, see *Figure 14* and *Figure 15.*

3 The offset adjustment is ratiometric to the power supply when V_{REF}^1 and V_{REF}^2 are used as dividers between the supplies.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Supply Voltage (V_S to GND)	6V
Input Voltage Range, Continuous	
Common-Mode	
+IN to GND	−20V to +85V
−IN to GND	−20V to +85V
Differential	
+IN to −IN	± 20V
V_{REF}^1, V_{REF}^2	GND − 0.3 V to V_S + 0.3 V
Reverse Supply Voltage	0.3V
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Output Short-Circuit Duration	Indefinite

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JB} is the junction-to-board thermal resistance. θ_{JCT} is the junction-to-case thermal resistance.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JB}	θ_{JCT}	Unit
RM-8	152	120.6	59.7	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board for θ_{JA}, JEDEC 2S2P thermal impedance with ring style cold plate attached to PCB for θ_{JB}, and a JEDEC 1S0P thermal test board for θ_{JCT}. Refer to JEDEC JESD-51.

Electrostatic Discharge (ESD) RATINGS

Table 4. AD8412A, 8-Leads MSOP

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±750	C2B

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

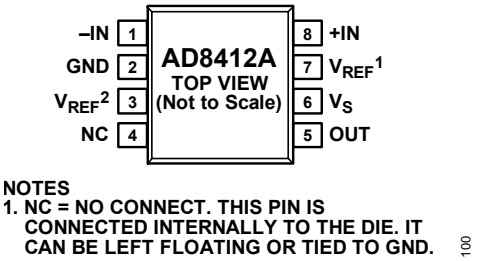

Figure 4. 8-Lead MSOP Configuration

Table 5. Pin Descriptions

PIN	NAME	DESCRIPTION
1	−IN	Negative Input
2	GND	Ground
3	V_{REF}^2	Reference Input 2
4	NC	No Connect. This pin is connected internally to the die. It can be left floating or tied to GND.
5	OUT	Output
6	V_S	Supply Voltage
7	V_{REF}^1	Reference Input 1
8	+IN	Positive Input

TYPICAL PERFORMANCE CHARACTERISTICS

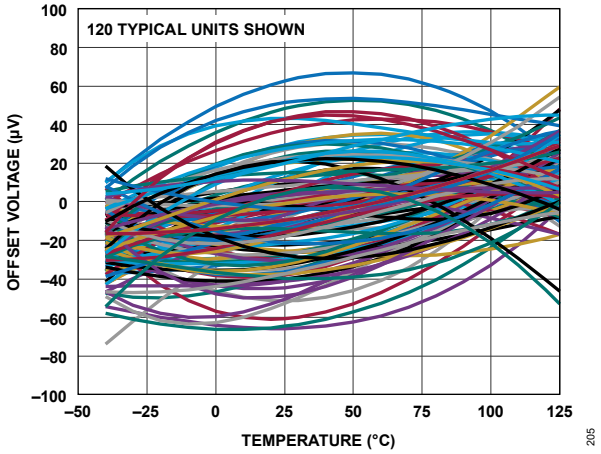

Figure 5. Offset Voltage vs. Temperature

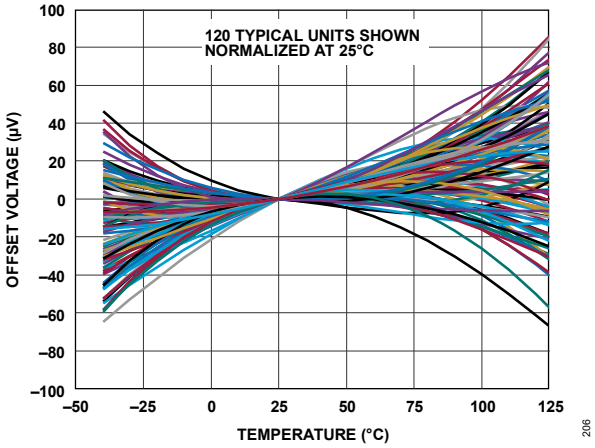

Figure 6. Offset Voltage vs. Temperature, Normalize at 25°C

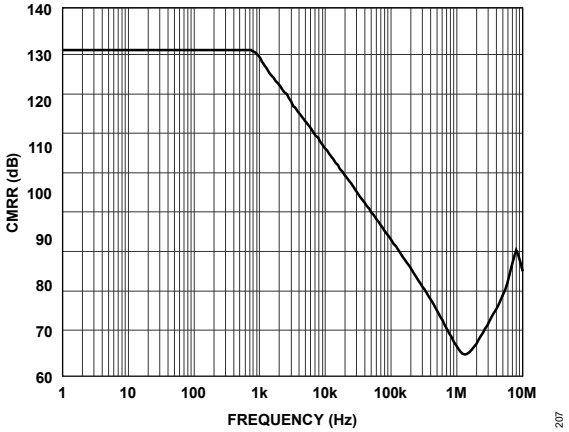

Figure 7. CMRR vs. Frequency

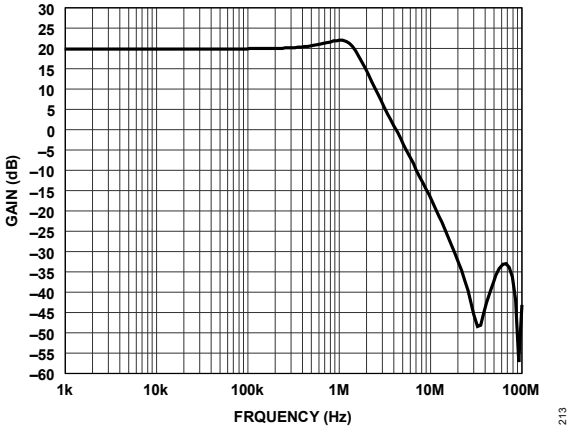

Figure 8. Typical Small Signal Bandwidth, V_{OUT} = 200mVp-p

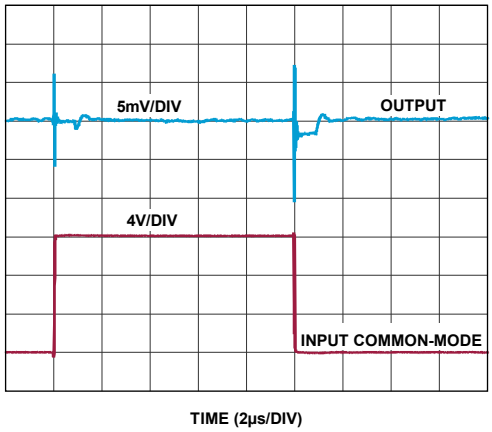

Figure 9. Input Common-Mode Step Response (0V to 12V), V_s = 5V, Inputs Shorted

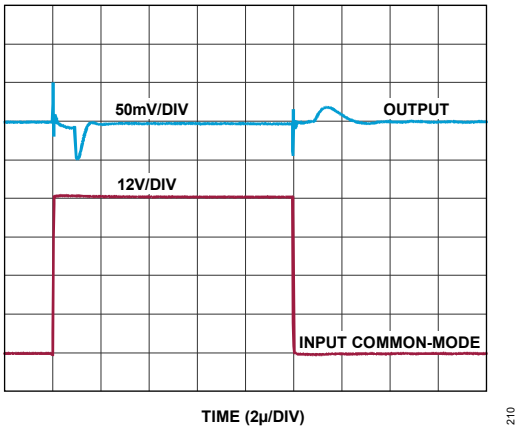

Figure 10. Input Common-Mode Step Response (0V to 48V), V_s = 5V, Inputs Shorted

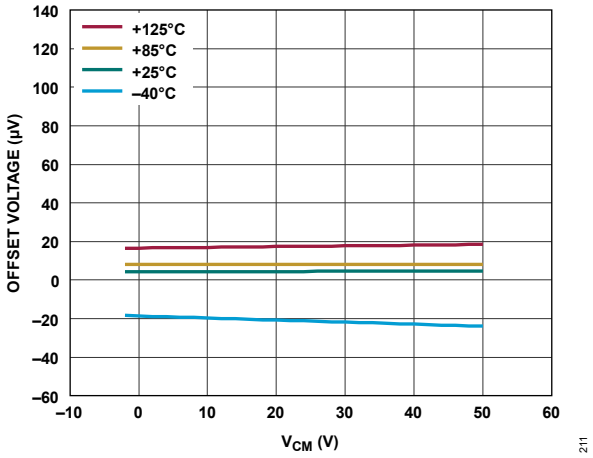

Figure 11. Offset Voltage vs. Common-Mode Voltage

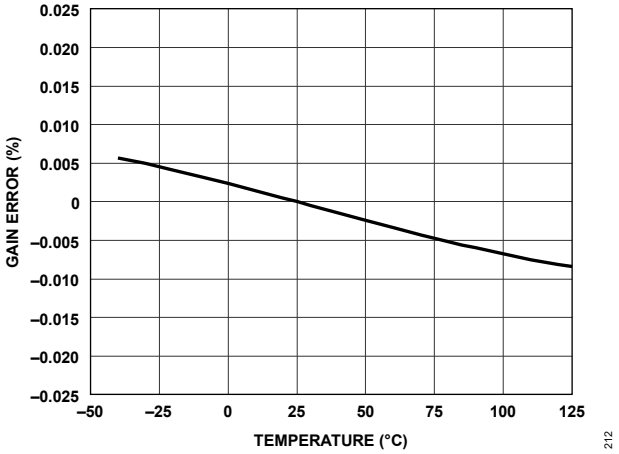

Figure 12. Gain Error vs. Temperature

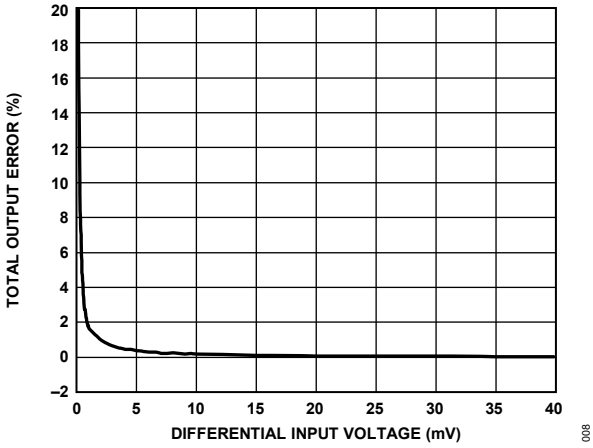

Figure 13. Total Output Error vs. Differential Input Voltage

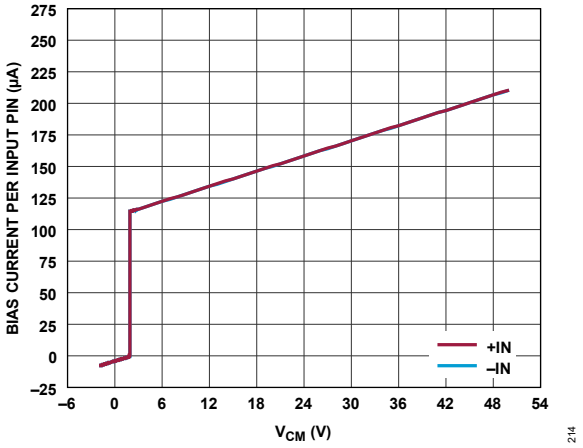

Figure 14. Bias Current per Input Pin vs. V_{CM}, V_S = 5V

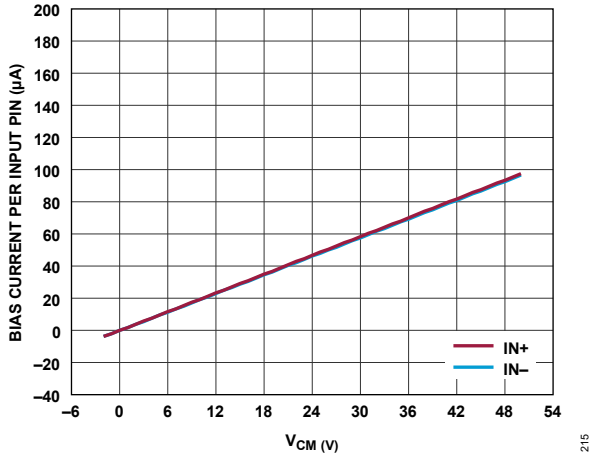

Figure 15. Bias Current per Input Pin vs. V_{CM}, V_S = 0V, R_L = 10kΩ

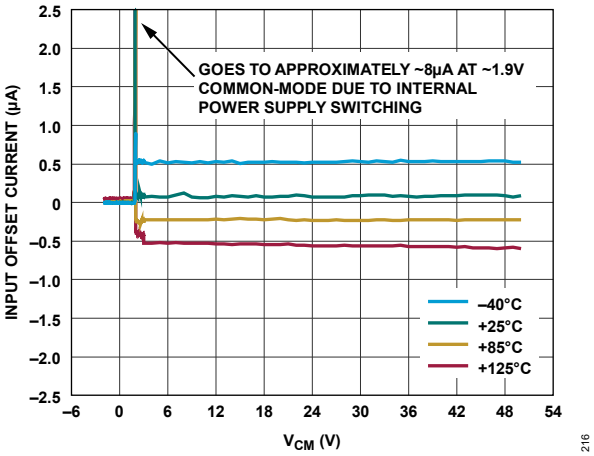

Figure 16. Input Offset Current vs. V_{CM} at Various Temperatures

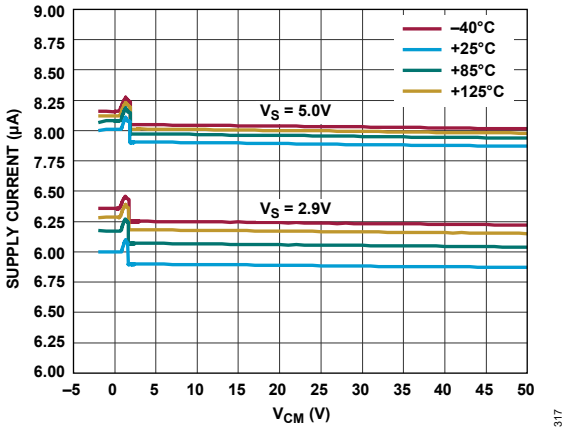

Figure 17. Supply Current vs. Input V_{CM} at Various Temperatures and Supply Voltages

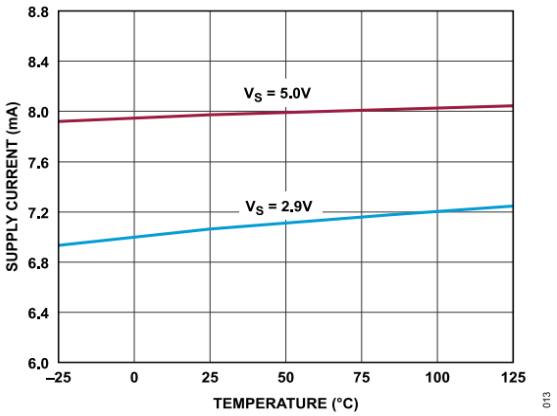

Figure 18. Supply Current vs. Temperature at Various Supply Voltages

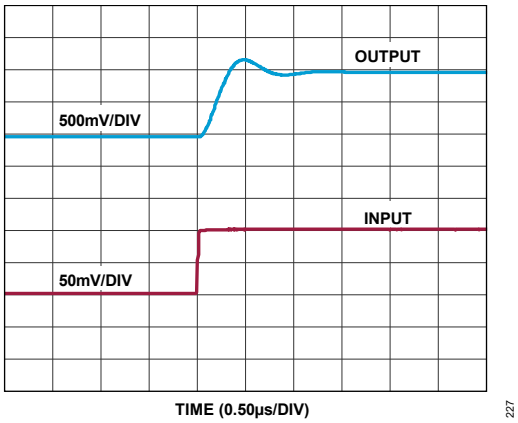

Figure 19. Rise Time, V_S = 2.9V

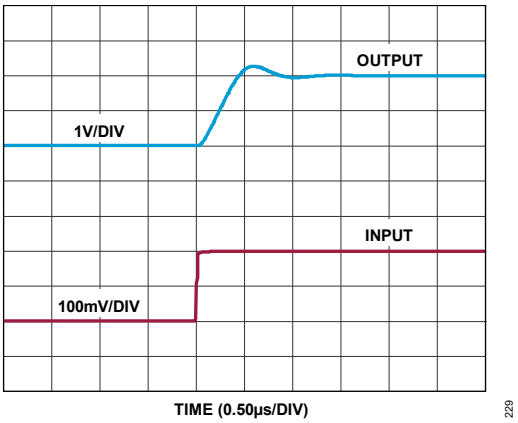

Figure 20. Rise Time, V_S = 5V

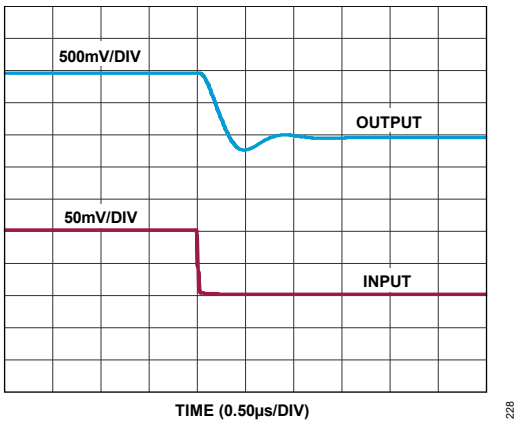

Figure 21. Fall Time, V_S = 2.9V

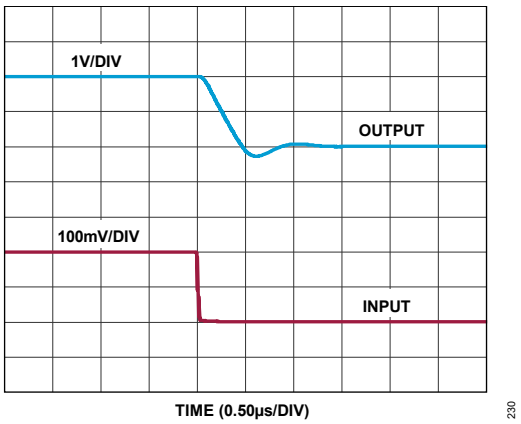

Figure 22. Fall Time, V_S = 5V

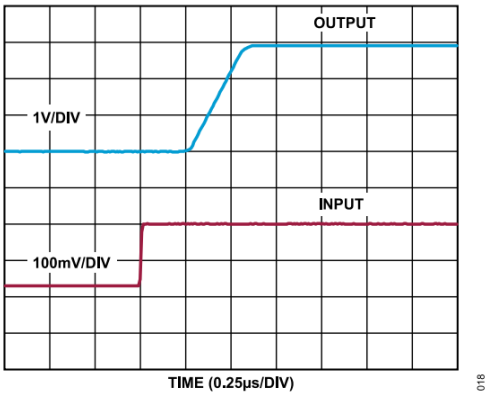

Figure 23. Differential Overload Recovery, Rising, V_S = 2.9V

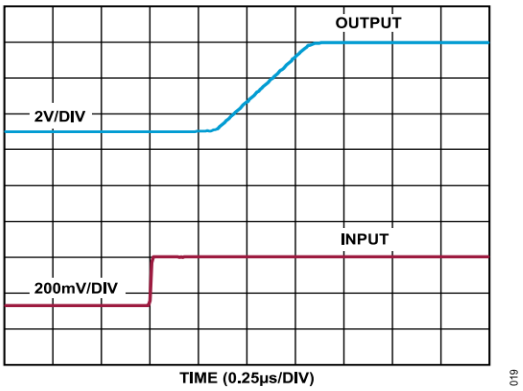

Figure 24. Differential Overload Recovery, Rising, V_S = 5V

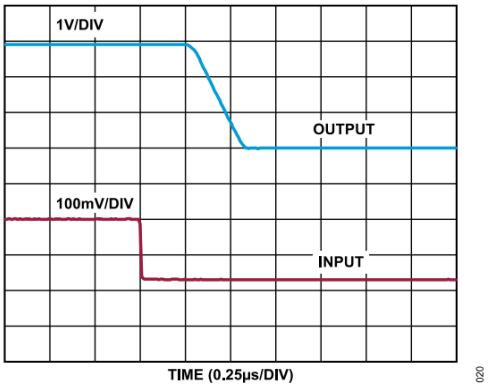

Figure 25. Differential Overload Recovery, Falling, V_S = 2.9V

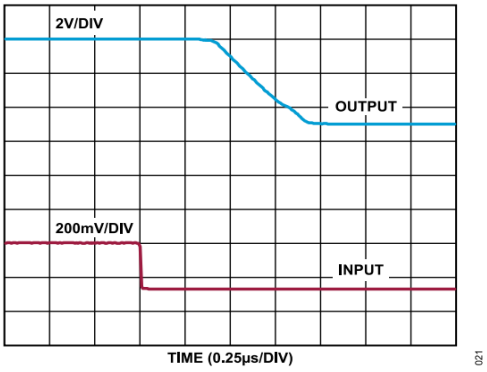

Figure 26. Differential Overload Recovery, Falling, V_S = 5V

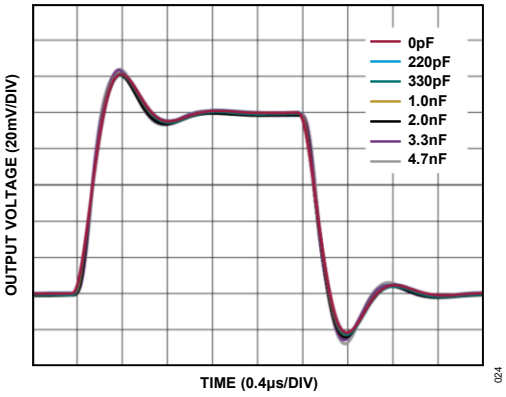

Figure 27. Small Signal Response for Various Capacitive Loads

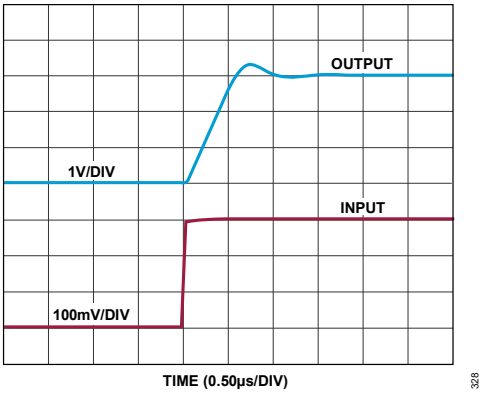

Figure 28. Large Signal Response, Rising, V_S = 5V

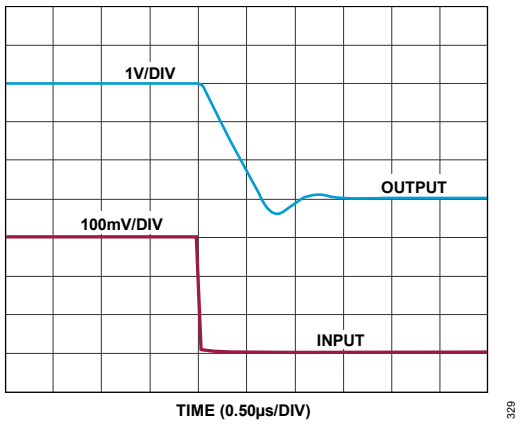

Figure 29. Large Signal Response, Falling, V_S = 5V

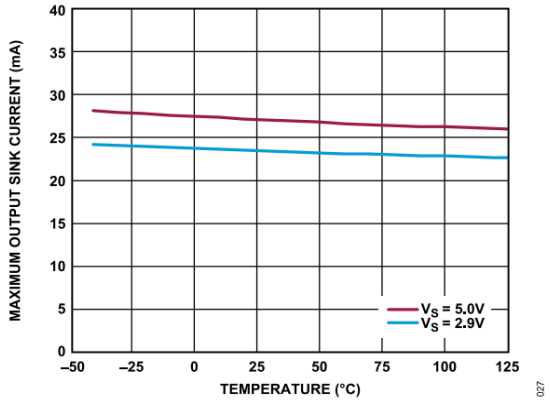

Figure 30. Maximum Output Sink Current vs. Temperature at Various Supply Voltages

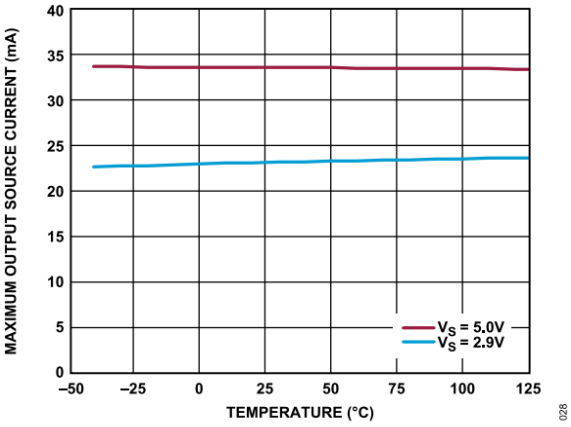

Figure 31. Maximum Output Source Current vs. Temperature at Various Supply Voltages

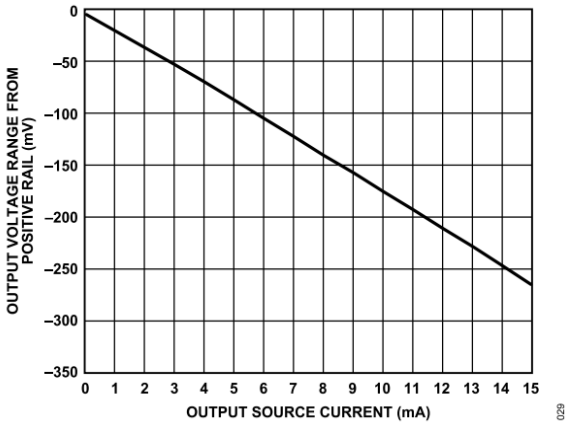

Figure 32. Output Voltage Range from Positive Rail vs. Output Source Current

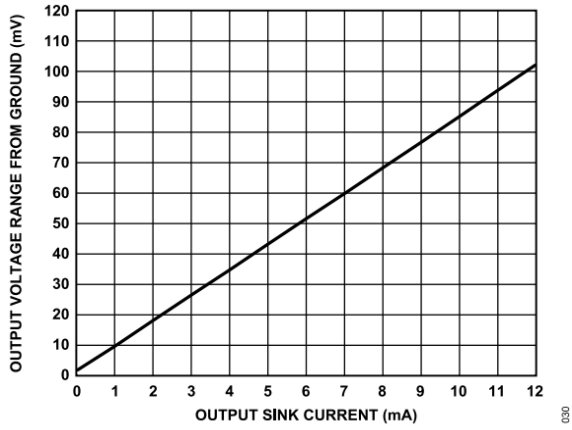

Figure 33. Output Voltage Range from Ground vs. Output Sink Current

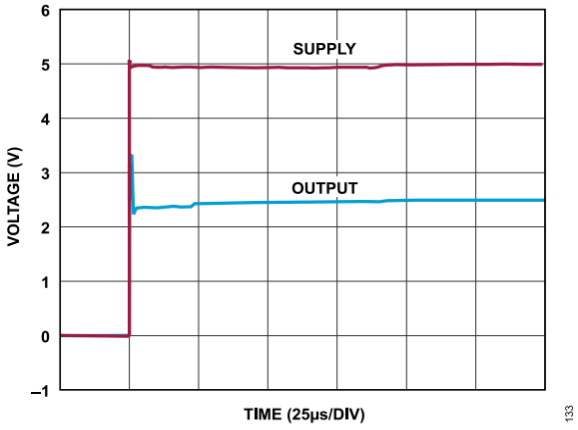

Figure 34. Startup Response

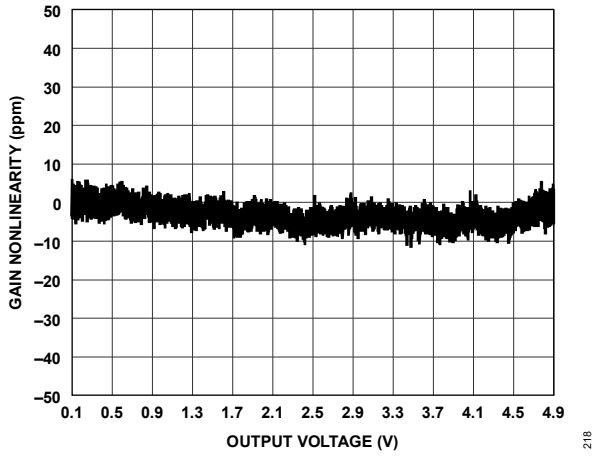

Figure 35. Gain Nonlinearity vs. Output Voltage, V_S = 5V

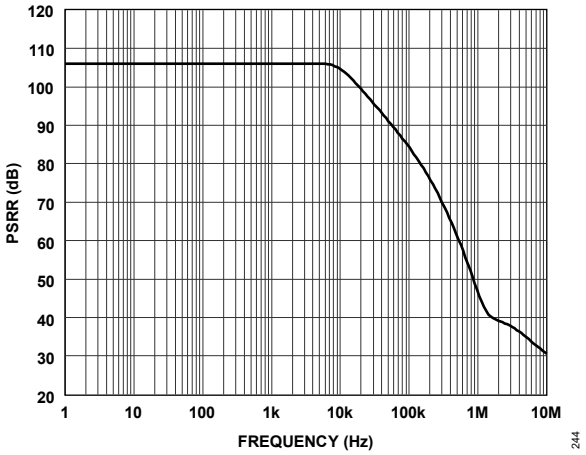

Figure 36. PSRR vs. Frequency

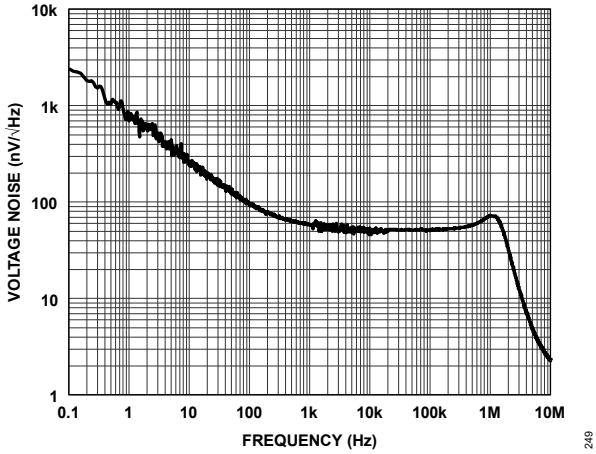

Figure 37. Spectral Density, RTI

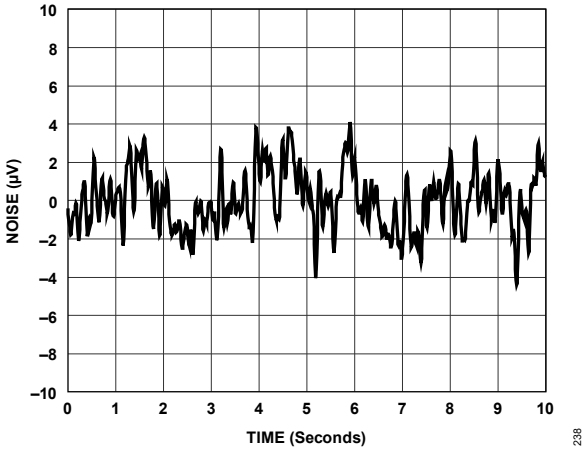

Figure 38. 0.1Hz to 10Hz Noise, RTI

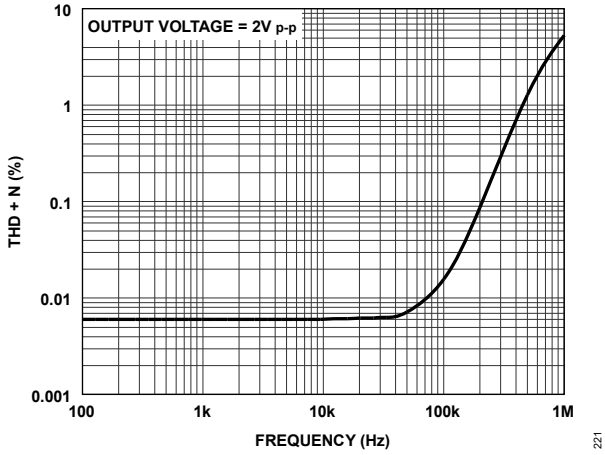

Figure 39. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

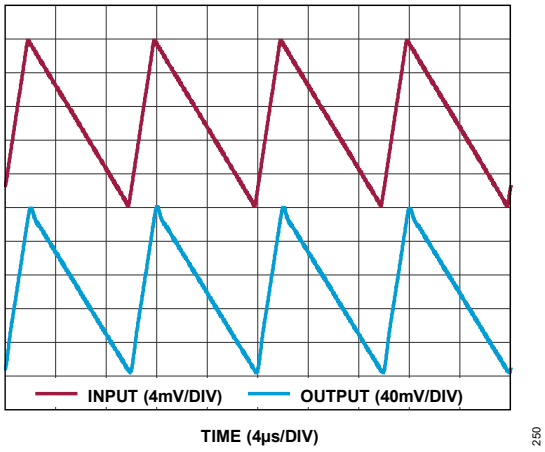

Figure 40. Output Response for 100kHz, 20% Duty-Cycle, Sawtooth Waveform, Input Voltage (V_{IN}) = 10mVp-p

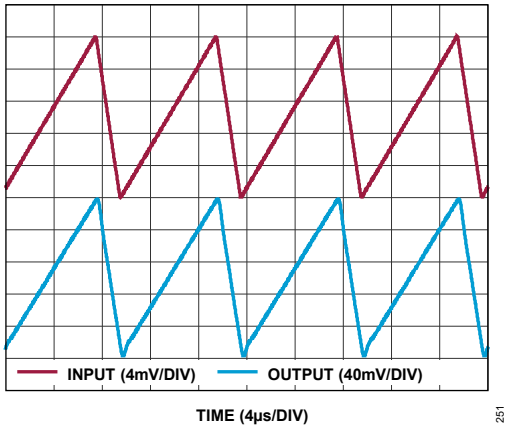

Figure 41. Output Response for 100kHz, 80% Duty-Cycle, Sawtooth Waveform, Input Voltage (V_{IN}) = 10mVp-p

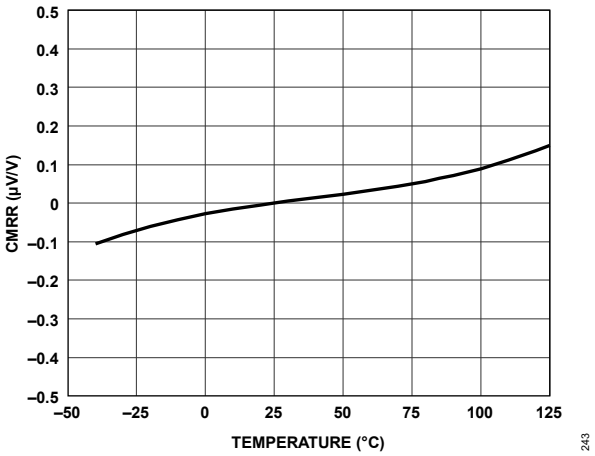

Figure 42. CMRR vs. Temperature

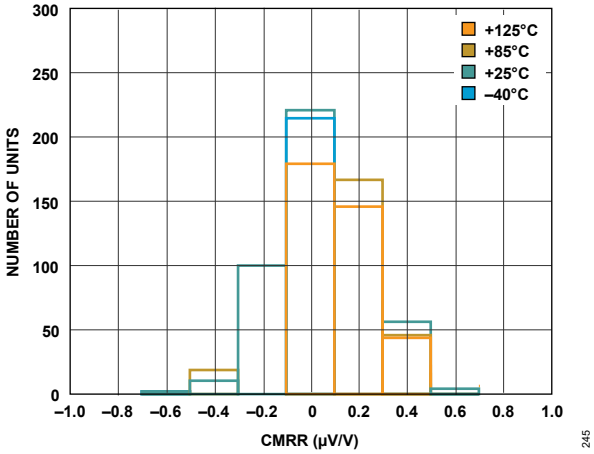

Figure 43. CMRR Distribution

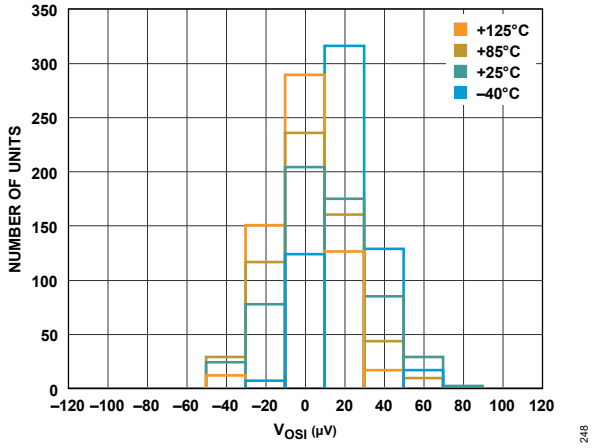

Figure 44. Offset Voltage (V_{OS}) Distribution, RTI

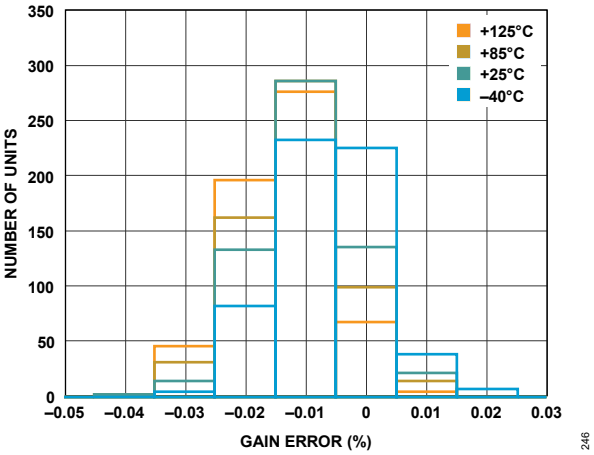

Figure 45. Gain Error Distribution

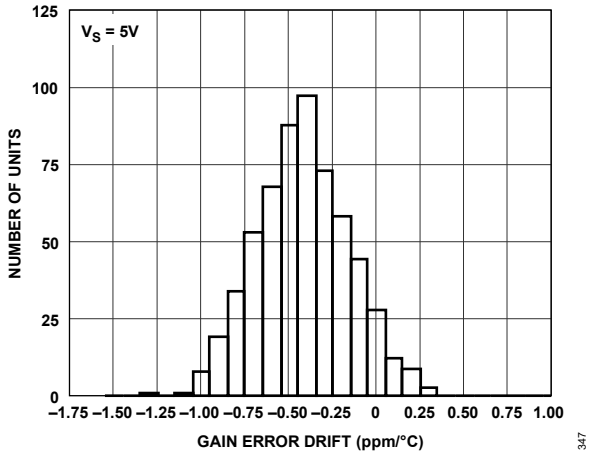

Figure 46. Gain Error Drift Distribution

THEORY OF OPERATION

The AD8412A is a wide input voltage range, high bandwidth, current-sense amplifier with pulse-width modulation (PWM) rejection that uses a unique architecture to accurately amplify the small differential current shunt voltages in the presence of rapidly changing common-mode voltages.

In typical applications, the AD8412A measures the current by amplifying the voltage across a shunt resistor connected to the inputs by a gain of 10V/V (see *Figure 47*).

The AD8412A design provides excellent common-mode rejection, even with PWM common-mode inputs that can change at fast rates, such as 1V/ns. The AD8412A has internal deglitch circuitry to reduce the negative effects (such as the amplitude and settling time) of the output response in the presence of common-mode PWM input signals typically found in the applications for current-sense amplifiers. When there is a large common-mode transient at the input of the AD8412A, the output of the AD8412A is held at the last value for about 1µs. This allows the change in the amplitude of the output of the AD8412A after a V_{CM} step to remain low and undisturbed. After the typical 1µs deglitch time, the output begins to settle to the appropriate value based on the differential voltage across the shunt resistor at the inputs (see *Figure 9* and *Figure 10*).

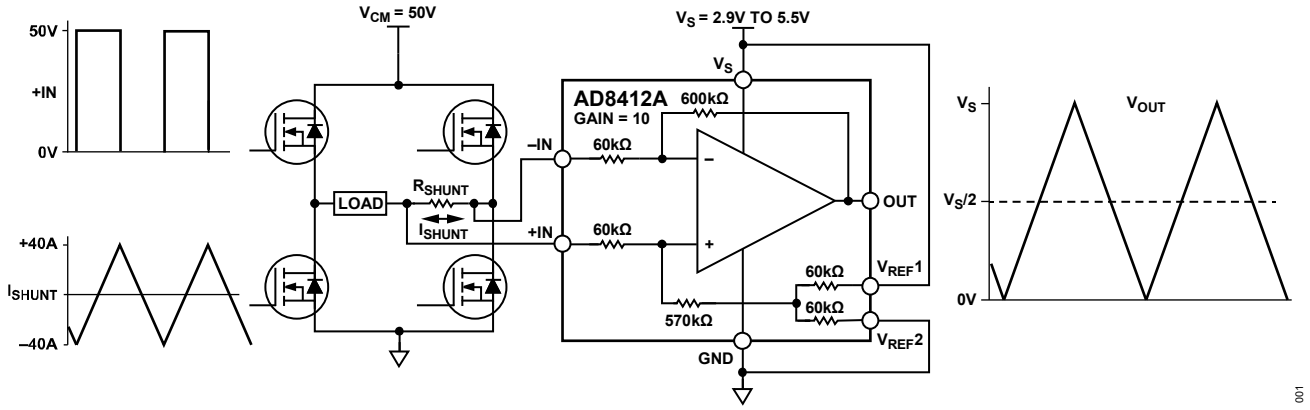

Figure 47. Typical Application

The AD8412A features an in-package trim core, which leads to a typical offset drift of ±0.30µV/°C throughout the operating temperature range and the common-mode voltage range without the need for chopping and autozero clocks (which can lead to intermodulation in the application). This architecture does not compromise bandwidth, which is typically rated at 1.8MHz.

The reference input pins, V_{REF}^1 and V_{REF}^2, are tied through 60kΩ resistors to the positive input of the main amplifier, which allows the output offset to be adjusted anywhere in the output operating range. The gain is 1V/V from the reference pins to the output when the reference pins are used in parallel. When the reference pins are used to divide the supply, the gain is 0.5V/V.

The AD8412A offers breakthrough performance without compromising the robust application needs typical of solenoid control, motor control, or DC to DC converters. The ability to reject PWM input common-mode voltages, and the DigiTrim architecture providing low offset and offset drift, allows the AD8412A to deliver total accuracy for these demanding applications.

CURRENT-SENSE LAYOUT GUIDELINES

Choosing a Shunt Resistor

There are different factors to consider in selecting the appropriate shunt resistor, including the resistor value, size, cost, tolerance, power dissipation, and thermal drift.

Commonly, the resistor value is selected based on the desired maximum differential voltage generated at the highest expected current, while considering the power loss budget. Another consideration is to ensure the output is maximized at full-scale current, taking full advantage of the available system dynamic range. Choosing the shunt resistor, R_{SHUNT}, value is often a compromise between these two considerations.

$$R_{SHUNT} = \frac{V_{DIFF,MAX}}{I_{MAX}} \quad (1)$$

The shunt resistor tolerance directly affects the accuracy of the overall gain error of the current measurement. The AD8412A is specified to have a maximum gain error of 0.11% over the specified temperature range from −40°C to +125°C. For optimal performance, select a 0.1% shunt resistor (or with lower tolerance) that does not introduce more gain error than the AD8412A.

The power dissipation in the shunt resistor is calculated using the equation: $P = I^2R$. Thus, a higher resistance results in higher power dissipation. Power dissipation in the shunt resistor leads to self heating, resulting in an increase in the temperature of the shunt resistor. Any change in shunt resistor temperature due to self-heating can result in a nonlinear error. Selecting a shunt resistor with a low temperature coefficient minimizes any self-heating of the shunt and minimizes any thermal nonlinearities.

The thermal drift of the voltage developed across the shunt resistor varies in relationship to the power dissipated by the resistor.

Shunt Resistor Connection

The shunt resistor, R_{SHUNT}, is connected between the input pins of the current-sense amplifier, which is shown in *Figure 48.* Typically, the shunt resistor has very low resistance. Thus, it is recommended to use a Kelvin (4-wire) connection on the shunt to achieve high accuracy current-sense measurement. A proper Kelvin connection avoids sensing across any parasitic PCB trace resistance.

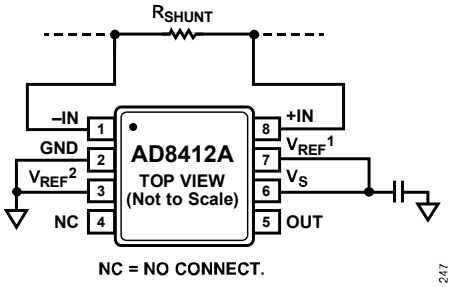

Figure 48. Shunt Resistor Layout

There are different ways to make the Kelvin connection to the R_{SHUNT} resistor. *Figure 49* shows a test board of five different layouts to verify the best layout to optimize high-current sensing accuracy. Based on the *Analog Dialogue* article, "Optimize High-Current Sensing Accuracy by Improving Pad Layout of LowValue Shunt Resistors" (Volume 46, June 2012), the sense points must be considered by placing them at the outer extremity of the resistor. The article shows that it was experimentally determined that the layouts with the lowest errors were Style C and Style D. Layout Style C is preferred because component placement tolerance issues are less likely to arise. Without a Kelvin

connection, measuring on the top pad, there is about a 22.8% error. Therefore, it is better to use a Kelvin connection when using a low-value R_{SHUNT} to obtain more accurate current-sense measurements.

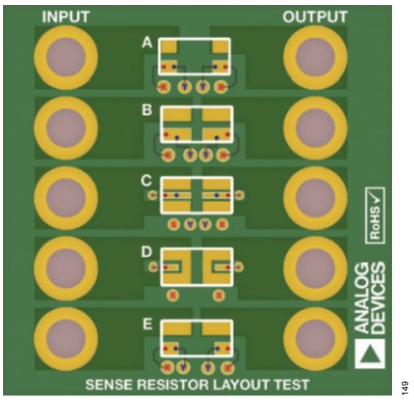

Figure 49. Sample R_{SHUNT} Layout Board

OUTPUT OFFSET ADJUSTMENT

The output of the AD8412A can be adjusted for unidirectional or bidirectional operation.

Unidirectional Operation

Unidirectional operation allows the AD8412A to measure currents through a resistive shunt in one direction. The basic modes for unidirectional operation are ground referenced output mode and V_S referenced output mode.

For unidirectional operation, the output can be set at the negative rail (near ground) or at the positive rail (near V_S) when the differential input is 0V. The output moves to the opposite rail when a correct polarity differential input voltage is applied. The required polarity of the differential input depends on the output voltage setting. If the output is set at the positive rail, the input polarity must be negative to decrease the output. If the output is set at ground, the polarity must be positive to increase the output.

Ground Referenced Output Mode

When using the AD8412A in ground referenced output mode, both referenced inputs are tied to the GND pin, which causes the output to sit at the negative rail when there are zero differential volts at the input (see *Figure 50*).

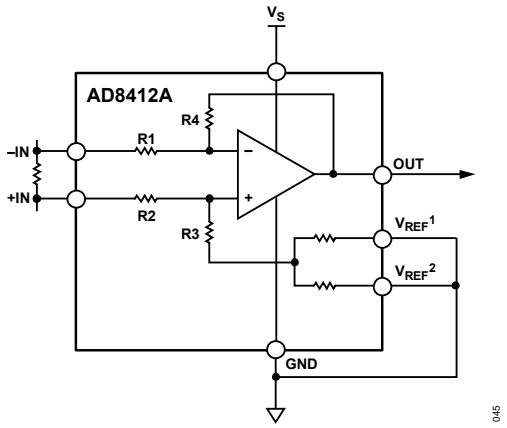

Figure 50. Ground Referenced Output

V_S Referenced Output Mode

V_S referenced output mode is set when both reference pins are tied to the positive supply. This mode is typically used when the diagnostic scheme requires detection of the amplifier and the wiring before power is applied to the load (see *Figure 51*).

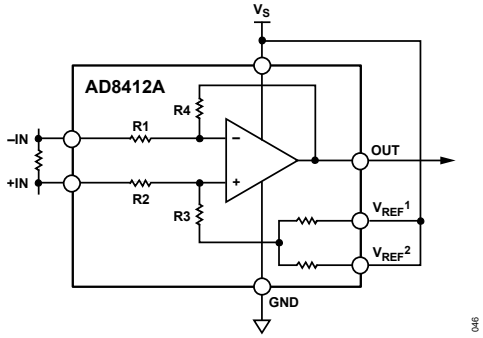

Figure 51. V_S Referenced Output

Bidirectional Operation

Bidirectional operation allows the AD8412A to measure the currents through a resistive shunt in two directions.

In this case, the output is set anywhere within the output range. Typically, the output is set at half-scale for an equal range in both directions. In some cases, however, the output is set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

Adjusting the output is accomplished by applying DC voltage to the reference inputs. $V_{REF}1$ and $V_{REF}2$ are tied to internal resistors that connect to an internal node. There is no operational difference between the reference pins.

External Referenced Output

Tie $V_{REF}1$ and $V_{REF}2$ together and to a reference to produce an output equal to the reference voltage when there is no differential input (see *Figure 52*). The output decreases with respect to the reference voltage when the input is negative, relative to the −IN pin, and increases when the input is positive, relative to the −IN pin.

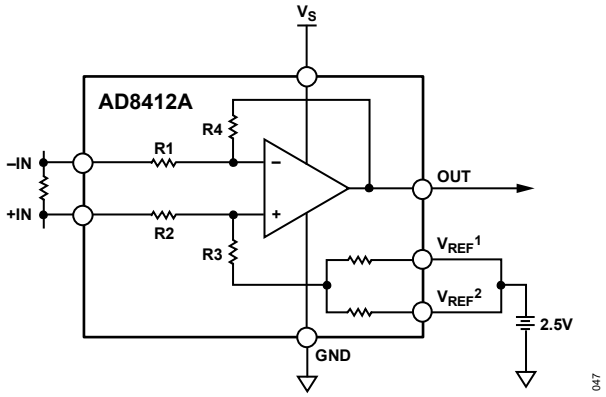

Figure 52. External Referenced Output

Splitting the Supply

By tying one reference pin to the V_S pin and the other reference pin to the GND pin, the output is set at half of the supply when there is no differential input (see *Figure 53*). The benefit of this configuration is that an external reference is not required to offset the output for bidirectional current measurement. Tying one reference pin to the V_S pin and the other reference pin to the GND pin creates a midscale offset ratiometric to the supply, which means if the supply increases or decreases, the output remains at half the supply. For example, if the supply is 5.0V, the output is at half-scale or 2.5V. If the supply increases by 10% (to 5.5V), the output increases to 2.75V.

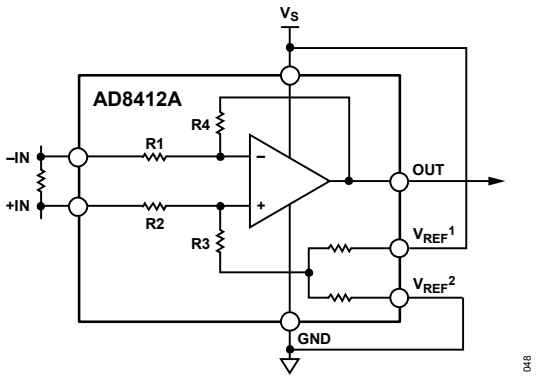

Figure 53. Split Supply

Splitting an External Reference

Use the internal reference resistors to divide an external reference by two with an accuracy of approximately 0.5%. Split an external reference by connecting one V_{REF}^X pin to the GND pin and the other V_{REF}^X pin to the reference voltage (see *Figure 54*).

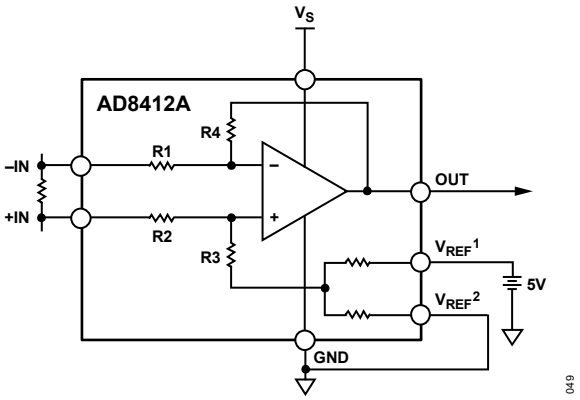

Figure 54. Split External Reference

OFFSET VOLTAGE TERMINOLOGY

Box Method

The AD8412A features an in-package trim core, which leads to a typical offset drift of ±0.30µV/°C (using the box method) throughout the operating temperature range and the common-mode voltage range. This architecture does not compromise bandwidth, but the offset voltage drift signatures for the AD8412A vary part-to-part, as shown in *Figure 55*. After observing the minimum and maximum value for V_{OS} over the full temperature range from −40°C to 125°C, the V_{OS} drift in µV/°C is calculated for each part using the box method.

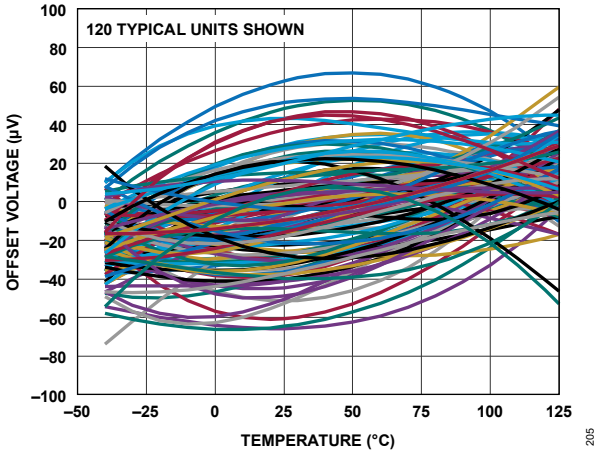

Figure 55. Offset Voltage vs. Temperature

A visual representation of this box method calculation and the mean value for the V_{OS} drift using the box method is shown in *Figure 56*. Based on the mean (typ) value of ±0.30 µV/°C and the standard deviation of the box method drift of the 360 parts, calculate a value (see Equation 2) for a guaranteed V_{OS} drift by characterization, ±0.87µV/°C.

$$\pm\text{MAX}(\text{ABS}(\text{mean} \pm 5 \times (\text{standard deviation}))) \quad (2)$$

This is valid from the −40°C to 125°C temperature range.

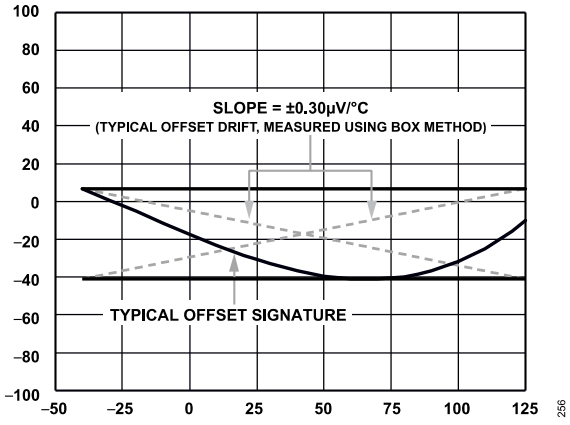

Figure 56. Box Method

Bowtie Method

Typically, in applications where the AD8412A is used, a calibration is done at +25°C. If a single-point calibration at +25°C is done, this creates a plot shown in *Figure 57*. For each part, the slope of the line from −40°C to +25°C and the slope from +25°C to +125°C are calculated. The mean and standard deviation for the slope of all the parts from

−40°C to +25°C are then calculated. The V_{OS} maximum drift of ±2.07µV/°C using the bowtie method is then calculated using Equation 2. The mean and standard deviation for the slope of all the parts from +25°C to +125°C is then calculated. The V_{OS} maximum drift of 1.68µV/°C using the bowtie method is then calculated using Equation 2. The red lines in *Figure 57* represent the worst-case V_{OS} drift slopes using the bowtie method that a user can guarantee through characterization. Calibrating at +25°C allows the maximum V_{OS} over the full temperature range to be reduced to ~±168V, as opposed to the ±200µV listed in the *Specifications* section as the maximum V_{OS} over temperature (with no calibration).

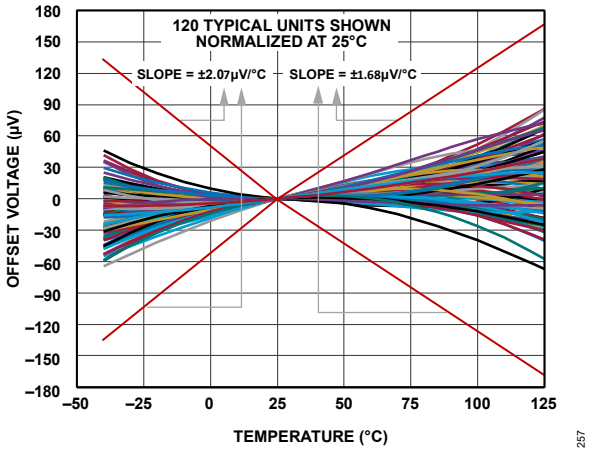

Figure 57. Bowtie Method

APPLICATIONS INFORMATION

Motor Control

Three-Phase Motor Control

The AD8412A is ideally suited for monitoring current in three-phase motor applications such as brushless DC motors. The 1.8MHz typical bandwidth of the AD8412A provides instantaneous current monitoring. Additionally, the typical low offset drift of ±0.30µV/°C means the measurement error between the two motor phases is at a minimum over temperature. The AD8412A rejects PWM input common-mode voltages in the −2V to +50V range. Monitoring the current on the motor phase allows sampling of the current at any point and provides diagnostic information, such as a short to ground and battery. The DigiTrim architecture used in the AD8412A provides precision specifications without the need for chopping and/or autozeroing. The DigiTrim architecture of the AD8412A avoids the potential for intermodulation distortion, which is observed when using amplifiers with chopping/autozero architectures. For the typical phase current measurement setup with the AD8412A, see *Figure 58*.

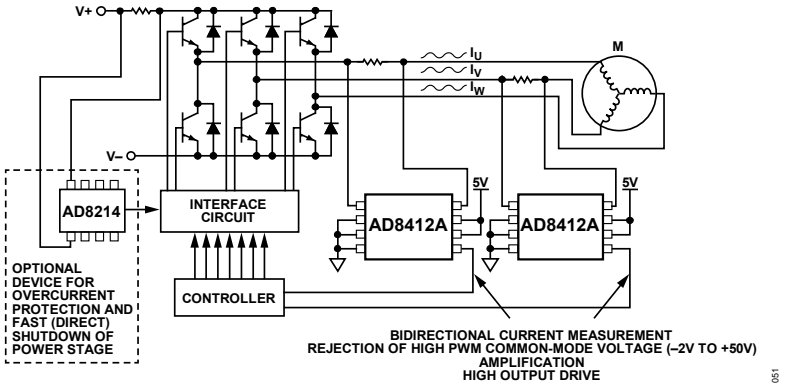

Figure 58. Three-Phase Motor Control

H-Bridge Motor Control

Another typical application for the AD8412A is to form part of the control loop in H-bridge motor control. In this case, place the shunt resistor in the middle of the H-bridge to accurately measure current in both directions by using the shunt available at the motor (see *Figure 59*). Using an amplifier and shunt in this location is a more accurate solution than a ground-referenced op amp because ground is not typically a stable reference voltage in this type of application. The instability of the ground reference causes inaccuracies in the measurements that can be made with a simple ground referenced op amp. The AD8412A measures current in both directions as the H-bridge switches and the motor change direction. The output of the AD8412A is configured in an external referenced bidirectional mode (see the *Bidirectional Operation* section).

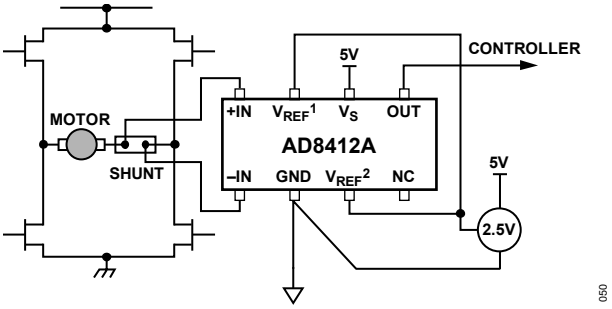

Figure 59. H-Bridge Motor Control

Solenoid Control

High-Side Current-Sense with a Low-Side Switch

In the case of a high-side current-sense with a low-side switch, the PWM control switch is ground referenced. Connect an inductive load (solenoid) to a power supply and place a resistive shunt between the switch and the load (see *Figure 60*). An advantage of placing the shunt on the high-side is that the entire current, including the recirculation current, is measurable because the shunt remains in the loop when the switch is off. In addition, diagnostics are enhanced because shorts to ground are detected with the shunt on the high-side.

In this circuit configuration, when the switch is closed, the common-mode voltage decreases to near the negative rail. When the switch is open, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop above the battery by the clamp diode.

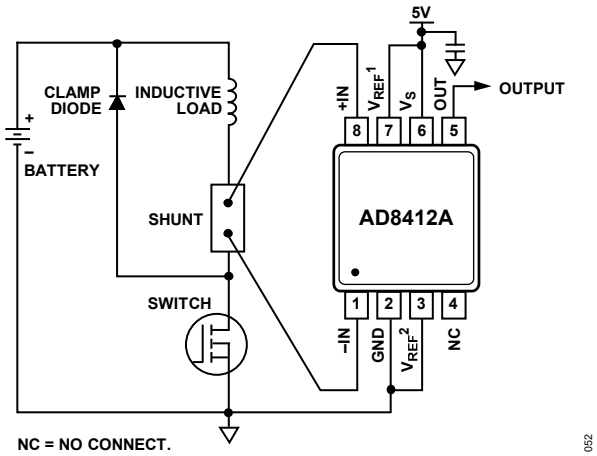

Figure 60. Low-Side Switch

High-Side Current-Sense with a High-Side Switch

The high-side current-sense with a high-side switch configuration minimizes the possibility of unexpected solenoid activation and excessive corrosion due to constant battery draw (see *Figure 61*). In this case, both the switch and the shunt are on the high-side. When the switch is off, the battery is removed from the load, which prevents damage from potential shorts to ground while still allowing the recirculating current to be measured and to provide diagnostics. Removing the power supply from the load for the majority of the time the switch is open minimizes the corrosive effects caused by the differential voltage between the load and ground.

When using a high-side switch, the battery voltage is connected to the load when the switch is closed, causing the common-mode voltage to increase to the same value as the battery voltage. In this case, when the switch is open, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop below ground by the clamp diode.

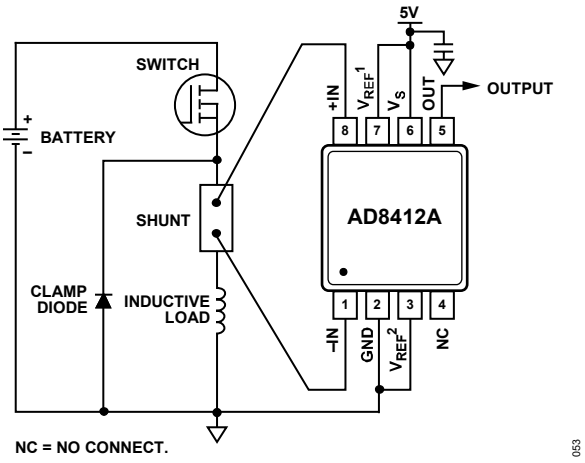

Figure 61. High-Side Switch

High Rail Current Sensing

In the high rail current sensing configuration, the shunt resistor is referenced to the battery. High voltage is present at the inputs of the current-sense amplifier. When the shunt is battery referenced, the AD8412A produces a linear ground-referenced analog output. Additionally, the AD8214 provides an overcurrent detection signal in <100 ns (see *Figure 62*). This feature is useful in high current systems where fast shutdown in overcurrent conditions is essential.

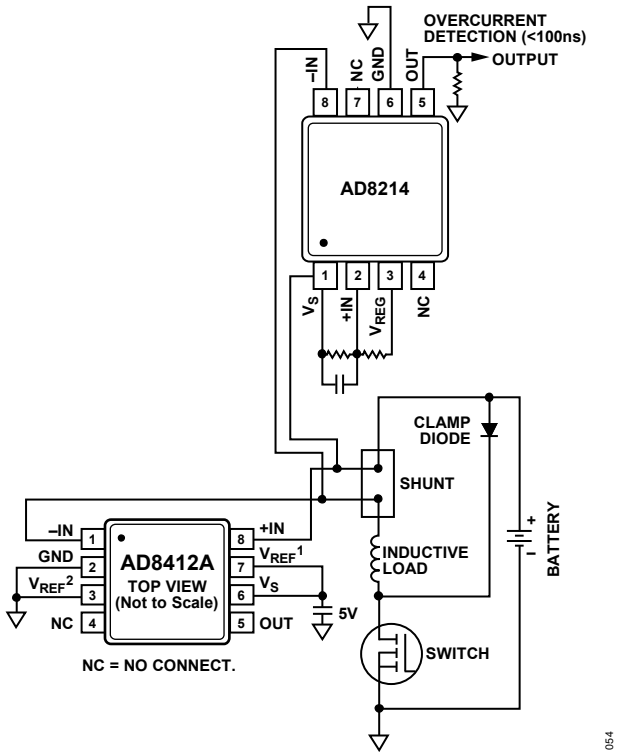

Figure 62. High Rail Current Sensing

Input Filter

In typical applications, such as motor control and solenoid current sensing, filtering at the input of the AD8412A can be beneficial in reducing differential noise, as well as transients and current ripples flowing through the input shunt resistor. Also, it is recommended to filter at the input of the AD8412A to further reduce the electromagnetic

interference (EMI). The EMI specifications vary depending on the application. Filter at the input if the output cannot be filtered because filtering at the output changes the low output impedance seen by the components attached to the output of the AD8412A. The +IN and −IN pins of the AD8412A have balanced input-bias currents. The input series resistors, R1 and R2, in *Figure 63*, must be the same measured value so as not to add large offset voltage on the output of the device because of R1 and R2. It is recommended to keep R1 and R2 at or below 100Ω. In *Figure 63*, C1 and C3 must be the same value.

For example, at 48V common-mode, when using a 10Ω resistor for R1 and R2, the estimated maximum error seen on the input of the AD8412A (V_{Error}RTI) due to the R1 and R2 resistors in the input filter is:

$$VErrorRTI = 10\Omega \times 2.7\mu A = 27\mu V \qquad (3)$$

where, 2.7µA is the maximum input offset current at 48V input common-mode, as listed in *Table 1*.

The EMI filter has two different bandwidths, common-mode and differential. The differential bandwidth defines the frequency response of the filter with a differential input signal applied between the two inputs of the amplifier, +IN and −IN.

The −3 dB differential bandwidth for the filter is:

$$\mathrm{BW_{DIFF}} = \frac{1}{2\pi \times \mathrm{R1} \times ((2 \times \mathrm{C2}) + \mathrm{C1})} \qquad (4)$$

The common-mode bandwidth defines what a common-mode RF signal sees between GND and the +IN and −IN of the amplifier tied together.

The −3 dB common-mode bandwidth for the filter is:

$$\mathrm{BW_{CM}} = \frac{1}{2\pi \times \mathrm{R1} \times \mathrm{C1}} \qquad (5)$$

Keep the resistor values to a 1% tolerance and the filter capacitors to a 5% tolerance to assist with reducing AC common-mode rejection (CMR) errors. Choose C2 to be at least 10× larger than C1 or C3 to reduce AC CMR errors, which are caused by component mismatching.

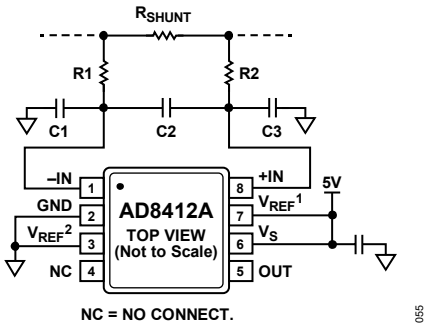

Figure 63. Input Filter

Overcurrent Detection

In several current-sensing applications, it is required to quickly detect when the current exceeds a certain threshold in the presence of a fault condition for safety concerns. As mentioned in the *High Rail Current Sensing* section, the AD8214 can be used for overcurrent detection in high current systems where fast shutdown in overcurrent conditions is essential.

Another common practice for overcurrent detection in current-sense applications is to use a comparator on the output of the currentsense amplifier. *Figure 64* and *Figure 65* show typical configurations for monitoring current and using a comparator for overcurrent detection in unidirectional current and bidirectional currents, respectively.

Choose the values of R1 and R2 in *Figure 64* and *Figure 65* to set the threshold voltage at which the overcurrent detection trips. For example, for the bidirectional overcurrent detection configuration shown in *Figure 65*, if the shunt resistance (R_{SHUNT}) is 50mΩ, and it is required to trip the overcurrent detection at ±3A, use Equation 6, Equation 7, and Equation 8 to find the R1 value after choosing an arbitrary value for R2. Choose, R2 = 4800Ω, and V_S = 5V.

Threshold voltage (V_{THR}) is the voltage the output of the AD8412A must reach to trip the overcurrent detection. If it is required the overcurrent detection trips at 3A, then:

$$V_{THR} = 3A \times R_{SHUNT} \times 10V/V + 2.5V \quad (6)$$

The 2.5V is added because the references are set up in split supply mode, then:

$$V_{THR} = 3A \times 50m\Omega \times 10V/V + 2.5V = 4V \quad (7)$$

After V_{THR} is known, use Equation 8 to find R1:

$$\mathrm{R1} = \frac{\mathrm{R2}(\mathrm{V_S} - V_{THR})}{V_{THR}} = \frac{4800\Omega \times (5\mathrm{V} - 4\mathrm{V})}{4\mathrm{V}} = 1200\ \Omega \quad (8)$$

For the second ADCMP601, keep the same values for R1 and R2. Attach the V_N pin to the output of the AD8412A, attach R2 to the 5V supply, attach R1 to ground, and attach the V_P pin to the connection between R2 and R1 to allow negative overcurrent detection (as shown in *Figure 65*).

Therefore, when the output of the AD8412A reaches as shown in Equation 9, the output of the ADCMP601 used for negative overcurrent detection trips high.

$$(2.5V - 3A \times 50m\Omega \times 10V/V) = 1V \quad (9)$$

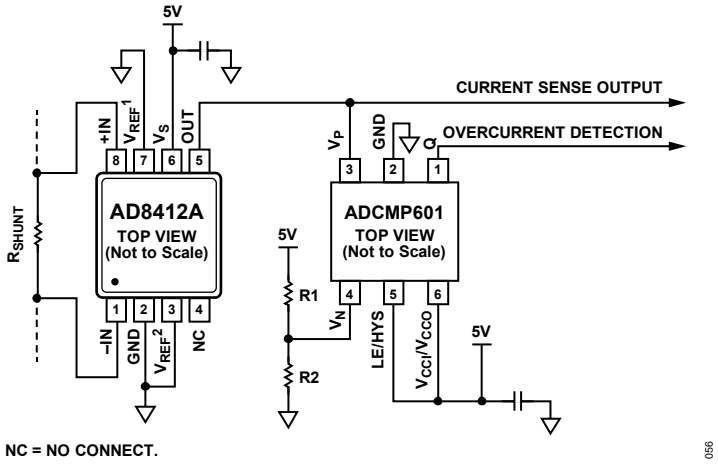

Figure 64. Unidirectional Overcurrent Detection

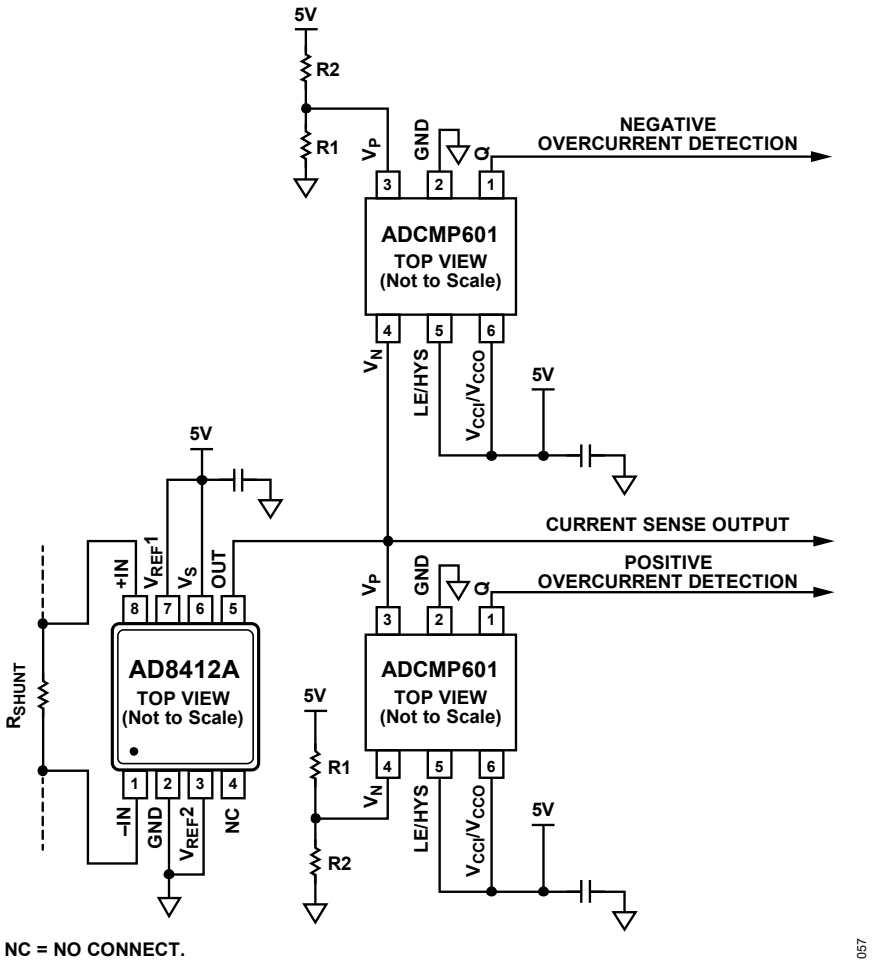

Figure 65. Bidirectional Overcurrent Detection

OUTLINE DIMENSIONS

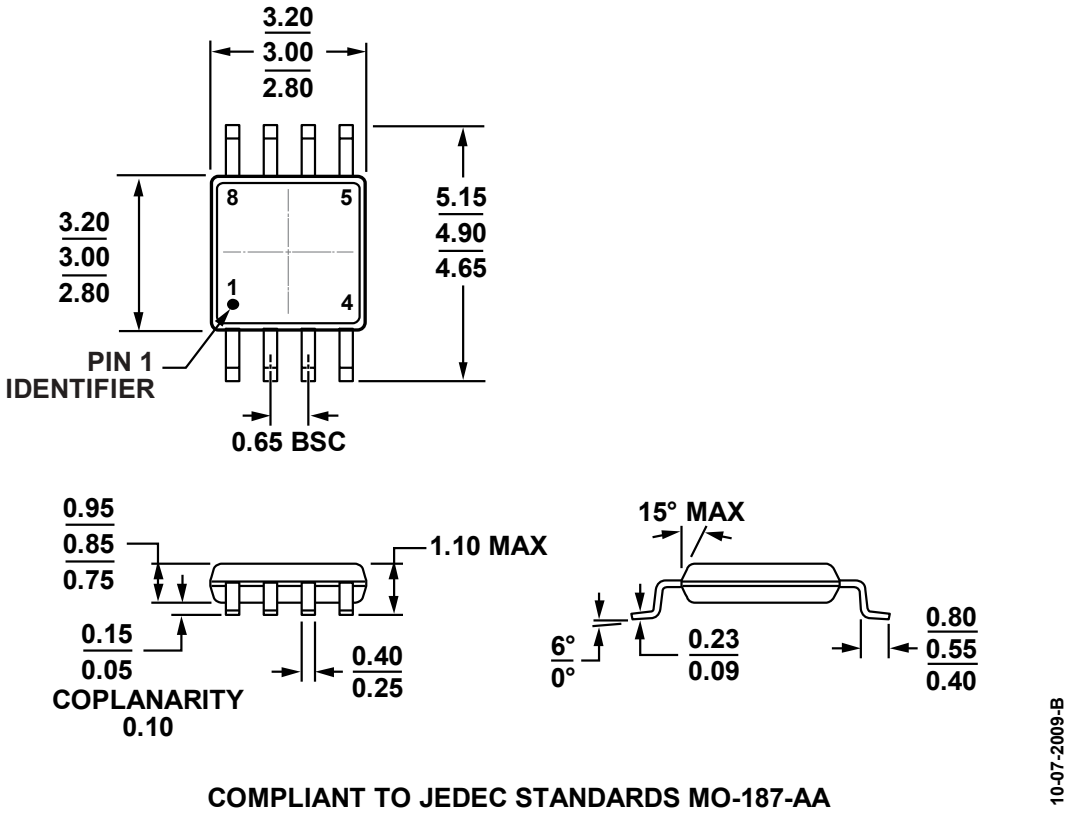

Figure 66. 8-Lead Mini Small Outline Package [MSOP] Narrow Body (RM-8). Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Table 6. Ordering Guide

Model 1, 2	TEMPERATURE RANGE	PACKAGE DESCRIPTION	Packing Quantity	PACKAGE OPTION	Marking Code
AD8412ABRMZ	−40°C to +125°C	8-Lead MSOP		RM-8	A5W
AD8412ABRMZ-RL	−40°C to +125°C	8-Lead MSOP	Reel, 3000	RM-8	A5W

[1] Z = RoHS compliant part

EVALUATION BOARDS

Model 1	Description
AD8412ARM-EVALZ	Evaluation Board for 8-Lead Mini Small Outline Package [MSOP]

[1] Z = RoHS compliant part