SELECTED ITEM DRAWING

			ANALOG DEVICES	
Unless otherwise specified DIMENSIONS ARE IN INCHES (MM)	TOLERANCES: .XX +/- 0.010 .XXX +/- 0.005 .XXXX +/- 0.002 ANGLES +/- .5 DEG	Drawing practices per **ASME Y14.100**	**14 Gpbs, Fast Rise Time D-Type Flip-Flop W/ Programmable Output Voltage & Positive Supply**	
			SIZE **A**	DRAWING NUMBER **SID000080**

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1. SCOPE

1.1. Scope

This drawing establishes the requirements for the 14 Gbps, Fast Rise Time D-Type Flip-Flop w/ Programmable Output Voltage & Positive Supply, assembled hermetically in the LH5 package, to be screened in accordance with MIL-PRF-38535, Class Level B, to the requirements specified in 4.1, 4.2, and 4.3 herein.

1.2. Analog Devices Part Number

Generic Part Number	Screened Part Number
ADH747S	HMC7121LH5

2. APPLICABLE DOCUMENTS

2.1. Government Documents

Unless otherwise specified, the following drawings and standards, of the issue in effect on the date of the accepted purchase order, in the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, shall form a part of this drawing to the extent specified herein.

DEPARTMENT OF DEFENSE TEST METHOD STANDARD

MIL-STD-883 Microcircuits

DEPARTMENT OF DEFENSE PERFORMANCE SPECIFICATIONS

MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification For

2.2. Non-Government Documents

The following documents, of the issue in effect on the date of the purchase order, form a part of this drawing to the extent specified herein:

Analog Devices Inc.

ADI Standard Space Products Program – Class Level B

HMC747LC3C Data Sheet Commercial Product Datasheet v07.0514 (Reference Only)

3. REQUIREMENTS

3.1. General Requirements
The devices delivered shall comply to this specification.

3.2. Design Construction and Physical Dimensions
The design construction and physical dimensions shall be as defined in Figure 1 herein.

3.3. Traceability
Each delivered device shall be traceable to the wafer lot and wafer number. Inspection lot records shall be maintained to provide traceability to the specific wafer and wafer lot from which the chips originated as well as traceability to package and materials.

3.4. Burn-In and Life Test Circuit
The burn-in and life test circuit and conditions shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test methods 1005 and 1015 per MIL-STD-883.

4. QUALITY ASSURANCE PROVISIONS

4.1. Wafer Lot Acceptance Testing
Wafer lot acceptance is not required for Class Level B.

4.2. Flight Screening Requirements
Flight screening requirements shall be per MIL-STD-883 TM 5004 for Class Level B microcircuits.

4.2.1. Electrical Test Requirements
Electrical test requirements are defined in Table I herein.

4.2.2. Electrical Performance Characteristics
Electrical performance characteristics are specified on Table II herein.

4.2.3. Burn-In Delta Requirements
Pre and Post Burn-In Electrical test and delta parameters shall consist of the tests specified in Table III herein.

4.3. Quality Conformance Inspection (QCI)
Group B, Group C, and Group D tests shall be performed per MIL-STD-883 TM 5005 for Class Level B microcircuits.

4.3.1. Post Steady State Life Electrical Test
Post steady state life electrical tests shall consist of the tests specified per Table II tested at room temperature only. Devices must meet delta parameter requirements in accordance with Table III herein.

5. MIL-PRF-38535 ASD-LITE EXCEPTIONS

The manufacturing flow described in the ADI STANDARD SPACE PRODUCTS PROGRAM is to be considered a part of this specification.

5.1. Wafer Fabrication

Foundry information is available upon request.

5.2. Group B

Subgroup 2: Resistance to solvents is not applicable.

5.3. Group C

Subgroup 1: Qty/Acc = 5/0.

5.4. Group D

Subgroup 3: Qty/Acc = 5/0.
Subgroup 4: Qty/Acc = 5/0.
Subgroup 5: Not applicable.
Subgroup 7: Not applicable.
Subgroup 8: Not applicable.
Subgroup 9: Not applicable.

6. PREPARATION FOR DELIVERY

The preparation for delivery, packaging, preservation, ESD protection and handling shall be in accordance with MIL-PRF-38535.

6.1. Part Marking

Devices shall be marked as specified on Figure 1 herein.

6.2. Inspection Data Requirements

The following data shall accompany each shipment.

a. A Certificate of Conformance (C of C) certifies that the lot(s) meets all requirements of this specification.
b. Summary of electrical test requirements defined in 4.2 herein.
c. Summary of QCI results defined in 4.3 herein.
d. Failure Analysis with photos (If applicable)
e. A cover sheet indicating the following purchasing information:
    1. Customer purchase order number.
    2. Analog Devices part number.
    3. Part lot identification codes.
    4. Date & quantity shipped.

TABLE I: ELECTRICAL TEST REQUIREMENTS

Test Requirement	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1, 4
Final Electrical Parameters	1, 4 1/2/
Group A Electrical Parameters	1, 2, 3, 4, 5, 6
Group C End-Point Electrical Parameters	1, 4 2/
Group D End-Point Electrical Parameters	1, 4

TABLE I Notes:
1/ PDA applies to Table I subgroup 1 and Table III delta parameters.
2/ See Table III for delta parameters

TABLE II: ELECTRICAL PERFORMANCE CHARACTERISTICS (-40 °C, +25 °C AND +85 °C)

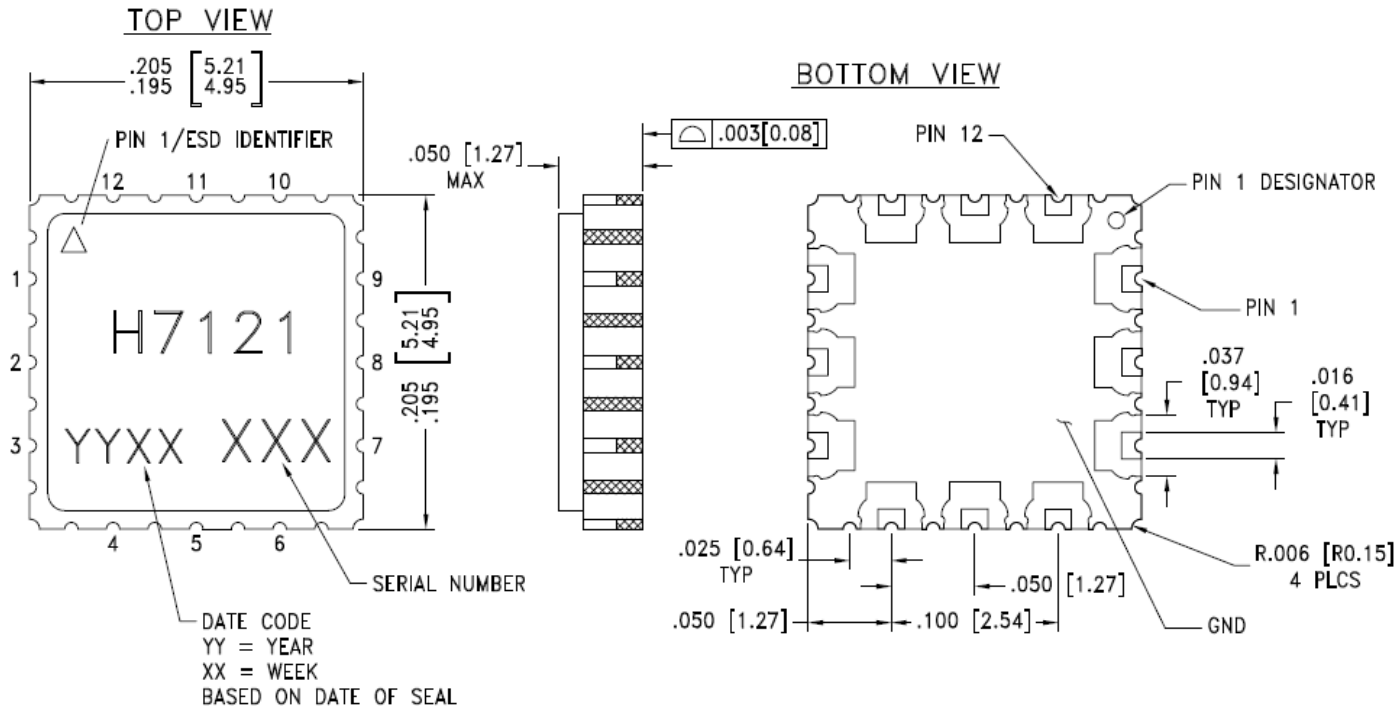
Parameter	Test Conditions 1/2/ Unless otherwise specified	Group A Subgroups	Limits		Units
			Min	Max	
QN High Voltage	DP-DN=Low, initiate a rising edge of the CLK by setting CP-CN=Low, then CP-CN=High.	1	3.2	3.32	V
QN Low Voltage	DP-DN=High, initiate a rising edge of the CLK by setting CP-CN=Low, then CP-CN=High.	1	1.8	2.1	V
QP High Voltage	DP-DN=Low, initiate a rising edge of the CLK by setting CP-CN=Low, then CP-CN=High.	1	1.8	2.1	V
QP Low Voltage	DP-DN=High, initiate a rising edge of the CLK by setting CP-CN=Low, then CP-CN=High.	1	3.2	3.32	V
QN Single-Ended Output Amplitude	13 Gbps 1010 Pattern to DP, 13 GHz CLK to CP Data and CLK set to 400 mVp-p	4	400	700	mV
QP Single-Ended Output Amplitude		4	400	700	mV
CP Rise Time		4	10	40	ps
CP Fall Time		4	10	40	ps
QN Single-Ended Output Amplitude	13 Gbps 1010 Pattern to DN, 13 GHz CLK to CN Data and CLK set to 400 mVp-p	4	400	700	mV
QP Single -Ended Output Amplitude		4	400	700	mV
CN Rise Time		4	10	40	ps
CN Fall Time		4	10	40	ps
Power Supply Current (Icc)		1	60	90	mA

TABLE II Notes:
1/ Test limits apply at +25 °C only with Vcc = +3.3 V and VR = +3 V
2/ -40 °C and +85 °C (Subgroups 2, 3, 5, and 6) shall be read and record only.

TABLE III: BURN-IN/LIFE TEST DELTA LIMITS 1/2/3/

Parameter	Test Conditions	Delta Limits	Units
Power Supply Current (Icc)	Per Table II	± 10	%

TABLE III Notes:
1/ Delta test is performed at T_A = +25 °C only.
2/ Table II limits will not be exceeded.
3/ Deltas calculated at pre/post 160 hours and post 160 hour / post1000 hours.



NOTES:

1. PACKAGE BODY MATERIAL: CERAMIC & KOVAR
2. LEAD AND GROUND PADDLE PLATING: GOLD 40-80 MICROINCHES.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. CHARACTERS TO BE LASER MARKED WITH .018"MIN to .030"MAX HEIGHT REQUIREMENTS. UTILIZE MAXIMUM CHARACTER HEIGHT BASED ON LID DIMENSIONS AND BEST FIT. LOCATE APPROX. AS SHOWN.
6. PAD BURR LENGTH 0.15mm MAX. PAD BURR HEIGHT 0.25mm MAX.
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
8. THE SOLDER FILLET BETWEEN PACKAGE AND COVER IS PART OF THE DESIGN SEAL AREA.

PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION	PIN #	FUNCTION
1	Vcc	4	N/C	7	QN	10	Vcc
2	DN	5	CP	8	QP	11	VR
3	DP	6	CN	9	Vcc	12	GND

Figure 1 – Device Outline for the HMC7121LH5

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
HMC7121LH5	–40 °C to +85 °C	12-Lead Ceramic Hermetic SMT	LH5 (E-12-5)

Revision History

Revision History		
Rev	Description of Change	Date
A	Initial release.	02/06/2025

ANALOG DEVICES

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