AD2437 A²B Transceiver Audio Performance Testing and Results

Contributed by John Tomarakos *Rev 1.0 –September 26, 2024*

Introduction

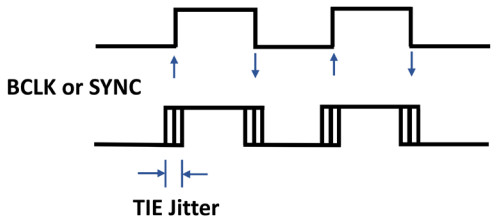
Systems based on the AD2437 A²B™ (Automotive Audio Bus) transceiver deliver multi-channel, bi-directional I²S/TDM audio, clock, and data over a maximum distance of 300 meters, using RJ45/CAT5 or XLR microphone cable. The AD2437 was designed for professional audio and distributed audio systems that have rigorous audio requirements beyond what consumer and automotive audio products have. The audio performance of such systems, which perform audio clock recovery from the transmitted stream, can be subject to some degradation due to clock jitter. The clock jitter accumulates as the clock information proceeds from node to node through the AD2437 bus. For most designers of consumer- or prosumer-grade products, this degradation in audio quality is not sufficient to cause concern and may be acceptable. For other products with more stringent quality requirements, a closer look at audio performance is warranted. This application note:

- Evaluates the audio performance of an AD2437 A²B bus.
- Describes results of testing performed on an AD2437 A²B bus.
- Discusses possible methods to mitigate audio degradation.

Jitter Accumulation in A²B Systems

A²B networks use a daisy-chain style topology, where a clock signal propagates and is recovered at each node. The A²B transceiver at the main node uses the SYNC and BCLK signals received at the I²S/TDM interface for the master clock of the entire A²B bus. This main node generates clocks and encodes them into the bus data from which each downstream sub node derives its own synchronization signals. Each subordinate node subsequently regenerates the clocks and embeds it into the A²B data for the next downstream node. The clock that is propagated along the cascaded nodes may show increased jitter as the number of nodes increases. While the data on the bus is bit-correct at all points, each node contributes a small amount of jitter to the clocks resulting in a slight increase in overall jitter as the node count increases. There are several ways to measure this jitter (Figure 1). The most common methods for clock recovery systems are cycle-to-cycle jitter and Time Interval Jitter (TIE).

Figure 1 Time Interval (TIE) Jitter



Time Interval Error (TIE) is the difference between the observed clock edge time and expected clock edge time. *TIE* refers to clock edges, while *period jitter* refers to the clock period. TIE is calculated by subtracting the actual clock edge from the ideal clock edge. Analog Devices provides RMS Time Interval Error (TIE_{RMS}) data measured at each subordinate node I^2S/TDM port in the *AD2437 A2B Transceiver Datasheet*[1]. Tables 14 and 15 of the *AD2437 A2B Transceiver Datasheet*[1] displayed in Figure 2, provide RMS TIE jitter for each node, for both the I^2S SYNC and BCLK signals, and a maximum of 16 supported subordinate nodes. However, it can be observed at each sub node I^2S/TDM port and can result in distortion during any A/D and D/A conversions.

Figure 2 AD2437 Datasheet Specified TIE_{RMS} Jitter for I^2S SYNC and BCLK Signals

Table 14. SYNC Output RMS TIE Jitter at Each Subordinate Node[1]

Subordinate Node	Typ	Max	Unit
1	1.25	2.28	ns
2	1.47	2.29	ns
3	1.59	2.41	ns
4	1.76	2.59	ns
5	1.88	2.95	ns
6	1.99	3.18	ns
7	2.14	3.57	ns
8	2.24	3.08	ns
9	2.31	4.01	ns
10	2.48	4.24	ns
11	2.60	4.31	ns
12	2.66	4.35	ns
13	2.70	4.55	ns
14	2.75	4.59	ns
15	2.80	4.70	ns
16	2.95	4.89	ns

[1] Measured at f_{SYNC} = 48 kHz.

Table 15. BCLK Output RMS TIE Jitter at Each Subordinate Node[1]

Subordinate Node	Typ	Max	Unit
1	1.19	2.09	ns
2	1.39	2.21	ns
3	1.59	2.33	ns
4	1.76	2.51	ns
5	1.86	2.86	ns
6	1.91	3.11	ns
7	2.06	3.31	ns
8	2.21	3.45	ns
9	2.28	3.84	ns
10	2.31	4.00	ns
11	2.47	4.03	ns
12	2.57	4.06	ns
13	2.74	4.28	ns
14	2.78	4.38	ns
15	2.83	4.50	ns
16	2.88	4.60	ns

[1] Measured at f_{BCLK} = 3.072 MHz.

Before taking Total Harmonic Distortion and Noise (THD+N) measurements, the APx555 Jitter measurements are taken from the I^2S/TDM port of each AD2437 sub node and displayed in Table 1. Notice that the measurements match closely with the datasheet values. The parts used in this experiment were selected because they have higher jitter at 25 deg C than the typical A2B part. Despite the increase in TIE_{RMS} with increasing node count, no degradation of THD+N was observed when analyzing the digital serial data measured from I^2S/TDM input at the main node to I^2S/TDM output at each sub node.

Table 1 Actual Jitter Measurements for 16 Subordinate Nodes Using the APx555 Audio Analyzer

Sub Node	Typical TIE_{RMS} (ns)	Sub Node (cont.)	Typical TIE_{RMS} (ns)
0	1.37	8	2.28
1	1.59	9	2.37
2	1.73	10	2.45
3	1.84	11	2.53
4	1.95	12	2.58
5	2.06	13	2.66
6	2.14	14	2.72
7	2.19	15	2.83

Audio Performance Measurement-Total Harmonic Distortion Plus Noise

The primary goal for designing high-quality audio systems is to ensure that the device output can faithfully transmit or reconstruct the audio signal that is fed into the system. And that means ideally, the output signal is an identical or scaled version of the input signal. Anything that alters the input signal in any way, such high-jitter clock on the D/A conversion stage, is known as distortion. Audio performance and quality (SNR, dynamic range, THD, and so forth) must be measured and quantified.

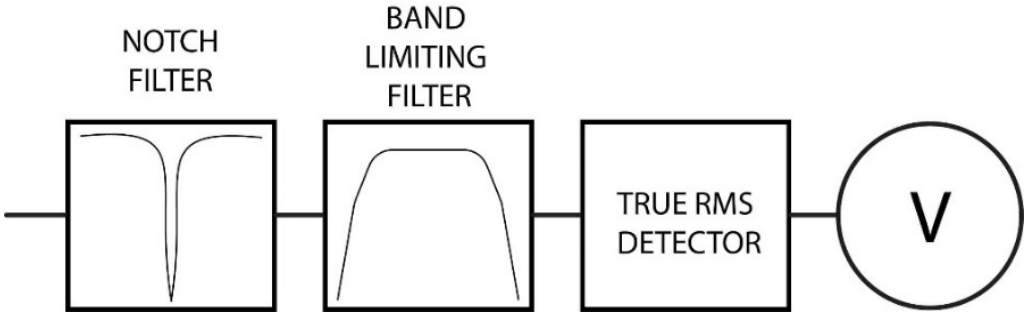
The best way to test the audio quality and performance of such a system is to simulate or inject into the system a pure sine tone and perform spectral analysis of the output signal. This helps us analyze the output of the system for any unwanted distortion components that were not part of the original signal input. These nonlinearities cause harmonic distortion at multiples of the input sine tone frequency generated and other noise components.

The most common method of measuring distortion and noise components (Figure 3) is THD+N, done by:

1. Implementing a notch filter tuned to the generated or measured fundamental sine tone frequency.
2. Following the notch filter with a band limiting filter (normally set within our audible hearing range of 20 Hz to 20 kHz).
3. Ending with an RMS level detector that determines the ratio of the residual noise and harmonic divided by the level of the input signal.

For the A^2B system, use the Audio Processor (AP) to inject a tone on the I^2S input and measure the THD+N at the far-end DAC analog output using the AP. To perform this test, Analog Devices used the APx555 Audio Precision Analyzer and APX500 version 8.0 software.

Figure 3 Block Diagram of THD+N Analyzer (Source: ap.com)

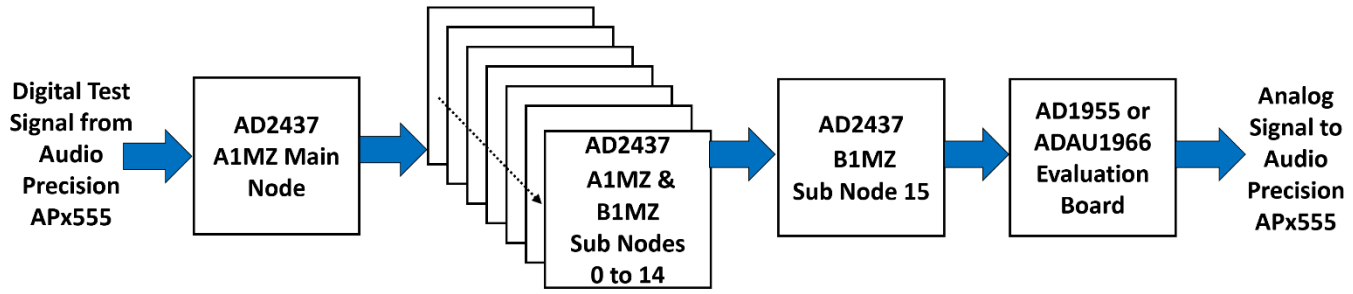


The AD2437 transceiver uses a built-in phase-locked loop (PLL) to recover the clock at each node. A small amount of jitter measured in single-digit nanoseconds happens at each node, resulting in a small amount of audio degradation that is additive as distance from the main node increases. The audio degradation is not tonal in nature but spread across the spectrum. With high-level signals, this results in earlier sub-nodes in an AD2437 transceiver-based system having slightly better measured audio performance than sub-nodes towards the end of the A^{2}B bus. The measured difference between nodes cannot be observed with lower-level audio signals; therefore, there is no audible decrease in audio performance with higher node counts and lower signal levels.

THD+N Measurement Setup and Equipment Required

The audio performance of the AD2437 A^{2}B bus can be measured using a series of AD2437 transceiver evaluation boards, an audio performance measurement system, and a digital-to-analog converter. This test used the Audio Precision APx555 Audio Analyzer with the Analog Devices AD1955 DAC or ADAU1966 DAC as shown in the Figure 4 block diagram. See *AD1955 High Performance Multibit Sigma-Delta DAC with SACD Playback Datasheet*[5] and *ADAU1966 16-Channel High Performance Differential Output, 192 kHz, 24-Bit DAC Datasheet*[8] for further setup information for this test.

Figure 4 Block Diagram of Test Setup

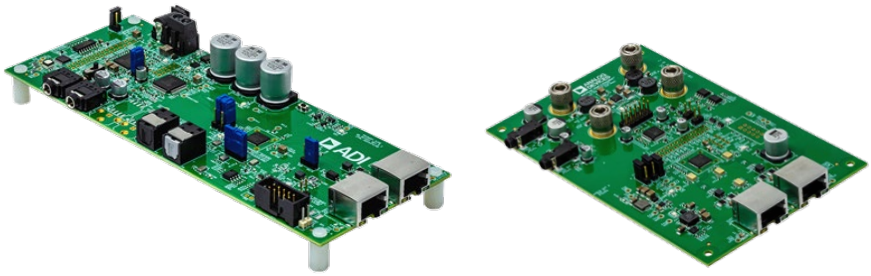


The Digital Signal taken from Audio Precision shown in Figure 4 is a digital 1 kHz or 11 kHz sine wave provided by the APx555 Audio Analyzer output to the AD2437 Transceiver Master Node board. Measurements are taken for both -1 dBV and -40 dBV input signals.

The Analog Signal connected back to Audio Precision shown in Figure 4 is connected to the input of the APx555 Audio Analyzer, and audio performance is measured. The A^{2}B bus is extended by inserting additional sub-nodes (depicted by the combination of AD2437 *A1MZ LPS and AD2437 BPS Sub-Node* blocks in Figure 4), enabling measurements for the full set of ten sub-nodes.

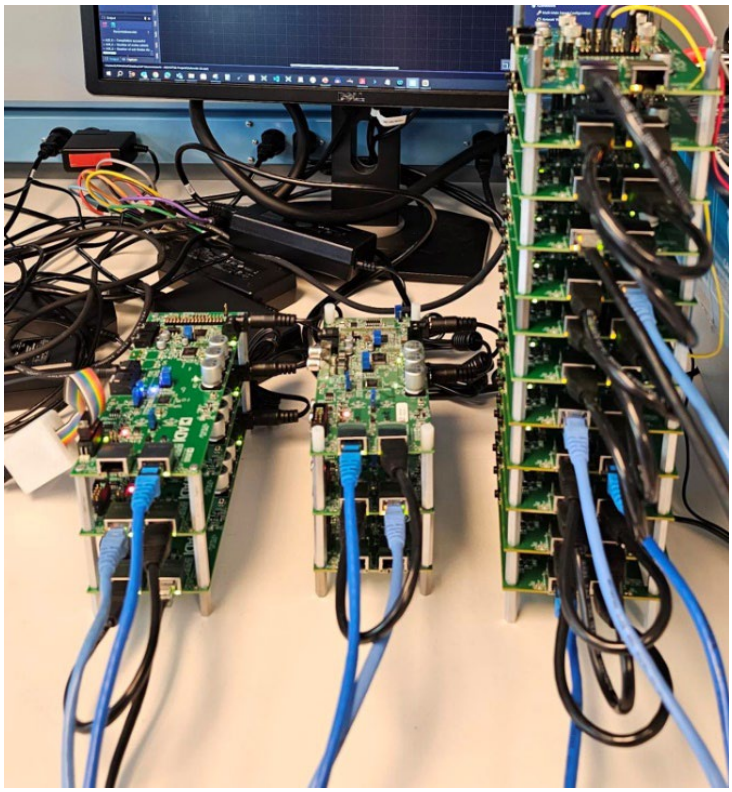
The test setup uses a combination of four EVAL-AD2437A1MZ evaluation kits (1 main and 4 sub nodes), plus twelve EVAL-AD2437B1MZ evaluation kits. The two evaluation kits are shown in Figure 5. Use *EVAL-AD2437A1MZ Manual*[3] and *EVAL-AD2437B1MZ Manual*[4] to set up the evaluation kits.

Figure 5 Hardware Configuration Using EVAL-AD2437A1MZ (left) and EVAL-AD2437B1MZ (right) Evaluation Kits



The A^{2}B network system is a combination local-powered subordinate nodes shown on the left (referred to as *A1MZ* boards) and bus powered subordinate notes shown on the right (referred to as *B1MZ* boards). Depending on the configuration used to test the number of nodes, the A1MZ board must be inserted in between every fourth node (between four consecutive B1MZ boards), so that sufficient voltage can drive the downstream boards. Figure 6 shows the test setup of the combination of A1MZ and B1MZ boards. The upper-left A1MZ board (Figure 6) is the main board, and all others are subordinate boards. The cables lengths between nodes were half a meter for B1MZ board connections and one meter for A1MZ connections to the B1MZ boards.

Figure 6 THD+N Test setup using a combination of EVAL-AD2437A1MZ and EVAL-AD2437B1MZ

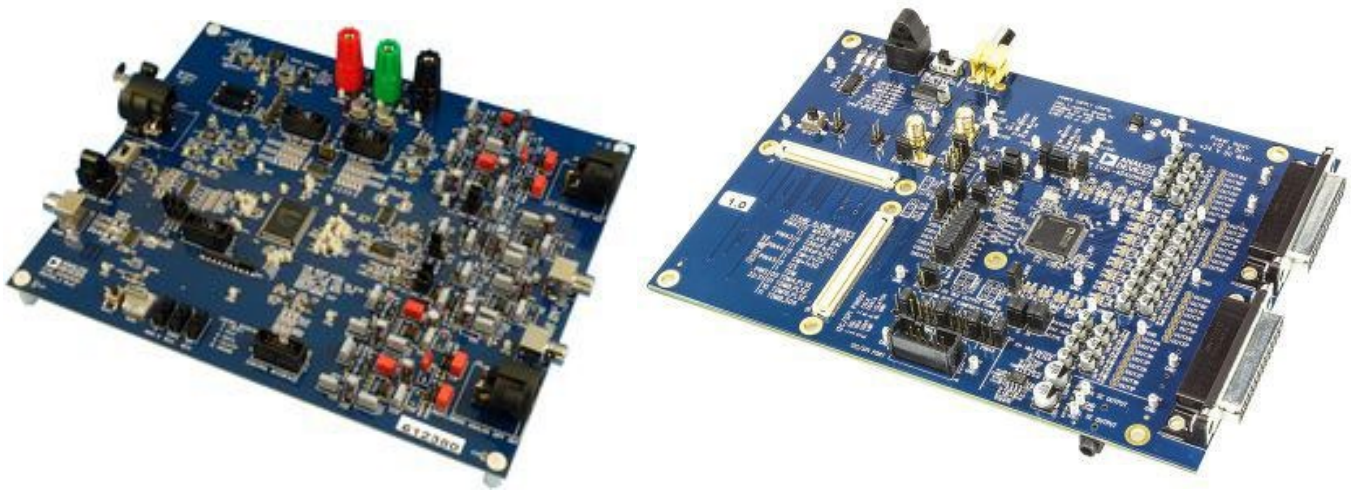


Measurements taken during this test setup (Figure 6) included a single sub-node (sub[0], depicted as the single *B1MZ Sub-Node* in Figure 4 with no *other A1MZ or B1MZ AD2437 Sub-Nodes* present) and up to a maximum sixteen sub nodes (sub[0…15], where sub[n] is the *A1MZ or B1MZ Sub-Node* in Figure 6. For each test setup, the measurement was taken at the last sub node, and all results are measured in THD+N dBrA, where A is set such that 0 dBrA = 0 dBFS.

Selection of High-Quality DAC for THD+N Performance Testing

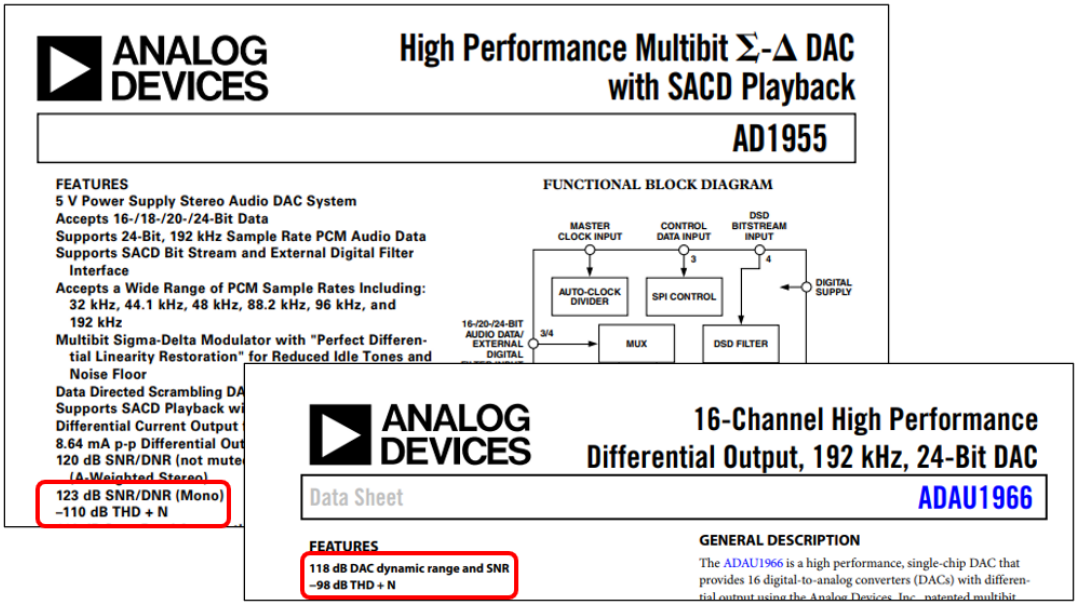
To examine the effects of accumulated jitter on an audio system, a high-quality DAC must be chosen to see when any negative audible artifacts are introduced because of the jitter introduced by consecutive A^{2}B sub nodes. The higher the dynamic range (SNR and THD+N), the lower the noise floor (baseline) in the FFT spectrum analysis. The Analog Devices DAC converter evaluation kits (EVAL-AD1955EBZ and EVAL-ADAU1966Z), shown in Figure 7 were chosen for this test. See *Evaluating the AD1955 High Performance, Multibit Sigma-Delta DAC with SACD Playback*[7] and *ADAU1966 16-Channel High Performance Differential Output, 192 kHz, 24-Bit DAC Datasheet*[8] for detailed set-up instructions.

Figure 7 EVAL-AD1955EBZ (right) and EVAL-ADAU1966Z (left) DAC Evaluation Kits



For high THD+N performance specifications, the AD1955 and ADAU1966 evaluation kits are the two products offered by Analog Devices. These products are *legacy* products which are 10 to 15 years old. The AD1955 is not recommended for new designs, however AD1955 evaluation kits and samples can be purchased through a few authorized distributors. These evaluation boards were chosen specifically because their performance exceeded other Analog Devices DACs on the market today (more than -95 dB THD+N). Figure 8 shows excerpts from the AD1955 datasheet (THD+N of -110 dB) and the ADAU1966 datasheet (THD+N at -98 dB, at 0 dBFS).

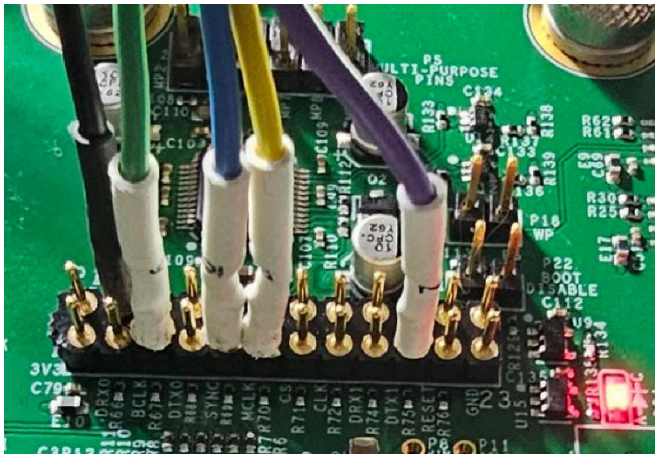
Figure 8 The AD1955 and ADAU1966 Were Two of the Highest Quality DACs from Analog Devices



Connecting the B1MZ sub node I2S Output to the AD1955 and ADAU1966

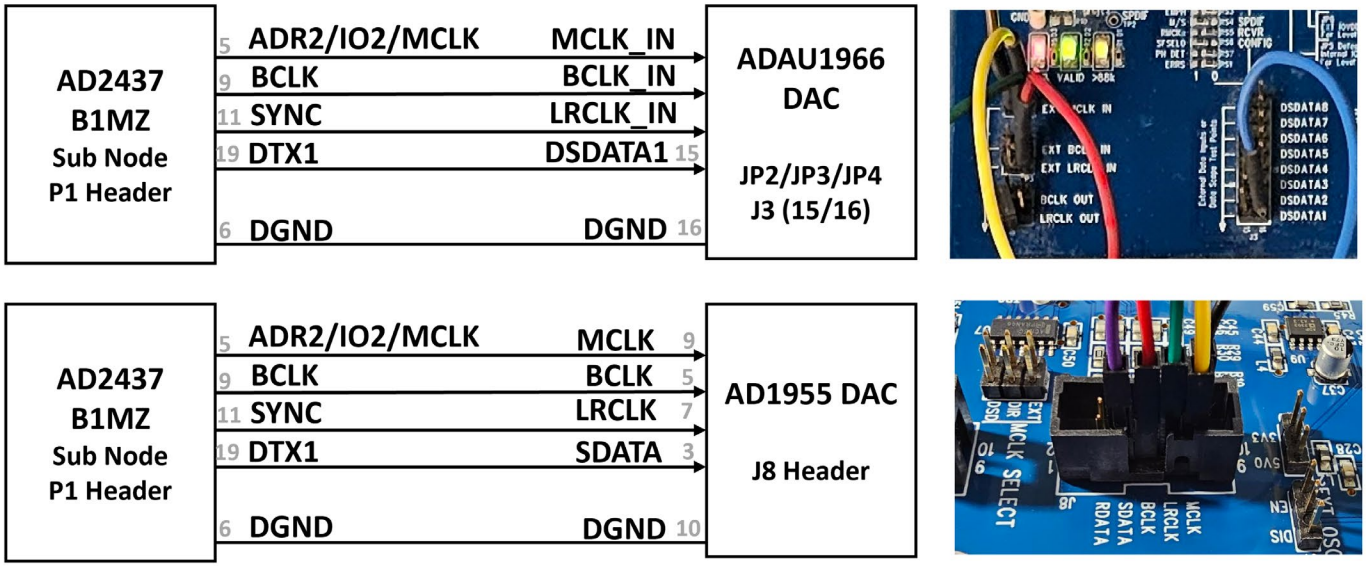
The last AD2437 B1MZ sub node provides the audio output through its I²S/TDM interface. Expect to hear the generated sine tone injected into the main AD2437 board streamed through the output of the last node. The two DAC boards also require a master clock (MCLK) to clock the device. The AD2437 needs to provide a 12.288 MHz CLKOUT on the ADR2 pin, the 3.072 MHz BCLK, 48 kHz SYNC, and DTX serial audio data. These pins are routed to the P1 header and are shown in Figure 9.

Figure 9 EVAL-AD2437B1MZ P1 Header I²S Signals



The block diagram for connecting the B1MZ I²S pins to the AD1955 and AAU1966 DAC evaluation boards is shown in Figure 10, including the P1 and J3/J8 header pin connections described in the evaluation kit schematics. Figure 10 also shows the connections with jumper wires for each DAC board.

Figure 10 B1MZ Sub Node I²S Output Connections to the AD1955 and ADAU1966 DAC Eval Kits



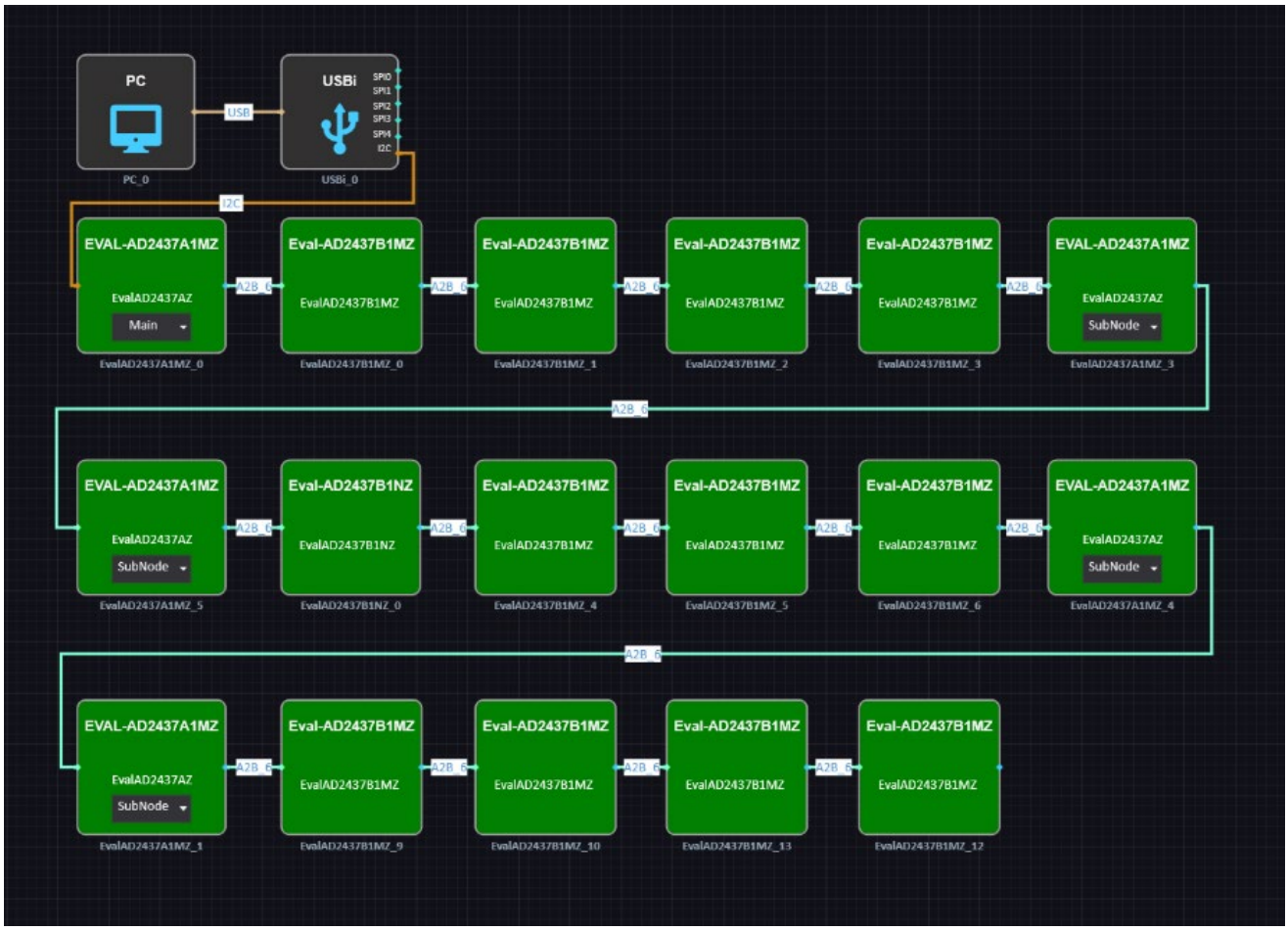
SigmaStudio+ Project Setup and Considerations

Use SigmaStudio version 2.0.1 and A²B plug-in version 1.2 to create the AD2437 test project. The test project configuration in Figure 11 has one main AD2437 node and sixteen AD2437 sub node connections.

In the SigmaStudio+ signal flow:

1. The first node in the system is defined as the main node using an AD2437A1MZ board.
2. Followed by four AD2437B1MZ bus-powered sub boards.
3. Next, there are two A1MZ local-powered sub nodes
4. Followed by four more B1MZ bus-powered sub boards.
5. Once again this is followed by two more A1MZ local-powered sub nodes.
6. Finally four additional B1MZ bus-powered sub nodes.

Figure 11 SigmaStudio+ 17-Node Configuration Used For the THD+N and Jitter Testing



SigmaStudio+ Generating 12.288 MHz CLKOUT2 on the ADR2/IO2 Pin for the AD1955/ADAU1966 MCLK Input

To properly connect the B1MZ I^{2}S interface to the DAC boards, enable a clock source on the *last* sub node for the Master Clock (MCLK) of the DACs. By default, this clock is not enabled in SigmaStudio+. The P1 header provides the ADR2/IO2 signal, which is enabled by programming the CLKCFG register to turn on the clock and divide the 24.575 MHz A^{2}B clock by two to generate the needed 12.288 MHz MCLK for the DACs. Figure 12 and Figure 13 show the required register settings in SigmaStudio+.

Figure 12 SigmaStudio+ AD2437 Subnode Register Settings for CLKOUT2 and CLKCFG Register

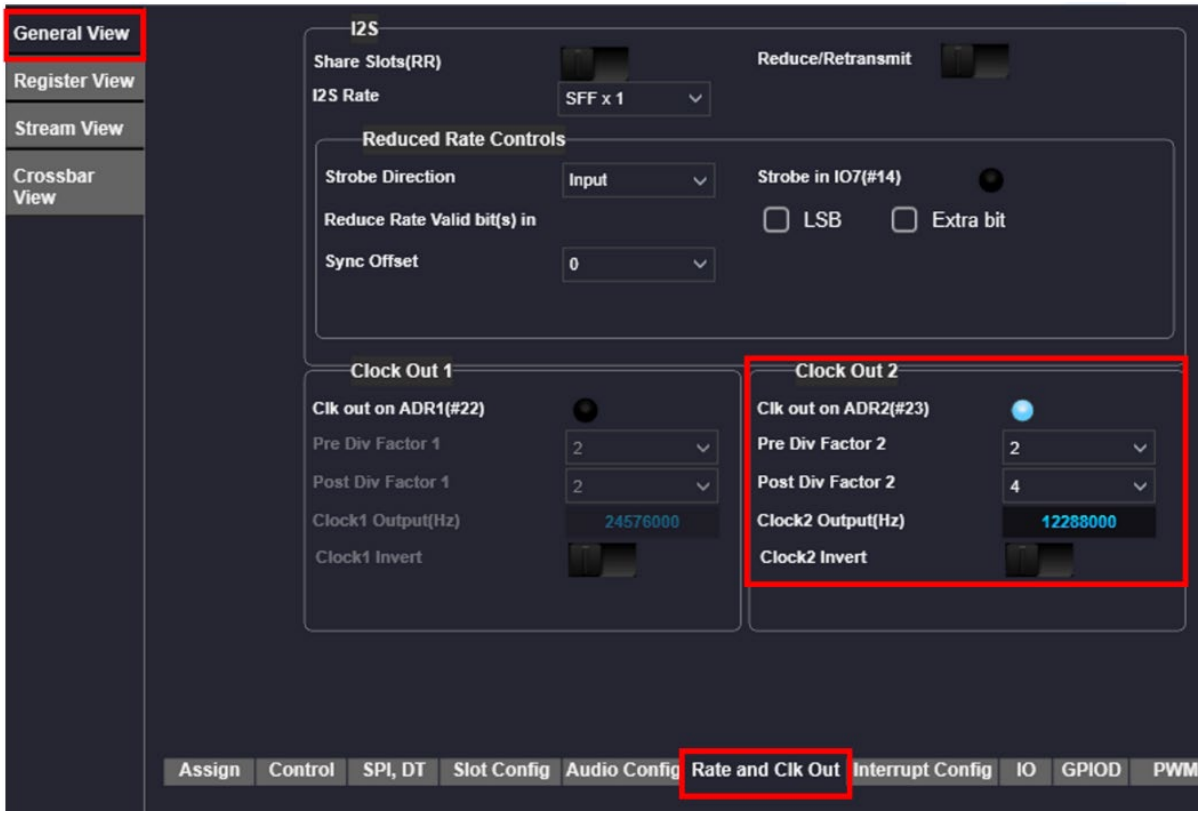


Figure 13 SigmaStudio+ CLKCFG Register bits 0 and 7 are set to 1

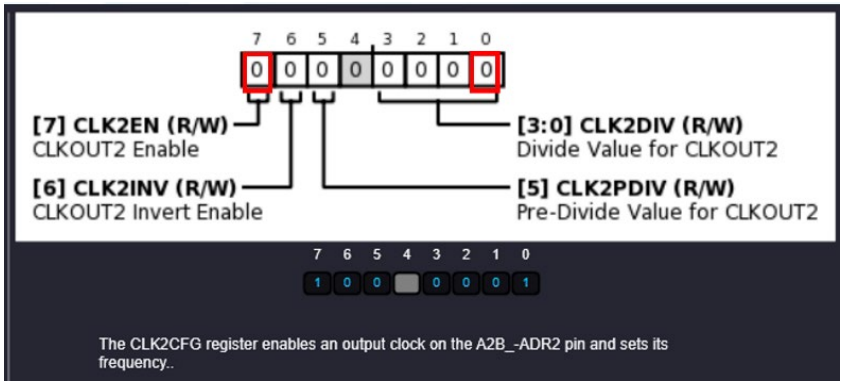
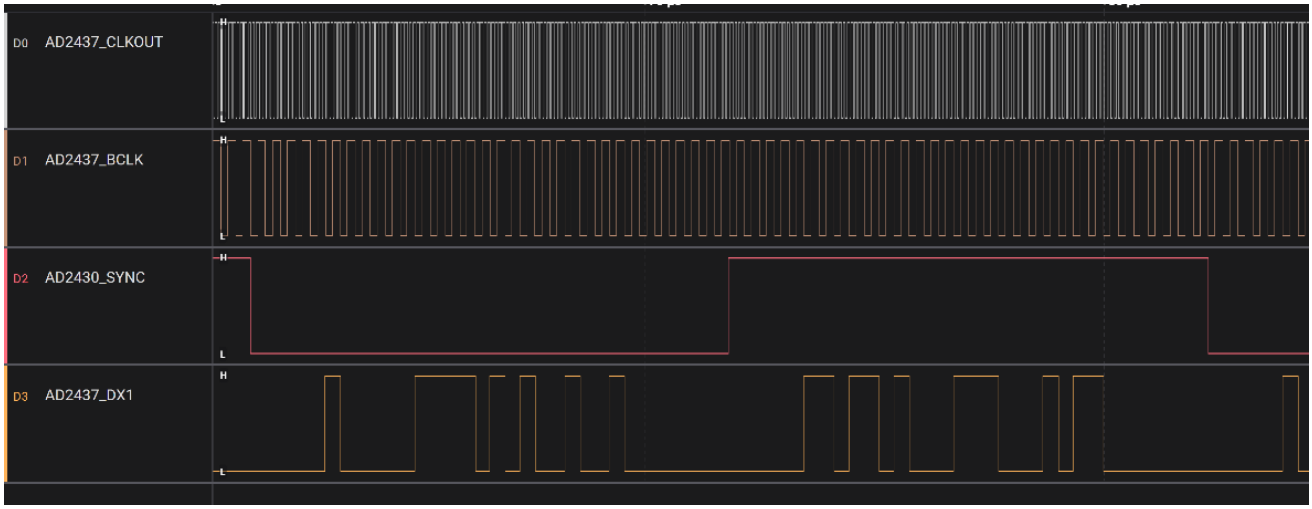


Figure 14 shows the required 12.288 MHz MCLK for the DAC (A2B's CLKOUT) is activated after programming the CLKCFG register.

Figure 14 Capture of B1MZ P1 Header – 12.288 MHz MCLK, 3.072 MHz BCLK, and 48 kHz SYNC



SPDIF Output – Source Used For Generating Tones for THD+N Test

When performing THD+N measurements using an A^2B system, the DSIO interface on the Audio Precision APx555 can be used to provide a direct I^2S connection to the AD2437 from the audio analyzer. When connecting the AP to the I^2S input pins on the P15 expansion connector, the ADAU1452 serial pins were preventing the ability to drive these pins. Previous AD242x eval kits provide additional jumpers to disconnect and directly access the SYNC, BCLK and data pins between the transceiver and ADAU1452.

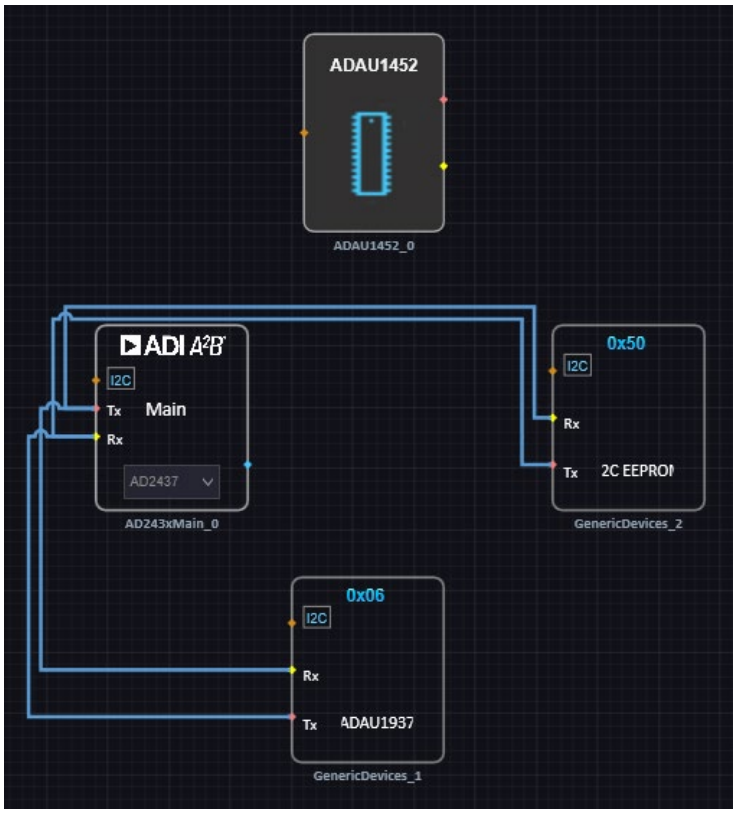
Instead of desoldering the ADAU1452 device, another alternative is to use the SPDIF optical input on the EVAL-AD2437-A1MZ main board to drive the test tones to the A^2B system. This signal path requires the on-board ADAU1452 to receive the digital audio optical signal and convert it to an I^2S stereo signal, which is transmitted to the AD2437 I^2S input, and streamed over the A^2B bus to the last sub node in the system.

SigmaStudio+ downloads a small DSP program that enables the optical SPIDF input to pass through a hardware ASRC conversion stage on the ADAU1452, before being transmitted out of the SPORT0. Initially, belief that the pure tone generated by the AP might be altered significantly by routing the SPDIF through the DSP to the AD2437 transceiver, proved nonexistent. However, measurements were taken to ensure there are no issues with the test setup.

SigmaStudio+ Project Settings to Enable SPDIF Input

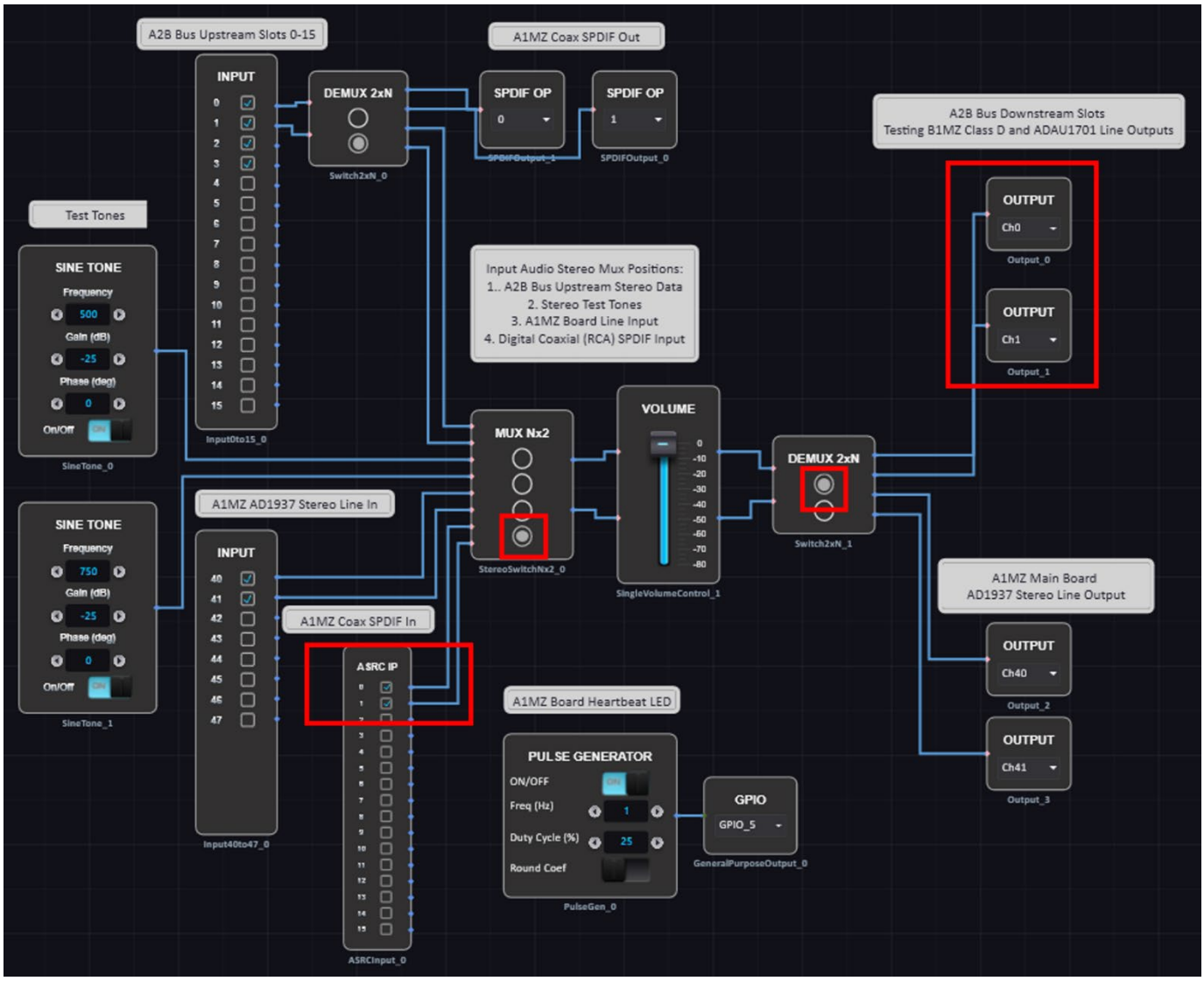
SigmaStudio+ includes additional benefits (vs. previous SigmaStudio software) with its hierarchal layout. An enhancement in the SigmaStudio+ tool helps configure and program the ADAU1452 within the same schematic block as the AD1937 main node transceiver. You can add a custom block for the ADAU1452 that allows for signal flow customization of the optical SPDIF input into the main node AD2437 I^2S input path, instead of linking in an XML file which contains the register and program settings for the ADAU1452. Figure 15 shows the system configuration within SigmaStudio+ for the main node.

Figure 15: Modified Main Node EVAL-AD2437A1MZ Platform that Provides Custom ADAU1452 Schematics



Double-click the ADAU1452 block, and the DSP core schematics display in a new tab (Figure 16). In this diagram the multiplexer and demultiplexer settings are set such that the audio is sourced from the ASRC input block associated with the SPDIF receiver (configured through the ADAU1452 register settings window under the project property settings). The ASRC0 audio path connects through the mux/de-mux stage and is transmitted using the SPORT0 I^2S out in the upper right of the schematic. This SPORT0 I^2S transmitter is physically connected to the AD2437 on the A1MZ evaluation kit. After a link-compile-download of the AD2437 project schematic, the audio stream for the A^2B bus automatically transfers SPDIF RX data over the A^2B bus using channel zero and channel one.

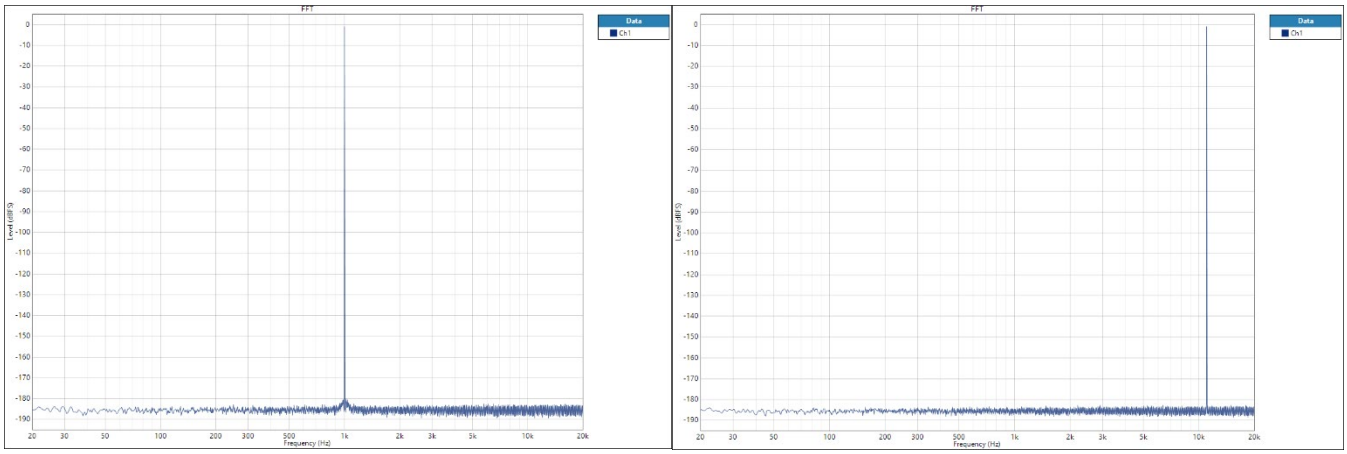
Figure 16: ADAU1452 Main Node Schematics Configuring SPDIF Input to Route to A²B Bus slots 0 and 1



APx555 SPDIF Loopback of 1 kHz and 11 kHz Test Tones

Test tones were measured from the APx555 SPIDIF transmitter to the SPDIF receiver input. The FFT spectrum of the audio signals (Figure 17 and Figure 18) shows no harmonic or noise generated, except for quantization noise which were the smallest LSBs of the 32-bit audio data approximating -185 to -190 dB.

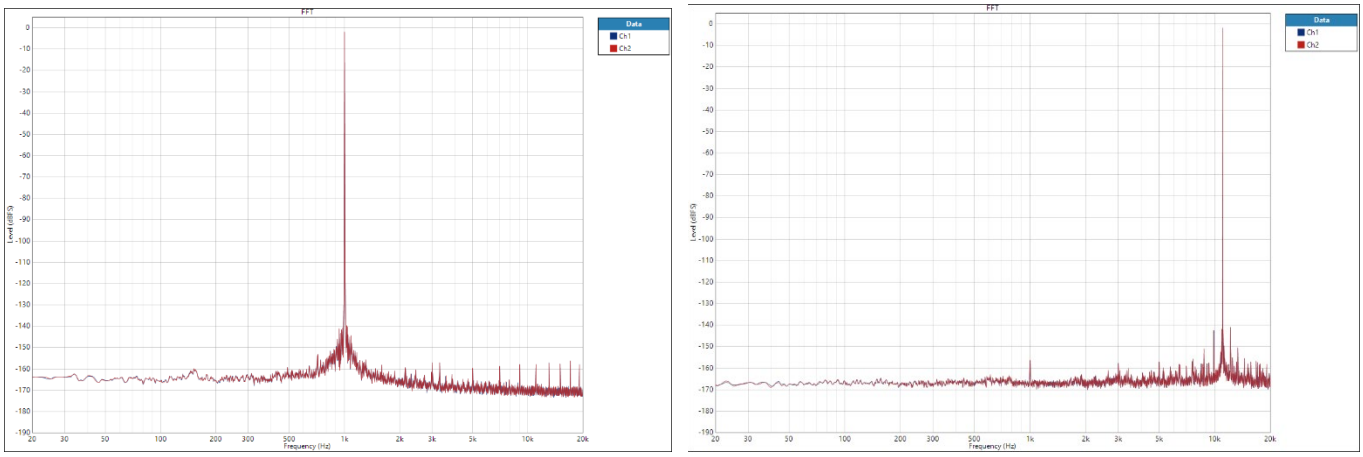
Figure 17 1 kHz at -1 dBFS APx555 SPDIF Loopback *Figure 18 11 kHz at -1 dBFS APx555 SPDIF Loopback*



1 kHz and 11 kHz Test Tones for THD+N Tests (Spectrum of Tone with APx555 DSIO Loopback)

Other measurements included the test tones injected into the SPDIF optical input on the A1MZ main board, and the DSIO I^2S Receiver capturing I^2S digital data on the 24-bit I^2S output. THD+N results are shown (Figure 19 and Figure 20) for both 1 kHz at -1 dBFS and 11 kHz at -1 dBFS measured at approximately -144 dB. The noise floor is less than typical results for the DAC converters by -20 to -30 dB and should not affect the THD+N results for the DACs because it is less than the noise floor for the audio converters.

Figure 19 1 kHz at -1dBFS APx555 DSIO I^2S Loopback *Figure 20 11 kHz at -1dBFS APx555 DSIO I^2S Loopback*



DAC THD+N Performance Results with AD2437 Node Cumulative Jitter

Table 2 and Table 3 show the results of the THD+N testing using the Audio Precision APx555 Audio Analyzer. The THD+N test parameters were set to A-weighted, band-limited frequency range from 20 Hz through 20 kHz. Table 2 displays the results for the AD1955 DAC and Table 3 displays the results for the ADAU1966 DAC. Test tones were measured at 1 kHz and 11 kHz at levels of -1 dBFS and -40 dBFS and THD+N results are shown along with the corresponding jitter measurement at each node. Each row corresponds to either the first baseline direct I^2S to DAC measurement or THD+N numbers for each A^2B

sub-node. The sub node number corresponds to where the measurement was taken. For each test this was the last bus-powered sub-node on the A^{2}B bus.

Table 2 Results for AD2437 A1/MZ/B1MZ Sub Node I^{2}S Output Connections to the AD1955

Sub node # I2S Output	APx555 Measured Jitter	AD1955 THD+N 1kHz -1 dBFS	AD1955 THD+N 1kHz -40 dBFS	AD1955 THD+N 11 kHz -1 dBFS	AD1955 THD+N 11 kHz -40 dBFS
I2S → DAC	75 ps	-111.392 dBrA	-122.524 dBrA	-120.829 dBrA	-121.035 dBrA
Sub 0	1.37 ns	-109.747 dBrA	-120.747 dBrA	-99.182 dBrA	-122.041 dBrA
Sub 1	1.59 ns	-109.225 dBrA	-120.602 dBrA	-98.288 dBrA	-121.954 dBrA
Sub 2	1.73 ns	-108.712 dBrA	-120.581 dBrA	-97.749 dBrA	-121.839 dBrA
Sub 3	1.84 ns	-108.506 dBrA	-119.971 dBrA	-97.489 dBrA	-121.332 dBrA
Sub 4	1.95 ns	-108.072 dBrA	-120.488 dBrA	-97.121 dBrA	-121.776 dBrA
Sub 5	2.06 ns	-107.717 dBrA	-120.624 dBrA	-97.086 dBrA	-121.921 dBrA
Sub 6	2.14 ns	-107.434 dBrA	-120.594 dBrA	-97.028 dBrA	-121.864 dBrA
Sub 7	2.19 ns	-107.271 dBrA	-120.582 dBrA	-96.976 dBrA	-121.845 dBrA
Sub 8	2.28 ns	-107.182 dBrA	-120.642 dBrA	-96.936 dBrA	-121.868 dBrA
Sub 9	2.37 ns	-107.053 dBrA	-120.546 dBrA	-96.904 dBrA	-121.876 dBrA
Sub 10	2.45 ns	-106.937 dBrA	-120.655 dBrA	-96.856 dBrA	-121.857 dBrA
Sub 11	2.53 ns	-106.725 dBrA	-120.668 dBrA	-96.785 dBrA	-121.752 dBrA
Sub 12	2.58 ns	-106.605 dBrA	-120.611 dBrA	-96.523 dBrA	-121.811 dBrA
Sub 13	2.66 ns	-106.285 dBrA	-120.557 dBrA	-96.411 dBrA	-121.832 dBrA
Sub 14	2.72 ns	-106.087 dBrA	-120.625 dBrA	-96.576 dBrA	-121.812 dBrA
Sub 15	2.83 ns	-105.872 dBrA	-120.597 dBrA	-96.497 dBrA	-121.883 dBrA

Table 3 Results for AD2437 A1/MZ/B1MZ Sub Node I^{2}S Output Connections to the ADAU1966

Sub node # I2S Output	APx555 Measured Jitter	ADAU1966 THD+N 1kHz -1 dBFS	ADAU1966 THD+N 1kHz -40 dBFS	ADAU1966 THD+N 11 kHz -1 dBFS	ADAU1966 THD+N 11 kHz -40 dBFS
I2S → DAC	75 ps	-98.017 dBrA	-117.008 dBrA	-117.071 dBrA	-117.347 dBrA
Sub 0	1.37 ns	-97.578 dBrA	-114.133 dBrA	-90.847 dBrA	-116.272 dBrA
Sub 1	1.59 ns	-97.536 dBrA	-114.039 dBrA	-89.943 dBrA	-116.187 dBrA
Sub 2	1.73 ns	-97.349 dBrA	-113.985 dBrA	-89.649 dBrA	-116.136 dBrA
Sub 3	1.84 ns	-97.127 dBrA	-114.008 dBrA	-89.422 dBrA	-116.074 dBrA
Sub 4	1.95 ns	-97.033 dBrA	-113.989 dBrA	-89.161 dBrA	-116.053 dBrA
Sub 5	2.06 ns	-96.481 dBrA	-114.014 dBrA	-89.079 dBrA	-116.089 dBrA
Sub 6	2.14 ns	-96.402 dBrA	-113.981 dBrA	-89.005 dBrA	-116.057 dBrA
Sub 7	2.19 ns	-96.334 dBrA	-113.975 dBrA	-88.973 dBrA	-116.024 dBrA
Sub 8	2.28 ns	-96.206 dBrA	-113.982 dBrA	-88.927 dBrA	-116.022 dBrA
Sub 9	2.37 ns	-96.077 dBrA	-114.035 dBrA	-88.809 dBrA	-116.645 dBrA
Sub 10	2.45 ns	-96.007 dBrA	-114.027 dBrA	-88.769 dBrA	-116.018 dBrA
Sub 11	2.53 ns	95.911 dBrA	-113.945 dBrA	-88.635 dBrA	-115.975 dBrA

Sub node # I2S Output	APx555 Measured Jitter	ADAU1966 THD+N 1kHz -1 dBFS	ADAU1966 THD+N 1kHz -40 dBFS	ADAU1966 THD+N 11 kHz -1 dBFS	ADAU1966 THD+N 11 kHz -40 dBFS
Sub 12	2.58 ns	-95.851 dBrA	-114.013 dBrA	-88.613 dBrA	-115.912 dBrA
Sub 13	2.66 ns	-95.717 dBrA	-114.022 dBrA	-88.571 dBrA	-115.888 dBrA
Sub 14	2.72 ns	-95.552 dBrA	-113.969 dBrA	-88.338 dBrA	-115.805 dBrA
Sub 15	2.83 ns	-95.221 dBrA	-113.873 dBrA	-88.112 dBrA	-115.742 dBrA

Analyzing the THD+N Results for the AD1955 and ADAU1966

As these parts were *typical* AD2437 silicon at 25 ℃, the observed jitter measurements, (column two of Table 2 and Table 3) using the APx555 Audio Analyzer DSIO input from the A^{2}B bus sub node outputs, were approximately the expected values provided in Table 17 of the *AD2437 A2B Transceiver Datasheet*[1].

Examining the THD+N measurements for both DACs, a degradation in audio performance was recorded (measured in dBrA units) with increasing accumulated jitter at higher nodes. These measured results using typical lot parts installed on Analog Devices A^{2}B evaluation boards showed approximately a 6 dB reduction in THD+N for the AD1955 DAC and approximately 3 dB degradation in performance for the ADAU1966 DAC, at the maximum measurement RMS jitter of the A^{2}B bus. These results must be considered when reviewing the full-system measurements.

Based on measured results, it's apparent the AD1955 (an older/legacy ADI converter) suffers a larg degradation in performance, however its THD+N calculation with higher accumulated jitter still performed much better than the ADAU1966 DAC. The ADAU1966 datasheet provides an improved noise-immune design for the on-chip PLL and the design benefits the results, as it was less affected by the higher jitter on the clocks and the degradation that resulted was about one-half that for the AD1955.

For the audio engineer, the amount of acceptable degradation must be weighed, depending on the type of audio product to be designed. For a consumer or automotive audio design, anything between -90 to -95 dB THD+N might be acceptable or *good enough*. However, for a professional audio product using converters with over 120 dB in dynamic range, this degradation can be unacceptable. Potential mitigation strategies (discussed in XX-XREF) may need to be employed in the A^{2}B system to prevent adverse effects on the performance of the audio converters, which can derive their I^{2}S or TDM serial clocks and frame syncs from the A^{2}B bus recovered clock.

Additionally, the *AD2437 A2B Transceiver Datasheet*[1]. does specify worst-case jitter values. It is possible to see jitter values up to 60 to 70% higher than the typical TIE_{RMS} value. Expect an additional reduction in THD+N than the test results shown. As an additional data point, worst case jitter AD2437 parts in the 16-sub node test system, measured from 93.5 to 94 dB THD+N on the ADAU1966 DAC for a 5.5 nsec TIE_{RMS}

FFT Spectrum Diagrams for -1/-40 dBFS using 1 kHz/11 kHz Test Tones

Figure 21 through Figure 68 show different various FFT Spectrum plots from four THD+N tests. It measures the performance of the audio quality while connected directly to the ADI D/A Converter Evaluation Kits to establish a best case expected performance value (the *baseline* measurement). After the baseline plots, measured frequency spectrum plots are shown for I^{2}S audio output stages for sub node zero, sub node four, sub node eight, sub node twelve, and sub node sixteen for both DACs.

AD1955 and ADAU1966 1 kHz -1 dBFS Test Results

Figure 21 and Figure 22 show the FFT spectrum analysis plots for the baseline direct I²S connection to the DACs from the Audio Processor, followed by spectrum plots (Figure 23 through Figure 32) for the A²B bus configurations of sub node 0, 4, 8, 12, and 15 where the A²B sub node I²S output is fed to each DAC. The results are based on a 1 kHz input sine wave at-1 dBFS.

Figure 21 1 kHz, -1 dBFS APx555 to AD1955 Only

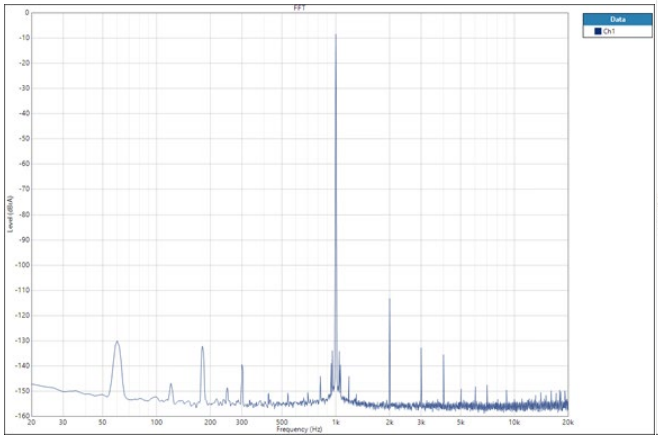


Figure 22 1 kHz, -1 dBFS APx555 to ADAU1966

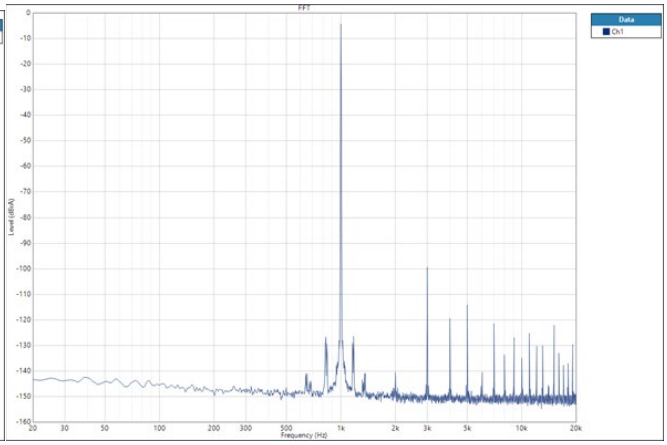


Figure 23 1 kHz, -1 dBFS S0 I²S to AD1955

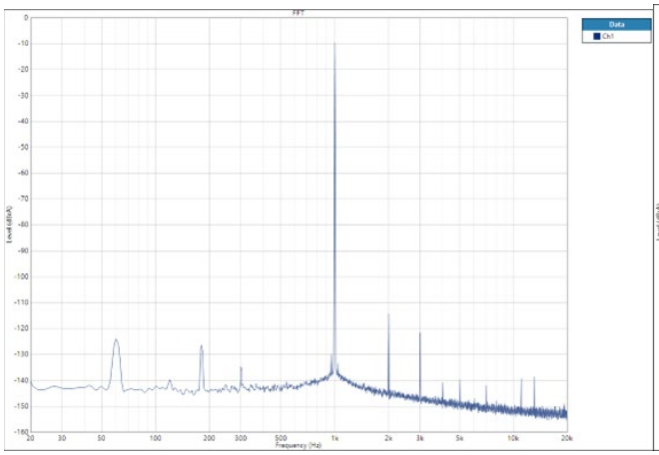


Figure 24 1 kHz, -1 dBFS S0 I²S to ADAU1966

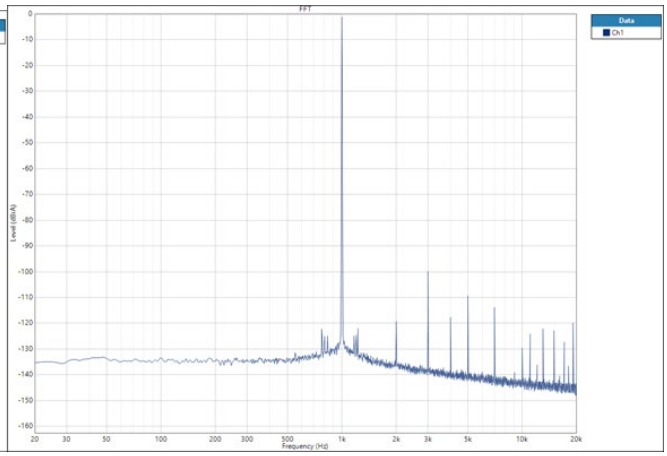


Figure 25 1 kHz, -1 dBFS S4 I²S to AD1955

Figure 26 1 kHz, -1 dBFS S4 I²S to ADAU1966

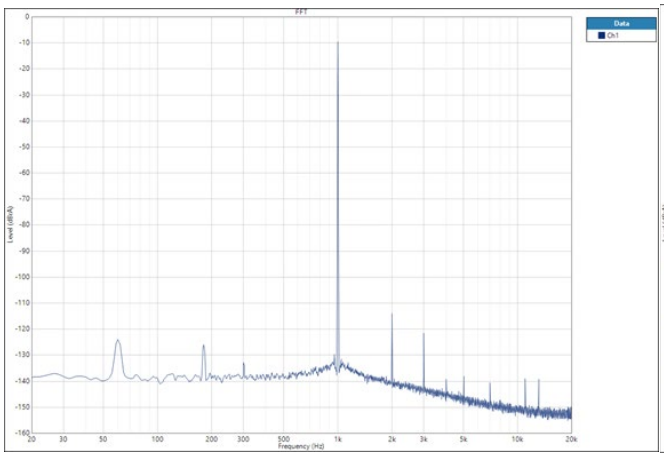


Figure 27 1 kHz, -1 dBFS S8 I²S to AD1955

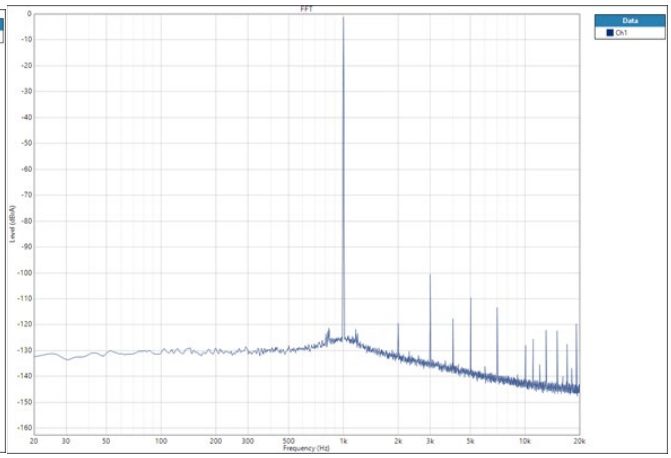


Figure 28 1 kHz, -1 dBFS S8 I²S to ADAU1966

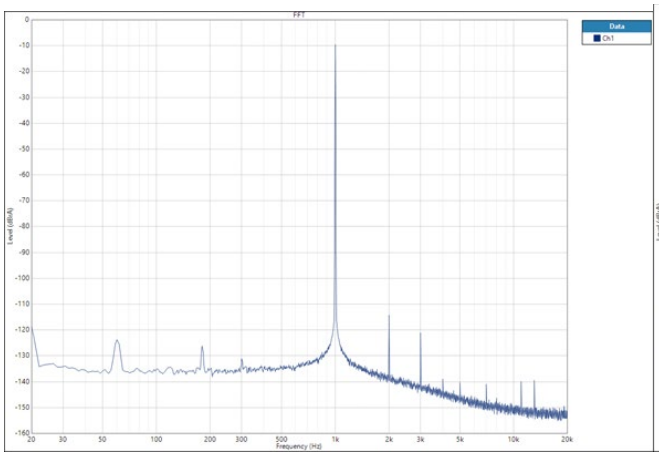


Figure 29: 1 kHz, -1 dBFS S12 I²S to AD1955

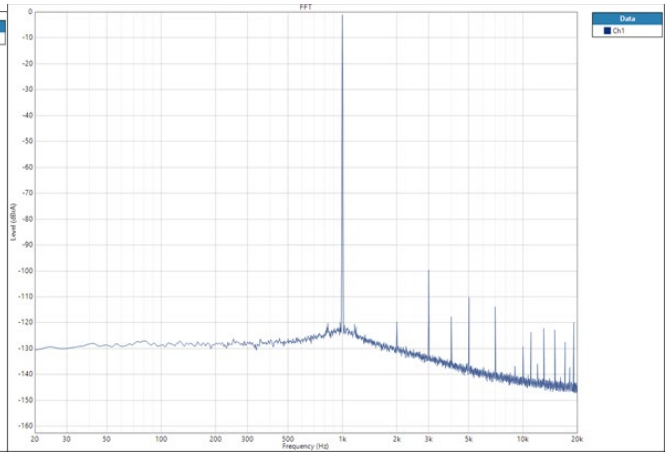
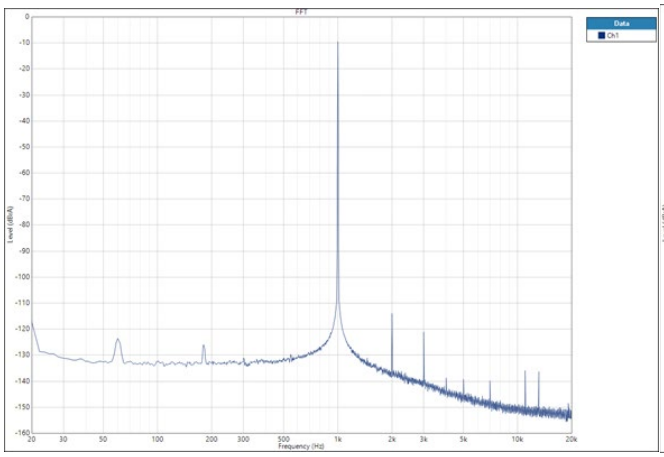


Figure 30 1 kHz, -1 dBFS S12 I²S to ADAU1966



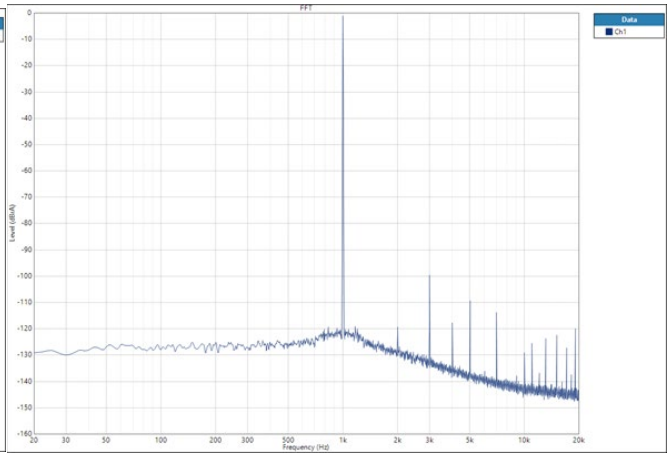


Figure 31: 1 kHz, -1 dBFS S15 I²S to AD1955

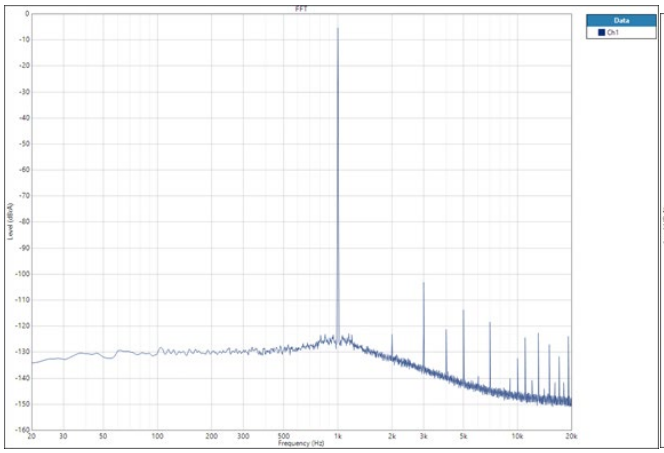


Figure 32: 1 kHz, -1 dBFS S15 I²S to ADAU1966

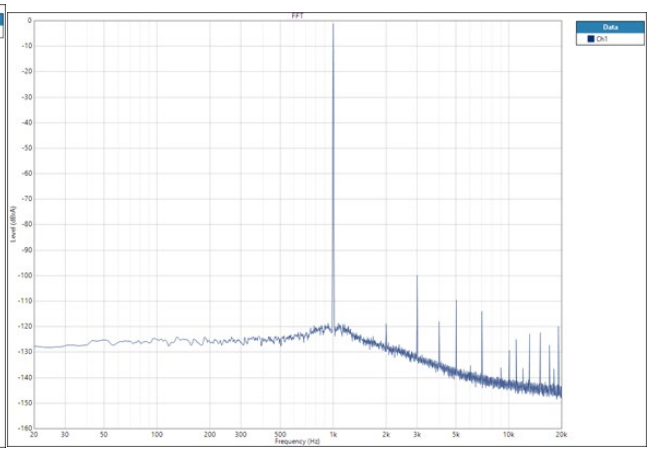


Figure 21 through Figure 32 Observations. The noise floor (measure of the noise density in dBm/Hz or the noise power in a signal of 1 Hz bandwidth) is raised significantly in the first sub node, and it is raised incrementally further as the number of nodes increases. The AD1955 low-frequency content eventually disappears into noise floor. Some higher frequency harmonics and noise are generated at higher-numbered nodes which do not exist for the initial baseline results, especially visible in the last node (sub node 15) for both the AD1955 and ADAU1966.

AD1955 and ADAU1966 1 kHz -40 dBFS Test Results

Figure 33 and Figure 34 show the FFT spectrum analysis plots for the baseline direct I²S connection to the DACs from the Audio Processor, followed by A²B bus configurations of sub node 0, 4, 8, 12, and 15 where the A²B sub node I²S output is fed to each DAC (Figure 35 through Figure 44). The results are based on a 1 kHz input sine wave at -40 dBFS.

Figure 33 1 kHz, -40 dBFS APx555 to AD1955 Only

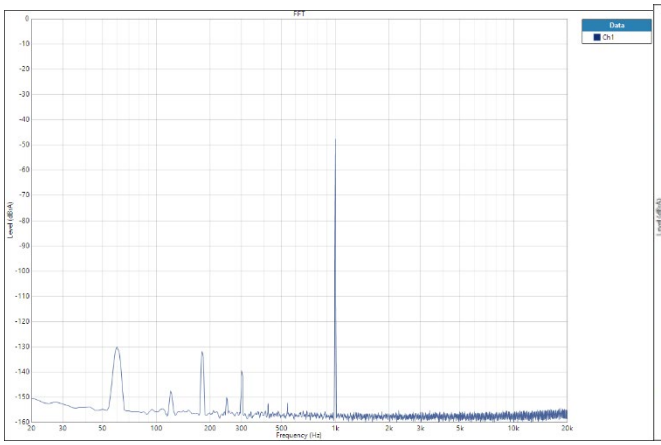


Figure 34 1 kHz, -40 dBFS APx555 to ADAU1966

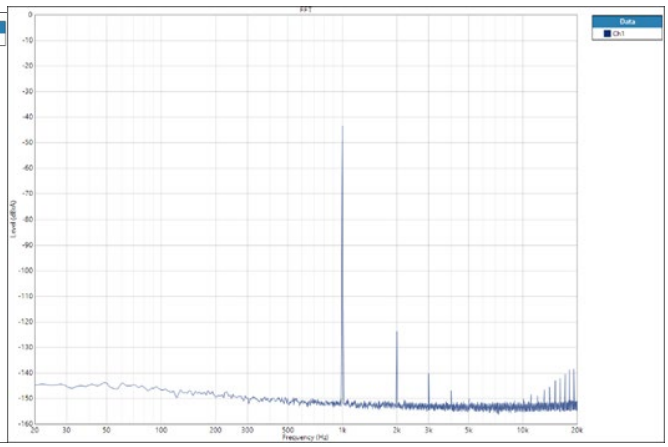


Figure 35: 1 kHz, -40 dBFS S0 I²S to AD1955

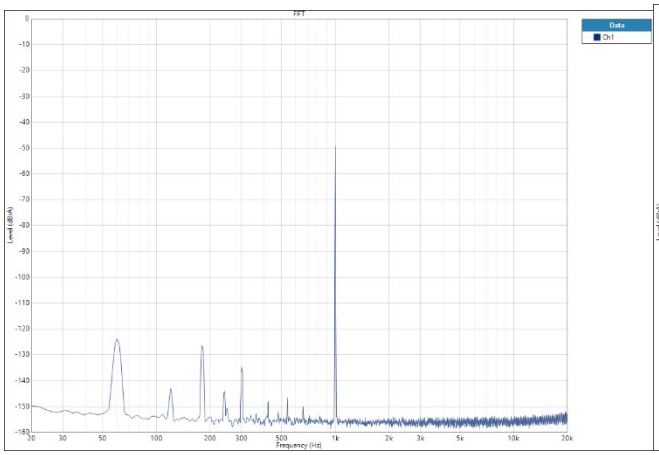


Figure 36 1 kHz, -40 dBFS S0 I²S to ADAU1966

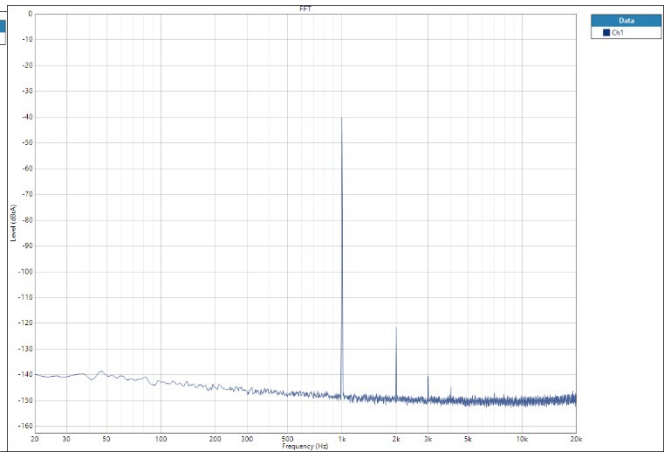


Figure 37 1 kHz, -40 dBFS S4 I²S to AD1955

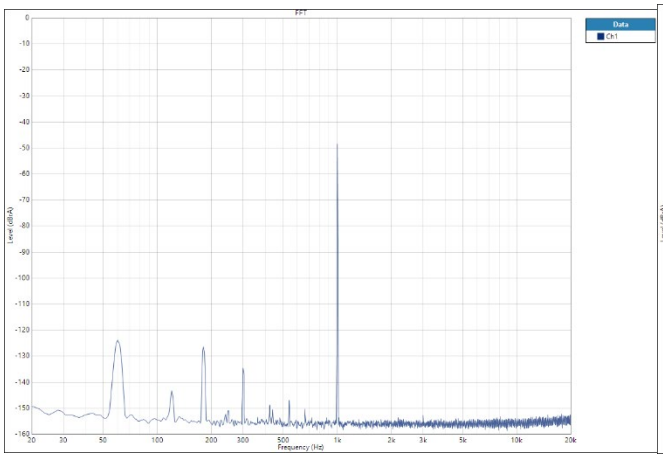


Figure 38 1 kHz, -40 dBFS S4 I²S to ADAU1966

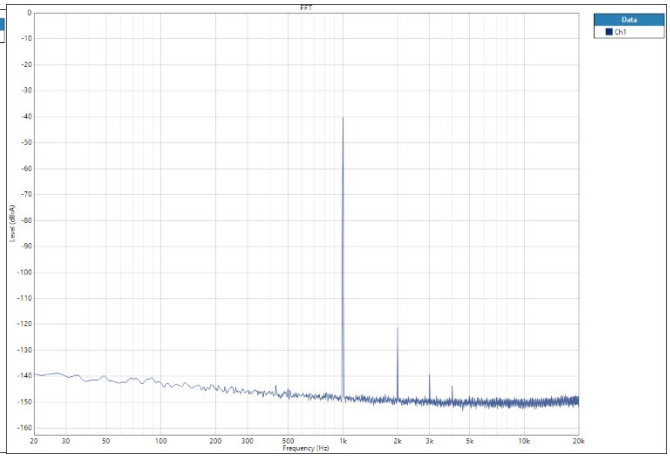


Figure 39 1 kHz, -40 dBFS S8 I²S to AD1955

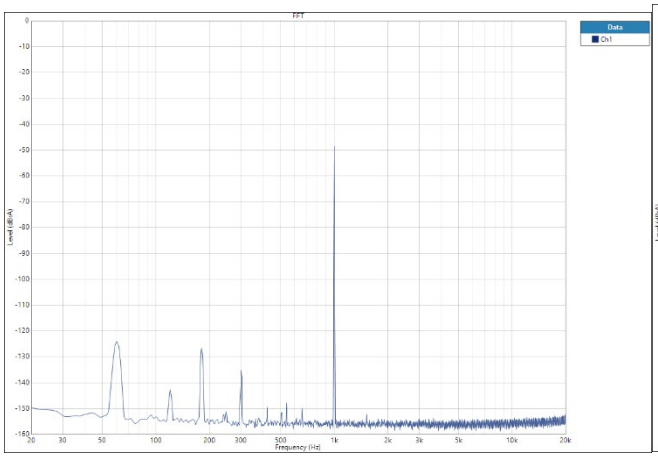


Figure 40 1 kHz, -40 dBFS S8 I²S to ADAU1966

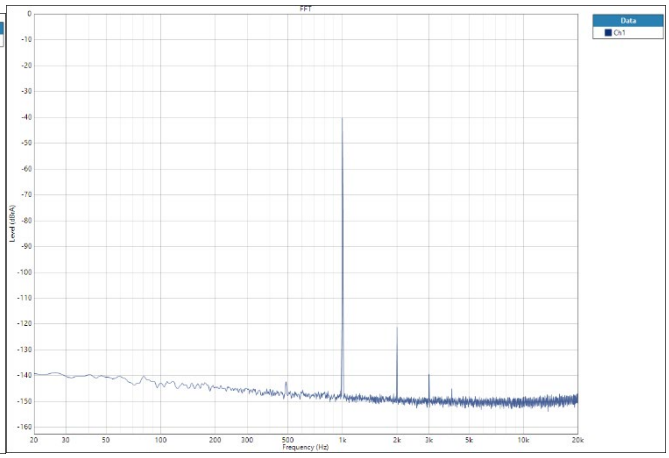


Figure 41 1 kHz, -40 dBFS S12 I²S to AD1955

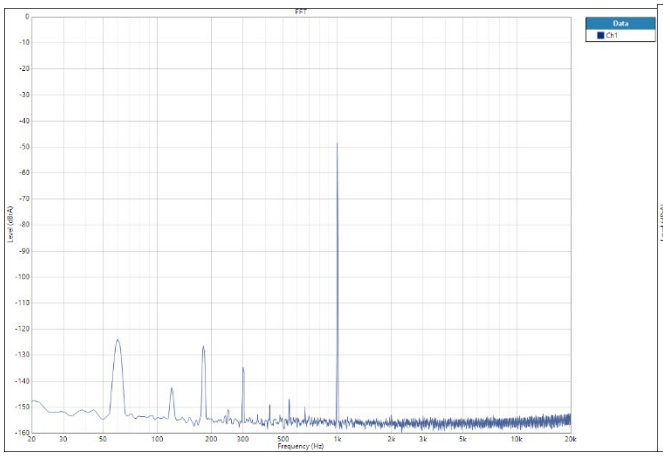


Figure 42 1 kHz, -40 dBFS S12 I²S to ADAU1966

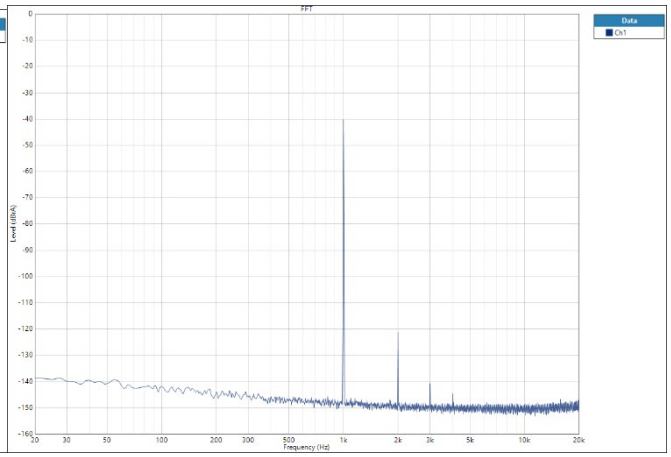


Figure 43 1 kHz, -40 dBFS S15 I²S to AD1955

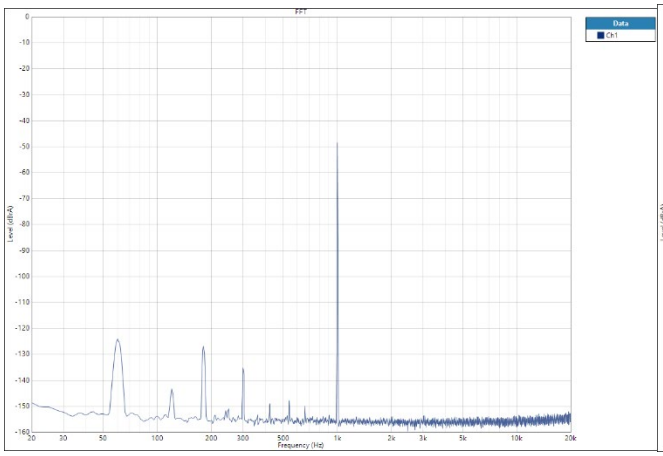


Figure 44 1 kHz, -40 dBFS S15 I²S to ADAU1966

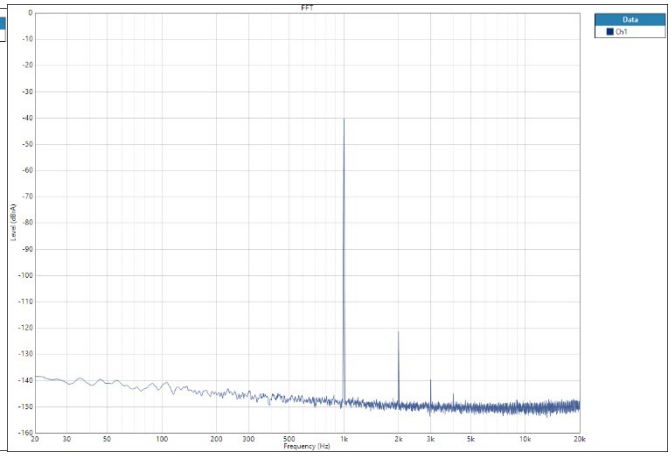


Figure 33 Through Figure 44 Observations. The noise floor at -40 dB is not much different than the baseline case. Perhaps worst case is two to three dB increase in noise floor for higher-numbered nodes. An observation is that the baseline spectrum for the ADAU1966 shows some high frequencies noise or harmonics between 10 kHz and 20 kHz, and the noise vanishes when the I²S data is received from the A²B bus and higher-jitter clock.

AD1955 and ADAU1966 11 kHz Test Results at -1 dBFS

Figure 45 and Figure 46 show the FFT spectrum analysis plots for the baseline direct I²S connection to the DACs from the Audio Processor, followed by A²B bus configurations (Figure 47 through Figure 56) for sub node zero, sub node four, sub node eight, sub node twelve, and sub node fifteen where the A²B sub node I²S output is fed to each DAC. The results are based on a 11 kHz input sine wave at -1 dBFS.

Figure 45 11 kHz, -1 dBFS APx555 to AD1955 Only

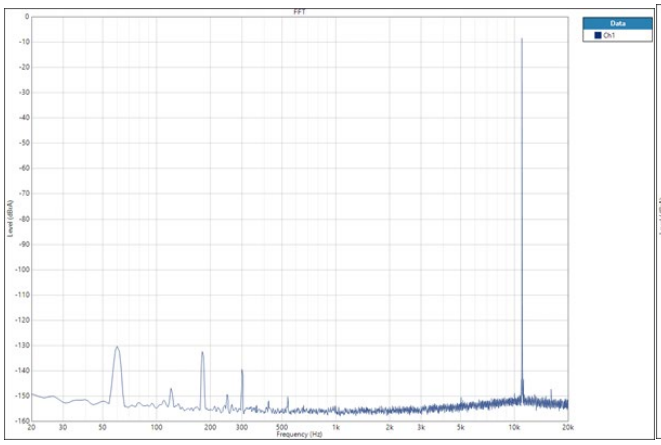


Figure 46 11 kHz, -1 dBFS APx555 to ADAU1966

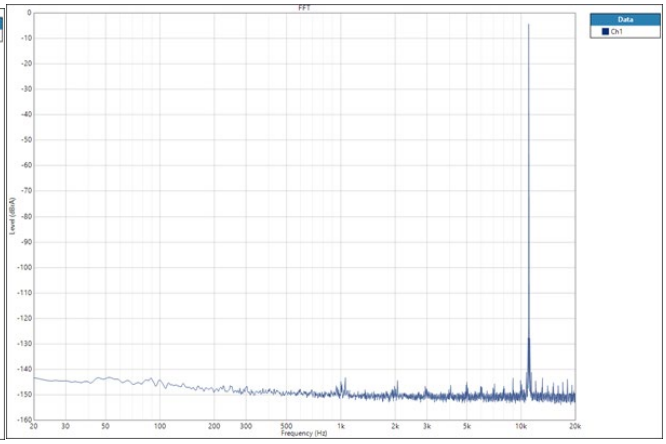


Figure 47 11 kHz, -1 dBFS S0 I²S to AD1955 Only

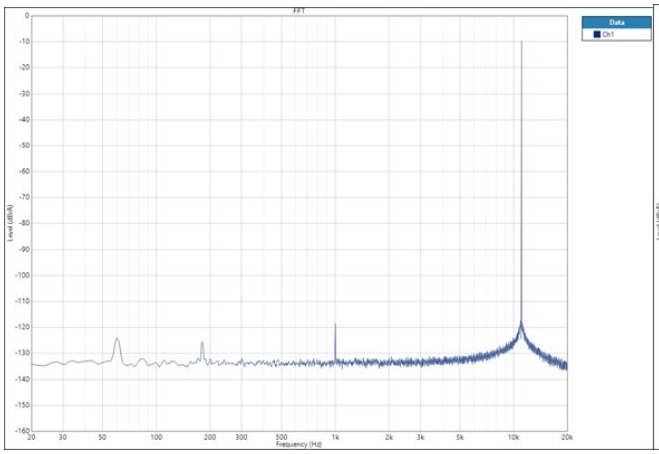


Figure 48 11 kHz, -1 dBFS S0 I²S to ADAU1966

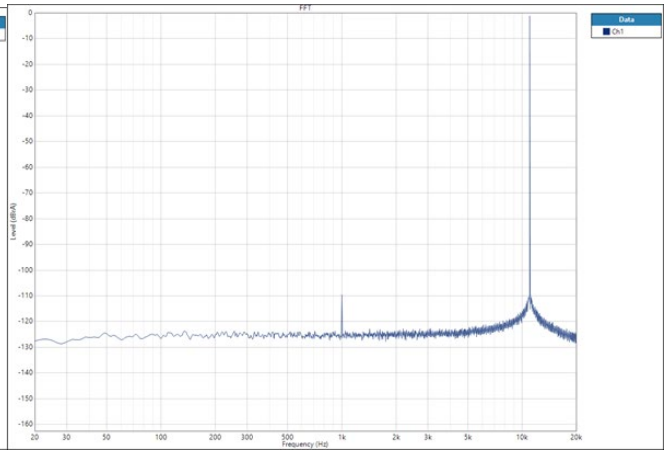


Figure 49 11 kHz, -1 dBFS S4 I²S to AD1955 Only

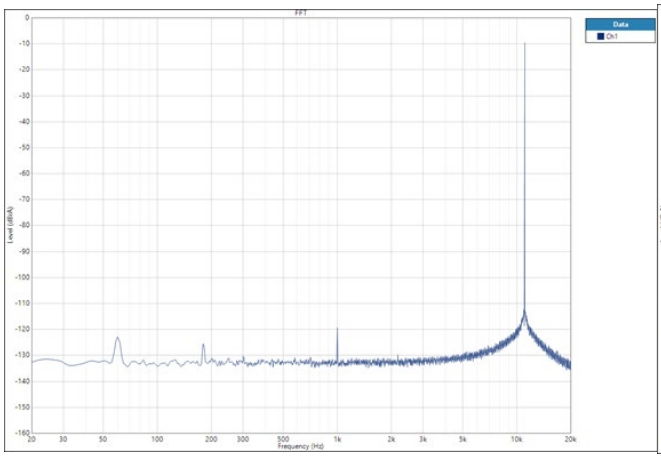


Figure 50 11 kHz, -1 dBFS S4 I²S to ADAU1966

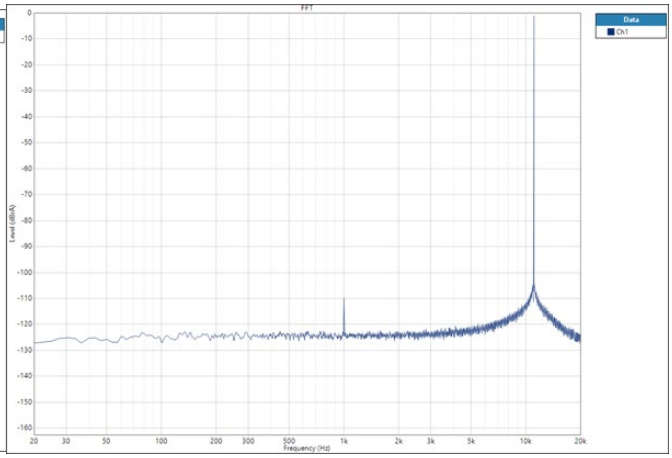


Figure 51 11 kHz, -1 dBFS S8 I²S to AD1955 Only

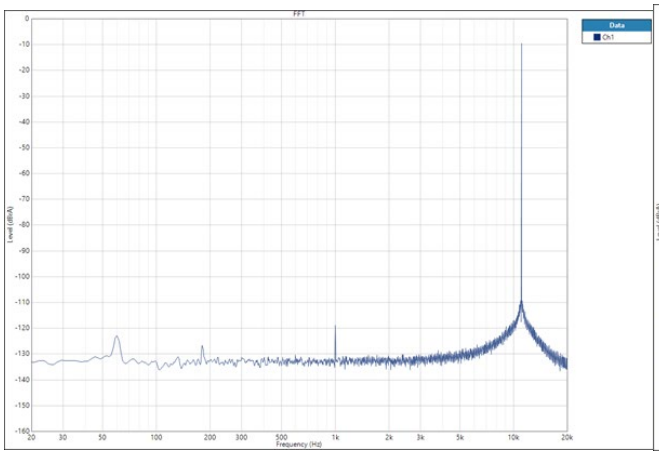


Figure 52 11 kHz, -1 dBFS S8 I²S to ADAU1966

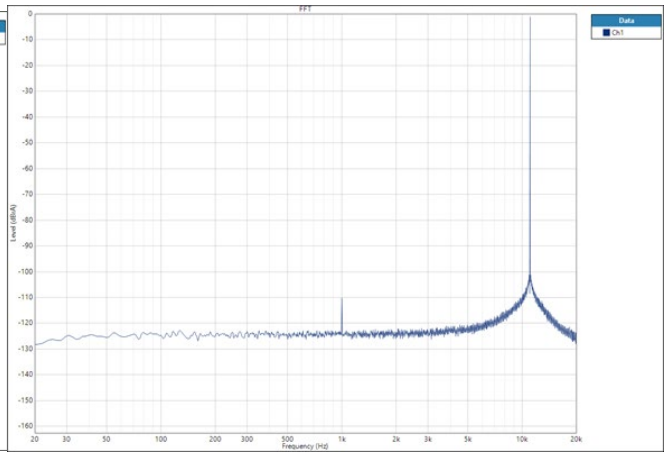


Figure 53 11 kHz, -1 dBFS S12 I²S to AD1955 Only

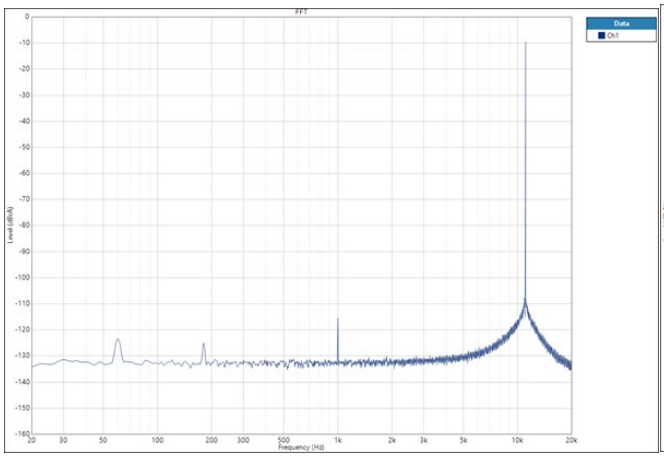


Figure 54 11 kHz, -1 dBFS S12 I²S to ADAU1966

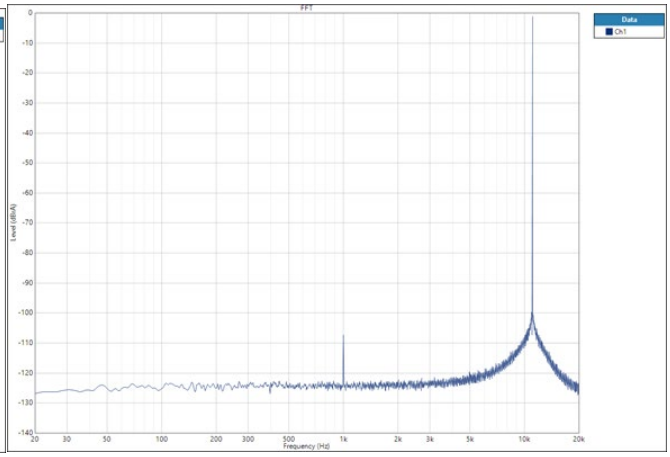


Figure 55 11 kHz, -1 dBFS S15 I²S to AD1955 Only

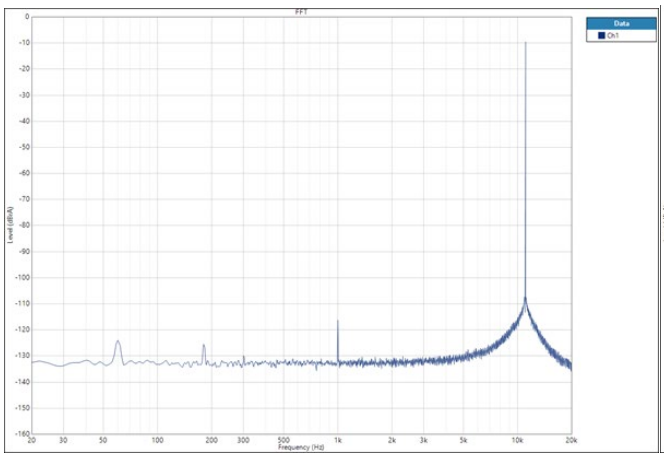


Figure 56 11 kHz, -1 dBFS S15 I²S to ADAU1966

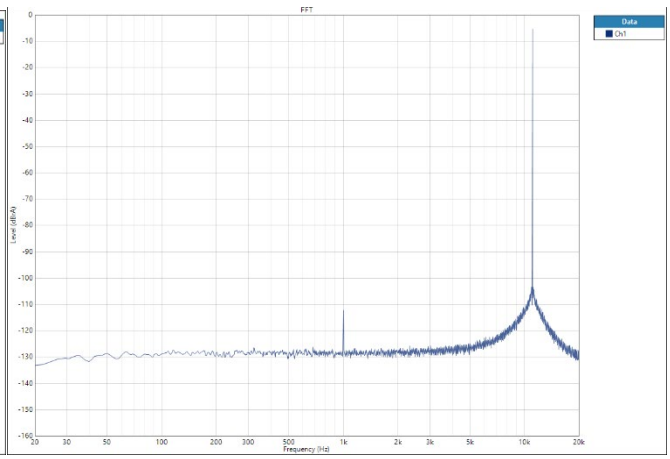


Figure 45 Through Figure 56 Observations. Once again, at -1 dB the noise floor is raised significantly, especially around the 11 kHz signal, and is raised further for the higher-numbered nodes. The low frequency content again eventually vanishes into the noise floor. Both the AD1955 and ADAU1966 DAC show harmonic or tone at 1 kHz. The accumulated jitter causes this mysterious tone to display for both DACs, approximating -110 dB to -120 dB.

AD1955 and ADAU1966 11 kHz Test Results at -40 dBFS

Figure 57 and Figure 58 show the FFT spectrum analysis plots the baseline direct I^2S connection to the DACs from the AP, followed by A^2B bus configurations (Figure 59 through Figure 68) of sub node zero, sub node four, sub node eight, sub node twelve, and sub node fifteen where the A^2B sub node I^2S output is fed to each DAC. The results are based on a 11 kHz input sine wave at -1 dBFS.

Figure 57 11 kHz, -40 dBFS APx555 to AD1955 Only

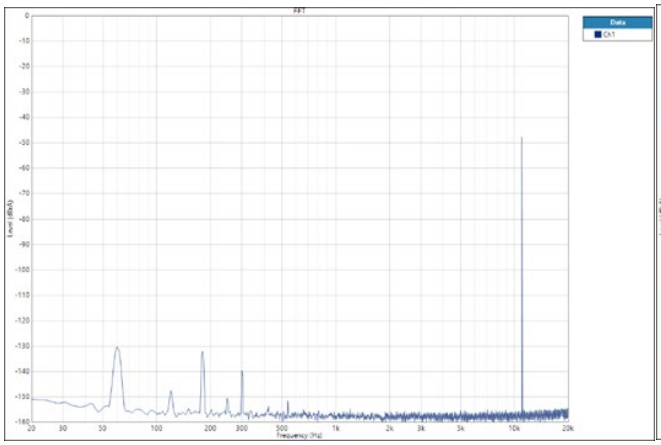


Figure 58 11 kHz, -40 dBFS AP I^2S out to ADAU1966

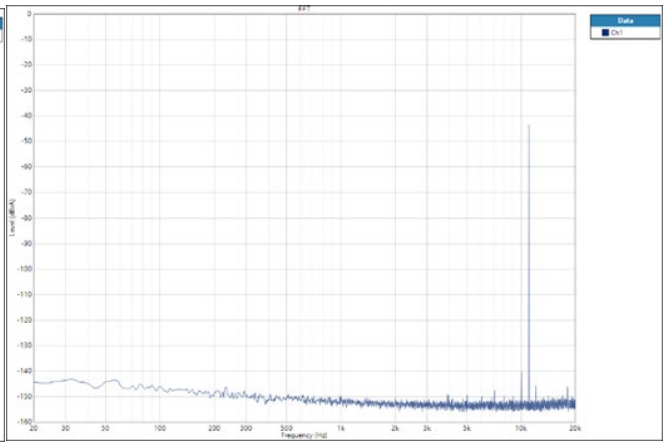


Figure 59: 11 kHz, -40 dBFS S0 I^2S to AD1955 Only

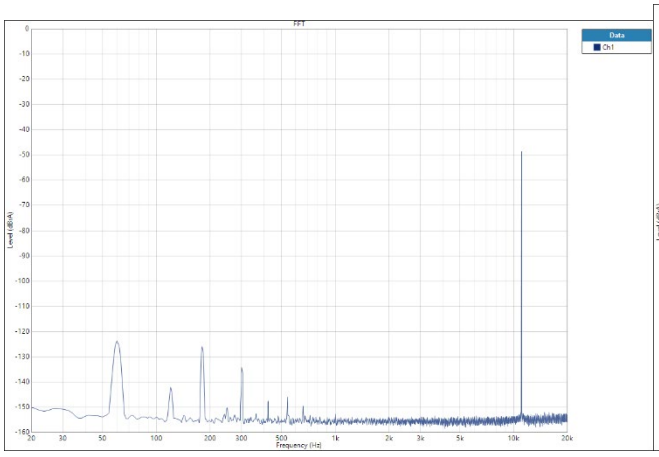


Figure 60 11 kHz, -40 dBFS S0 I^2S to ADAU1966

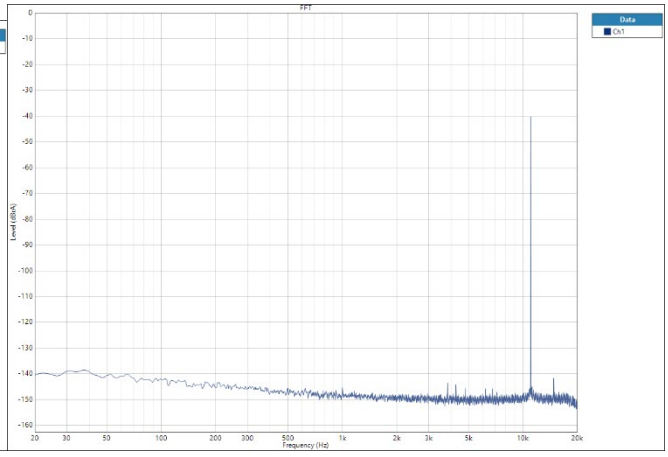


Figure 61 11 kHz, -40 dBFS S4 I²S to AD1955 Only

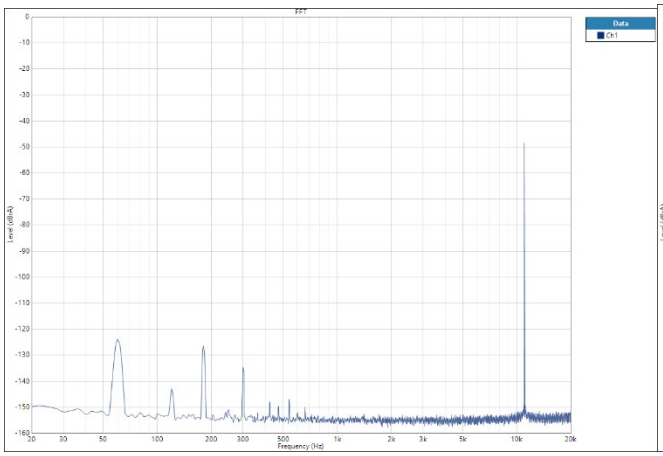


Figure 62 11 kHz, -40 dBFS S4 I²S to ADAU1966

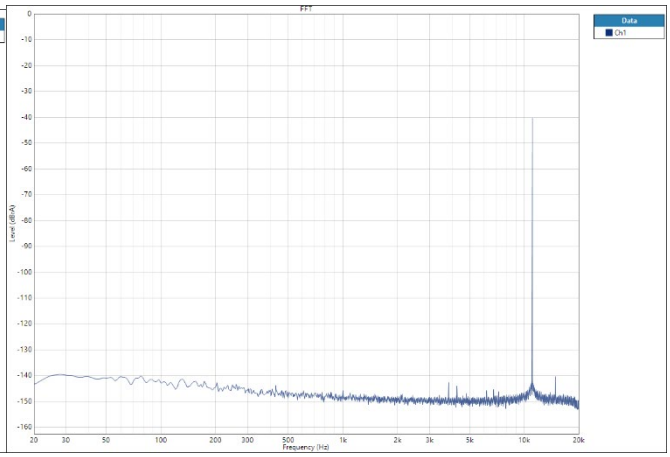


Figure 63 11 kHz, -40 dBFS S8 I²S to AD1955 Only

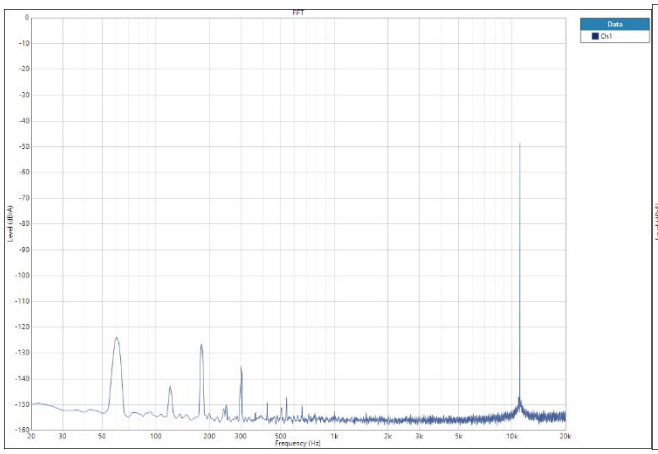


Figure 64 11 kHz, -40 dBFS S8 I²S to ADAU1966

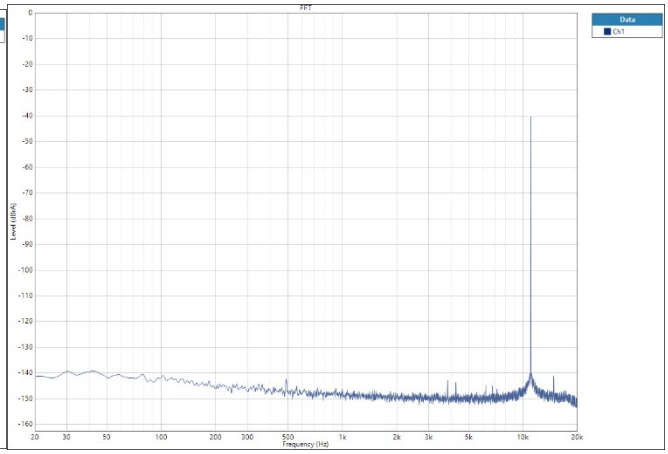


Figure 65 11 kHz, -40 dBFS S12 I²S to AD1955 Only

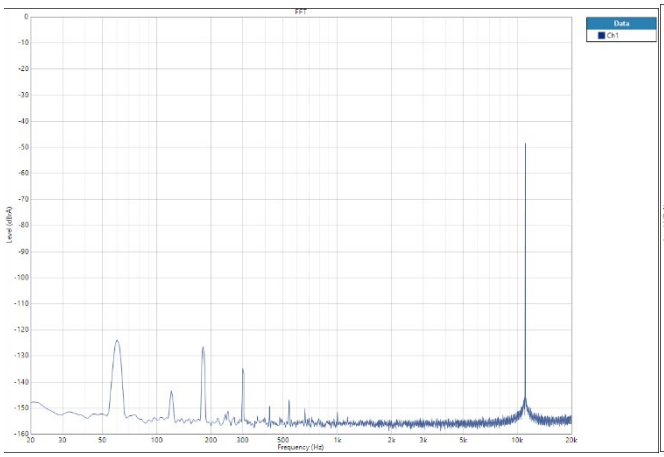


Figure 66 11 kHz, -40 dBFS S12 I²S to ADAU1966

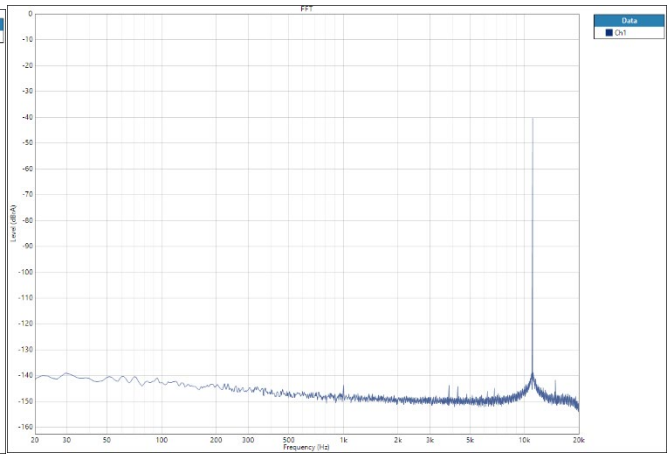


Figure 67 11 kHz, -40 dBFS S15 I²S to AD1955 Only

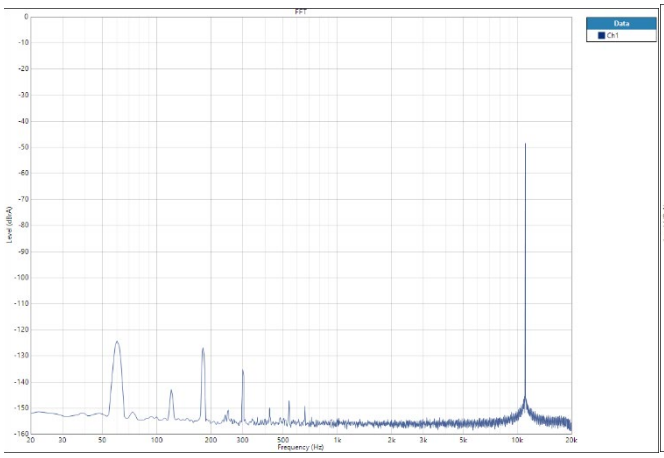


Figure 68 11 kHz, -40 dBFS S15 I²S to ADAU1966

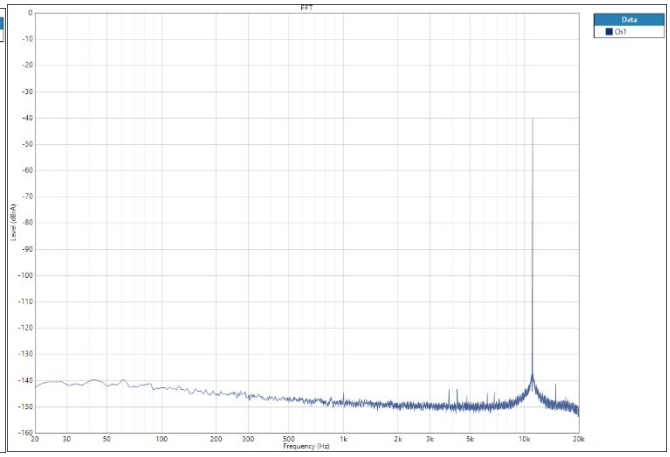


Figure 57 through Figure 68 Observations. The noise floor is not much different (slightly higher) than the baseline case with degradation of THN+N is approximately -1.5 dB for higher-numbered nodes. For the ADAU1966 some of the frequencies between 5K to 20K are raised by approximately 5 dB, while others vanish as compared to baseline I²S case.

Strategies for Mitigation of Audio Degradation

For system designs using ADCs and DACs, onboard PLLs with more robust specifications ensure a cleaner clock signal for the converters, reducing the performance degradation of the audio signals.

However, when the DAC performance is still affected by the accumulated jitter in the recovered I²S bit and word clocks, possible methods to mitigate the audio degradation due to accumulated jitter effects are:

- Perform a sample rate conversion at the DAC to align the samples to a clean clock signal. This is possible because the maximum accumulation of jitter is measured in single-digit nanoseconds, but the digital data remains correct. Resampling to a clean, low-jitter clock reference for the master I²S output of the rate converter eliminates the THD+N degradation and reduces the clock jitter on the serial bus to a range of 100 to 200 picoseconds.

- Use a low-bandwidth PLL or Jitter Attenuator (JA) device to remove the upper-frequency components of the jitter on the recovered clock. This provides a similar performance benefit as the resampling data to a different master clock source. Jitter can be reduced to less than 100 picoseconds.

Solution One-Use a HW ASRC to Improve DAC THD+N Performance on Sub Nodes

Asynchronous sample rate conversion (ASRC) is a technique normally used to convert between audio streams running at different sample rates, or to perform sample rate conversion between audio streams running at the same sample rate but with different clock domains, such as a 48-kHz to 48-kHz rate conversion. An ASRC will convert the sample rate of a digital signal without locking the output clock to the input clock. The output clock can clock the audio data free from jitter effects of the input clock for the audio data samples. ASRCs can modify the sampling frequence in small increments over time without producing audible artifacts. Thus, we can utilize this rate conversion to transfer the same audio data to a

new clock domain, and specifically in the case of a A^{2}B-recovered clock, move the resampled data synchronized to a new I^{2}S master with significantly less jitter (free) master clock, bit clock, and frame sync.

This next test case uses the same A^{2}B 16-node system, but with a HW ASRC inserted between the last node and the DAC board. For this test, an *EVAL-ADAU1452 Obsolete Evaluation Board*[26] was used. Although the A1MZ LPS evaluation kit uses the obsolete ADAU1452, the expansion header did not expose the right I^{2}S outputs for transmitting rate-converted audio to the DAC boards.

Figure 69 shows the functional block diagram defining the necessary connections required between the EVAL-AD2437B1MZ sub node, the ADAU1452MINIZ board, and the AD1955 or ADAU1966 eval kits. The ADAU1452MINIZ board receives I^{2}S audio on SPORT2 and transmits rate-converted audio on SPORT3. These signals are accessible on header J3 and the various test points provided on the board. Figure 70 and Figure 71 shows the actual test setup between the three boards using jumper wires to connect the I^{2}S pins between the A^{2}B transceiver, the DSP, and the DAC.

Figure 69 Test Setup with Sub Node 15 Connection to ADAU1452's ASRC0 to ADAU1966 DAC

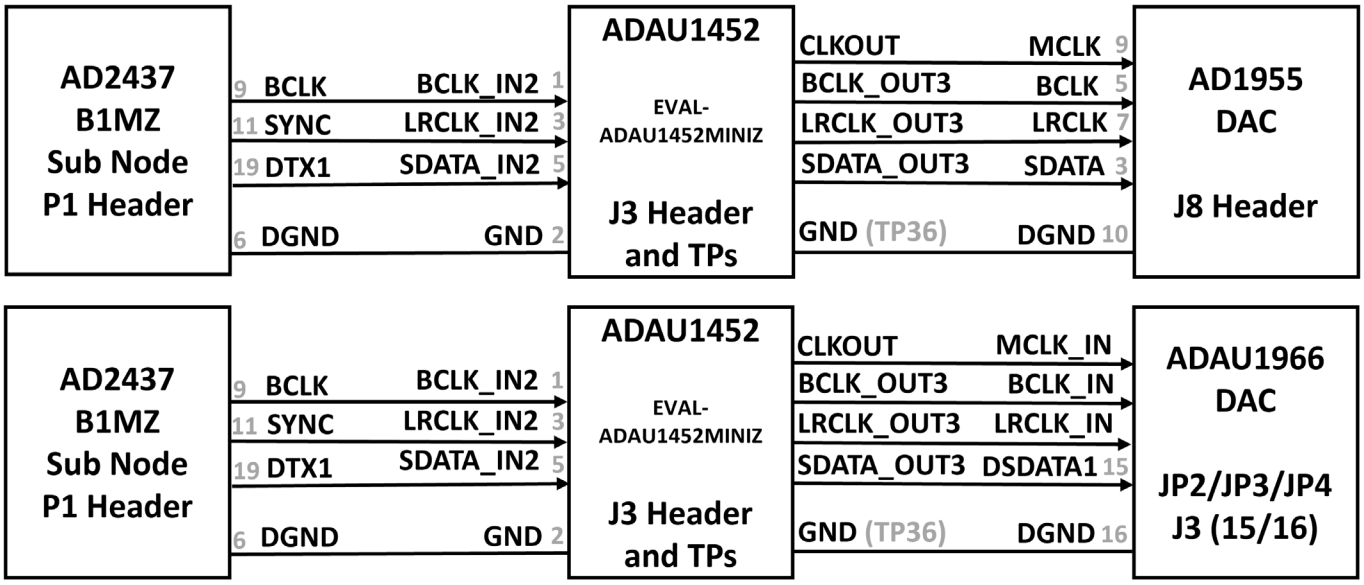


Figure 70 Test Setup with Sub Node 15 Connection to ADAU1452's ASRC0 to ADAU1966 DAC

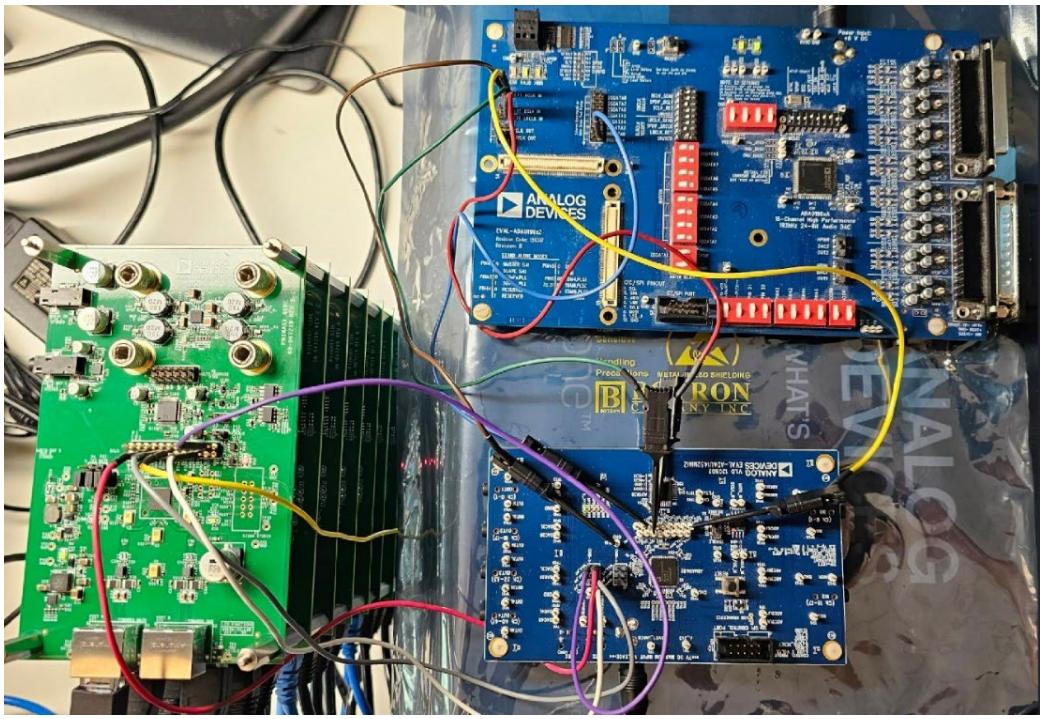
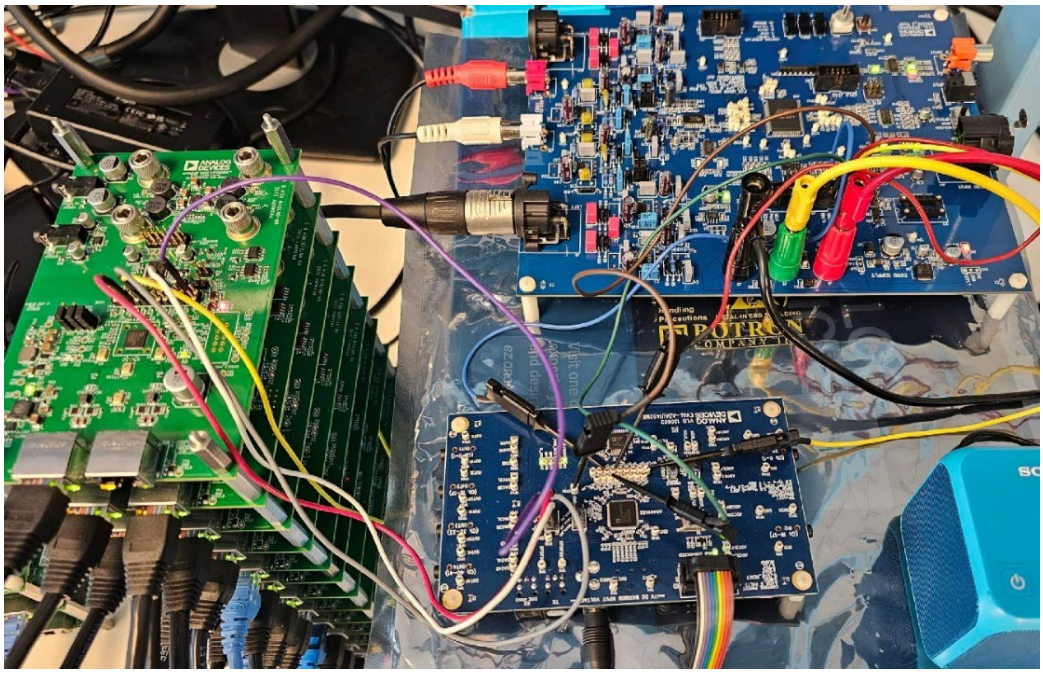
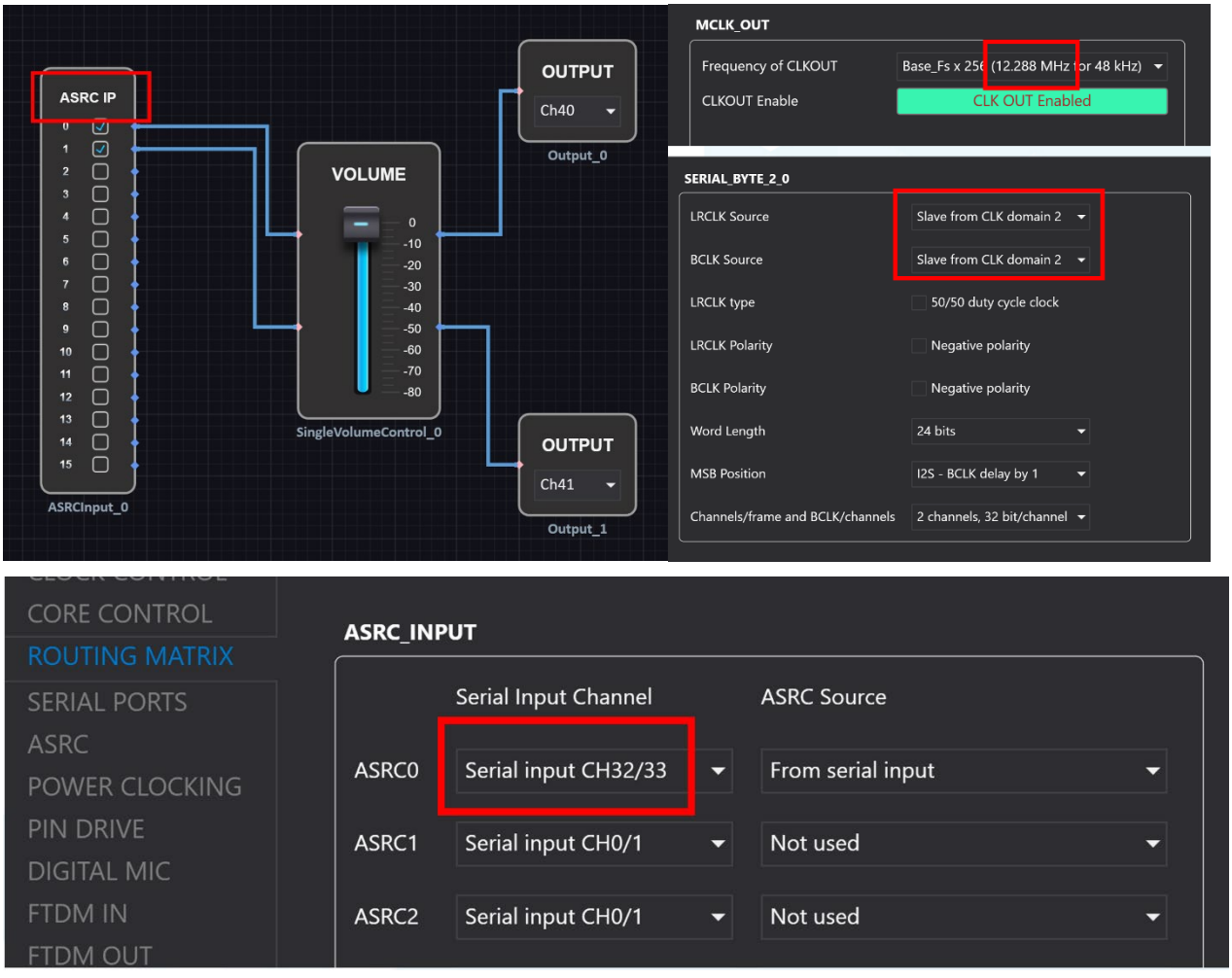


Figure 71 Test Setup with Sub Node 15 Connection to ADAU1452's ASRC0 to 1955 DAC



To configure the ADAU1452 evaluation kit, use the SigmaStudio+ 2.0 schematic project for a simple passthrough of audio data coming from SPORT2, which is connected to the A1MZ last sub node I²S output. The I²S data on SPORT2 is connected to ASRC0. The output of ASRC0 is fed to the ADAU1452 Sigma300 DSP core, which does an audio *talkthru* out to the channels associated with SPORT3 (configured as an I²S master). Last, configure the CLKOUT to generate a 12.288 MHz. This is needed to drive the MCLK inputs for the AD1955 and ADAU1966. The project settings in Figure 72 configure the ASRC0, SPORT2, SPORT3, and CLKOUT/MCLK. The settings are the I²S slave SPORT2 input to SPORT3 Master I²S output using ASRC0, plus generating a 12.288 MHZ Master CLKOUT for the ADAU1966 and AD1955 MCLK Source

Figure 72 SigmaStudio+ ADAU1452 Project Settings



DAC THD+N Performance Results with ADAU1452 Integrated HW ASRC

Tables 4 and Tables 5 below show the measured results when adding the ADAU1452 ASRC (asynchronous sample rate converter) block in the signal path between the last "nth" sub node in the A2B system and the connection to the AD1955 or ADAU1966 DAC. First in the test, the jitter was measured on the output of the ADAU1452 I2S output after passing through the HW ASRC block (note: this measured jitter is the same for both tables 4 and 5 and only done once before measuring the THD+N performance for each of the D/A converters). Compared to the previous measured accumulated jitter results shown in Tables 2 and 3, the measured jitter at the ADAU1452 DSP's ASRC/I2S out path showed a significantly reduction from the accumulated A2B bus jitter to now only about 100 to 240 picoseconds of jitter for BCLK and SYNC clocks. The THD+N measurements in the table below shows that the reduced jitter resulted in a much-improved THD+N performance matching the datasheet typical THD+N values for both the AD1955 and ADAU1966. This was regardless of the addition of any higher number of nodes in the A2B system. The results are almost identical for each node. Thus, the use of the ASRC demonstrates the benefit of reduced I2S clock jitter which also provides optimal THD+N performance for the D/A converters – once sensitive to accumulated clock jitter affects. For example, the results below show the DAC performance is equal to the datasheet typical THD+N numbers of -110 dB for the AD1955 and -98 dB at for the ADAU1966 using a tone generated at 1 kHz and -1 dBFS.

Table 4. AD1955 THD+N Results with ASRC Inserted Between Sub Node [n] Path to DAC

Sub node # I2S Output	APx555 Measured Jitter	AD1955 THD+N 1kHz -1 dBFS	AD1955 THD+N 1 kHz -40 dBFS	AD1955 THD+N 11 kHz -1 dBFS	AD1955 THD+N 11 kHz -40 dBFS
I2S → DAC	75 ps	-111.392 dBrA	-122.524 dBrA	-120.829 dBrA	-121.035 dBrA
Sub 0	185 ps	-110.931 dBrA	-118.209 dBrA	-116.212 dBrA	-119.529 dBrA
Sub 1	217 ps	-111.028 dBrA	-119.107 dBrA	-116.433 dBrA	-120.359 dBrA
Sub 2	101 ps	-111.037 dBrA	-119.797 dBrA	-116.521 dBrA	-120.859 dBrA
Sub 3	215 ps	-111.085 dBrA	-119.447 dBrA	-116.404 dBrA	-120.816 dBrA
Sub 4	211 ps	-111.012 dBrA	-118.973 dBrA	-115.773 dBrA	-120.554dBrA
Sub 5	109 ps	-111.067 dBrA	-118.655 dBrA	-116.027 dBrA	-119.993 dBrA
Sub 6	214 ps	-111.037 dBrA	-118.236 dBrA	-116.256 dBrA	-119.390 dBrA
Sub 7	219 ps	-110.658 dBrA	-117.346 dBrA	-115.623 dBrA	-118.586 dBrA
Sub 8	189 ps	-110.562 dBrA	-116,266 dBrA	-115.137 dBrA	-117.767 dBrA
Sub 9	187 ps	-111.353 dBrA	-116.747 dBrA	-115.758 dBrA	-118.057 dBrA
Sub 10	199 ps	-110.555 dBrA	-116.354 dBrA	-115.432 dBrA	-117.930 dBrA
Sub 11	228 ps	-111.201 dBrA	-120.280 dBrA	-116.736 dBrA	-121.713 dBrA
Sub 12	251 ps	-111.758 dBrA	- 118.549 dBrA	-116.102 dBrA	-120.144 dBrA
Sub 13	238 ps	-111.027 dBrA	-119.033 dBrA	-115.206 dBrA	-120.338 dBrA
Sub 14	234 ps	-110.898 dBrA	-118.653 dBrA	-115.643 dBrA	-119.748 dBrA
Sub 15	193 ps	-110.334 dBrA	-118.629 dBrA	-114.998 dBrA	-119.762 dBrA

Table 5 ADAU1966 THD+N Results with ASRC Inserted Between Sub Node [n] Path to DAC

Sub node # I2S Output	APx555 Measured Jitter	ADAU1966 THD+N 1 kHz -1 dBFS	ADAU1966 THD+N 1 kHz -40 dBFS	ADAU1966 THD+N 11 kHz -1 dBFS	ADAU1966 THD+N 11 kHz -40 dBFS
I2S → DAC	75 ps	-98.017 dBrA	-117.008 dBrA	-117.071 dBrA	-117.347 dBrA
Sub 0	185 ps	-98.394 dBrA	-113.801 dBrA	-112.500 dBrA	-116.131 dBrA
Sub 1	217 ps	-98.386 dBrA	-113.752 dBrA	-112.617 dBrA	-116.044 dBrA
Sub 2	101 ps	-98.499 dBrA	-113.954 dBrA	-112.476 dBrA	-116.325 dBrA
Sub 3	215 ps	-98.354 dBrA	-113.872 dBrA	-112.543 dBrA	-116.307 dBrA
Sub 4	211 ps	-98.260 dBrA	-113.638 dBrA	-112.342 dBrA	-116.147 dBrA
Sub 5	109 ps	98.264 dBrA	-113.711 dBrA	-112.637 dBrA	-116.271 dBrA
Sub 6	214 ps	-98.241 dBrA	-113.937 dBrA	-112.515 dBrA	-116.561 dBrA
Sub 7	219 ps	-98.176 dBrA	-113.786 dBrA	-112.412 dBrA	-116.145 dBrA
Sub 8	189 ps	-98.325 dBrA	-113.800 dBrA	- 112.434 dBrA	-116.188 dBrA
Sub 9	187 ps	-98.268 dBrA	-113.725 dBrA	-112.436 dBrA	-116.038 dBrA
Sub 10	199 ps	-98.254 dBrA	-113.643 dBrA	-112.449 dBrA	-116.341 dBrA
Sub 11	228 ps	-98.347 dBrA	-113.733 dBrA	-112.568 dBrA	-116.067 dBrA
Sub 12	251 ps	-98.180 dBrA	-113.661 dBrA	-112.079 dBrA	-115.991 dBrA
Sub 13	238 ps	-98.247 dBrA	-113.625 dBrA	-112.201 dBrA	-116.116 dBrA
Sub 14	234 ps	-98.302 dBrA	-113.757 dBrA	-112.275 dBrA	-116.057 dBrA
Sub 15	193 ps	-97.160 dBrA	-113.375 dBrA	-112.933 dBrA	-116.517 dBrA

AD1955 and ADAU1966 -1 dBFS Test Results with ADAU1952 ASRC0 Added Before DAC

Figure 73 through Figure 84 are the supporting FFT spectrum analysis plots for the direct I^2S, plus the sub node zero, sub node four, sub node eight, sub node twelve, and sub node fifteen A^2B bus configurations. All figures depict the performance with a 1 kHz input sine wave at -1 dBFS.

Figure 73: 1 kHz, -1 dBFS AP I²S Out to AD1955 Only *Figure 74 1 kHz, -1 dBFS AP I²S Out to ADAU1966*

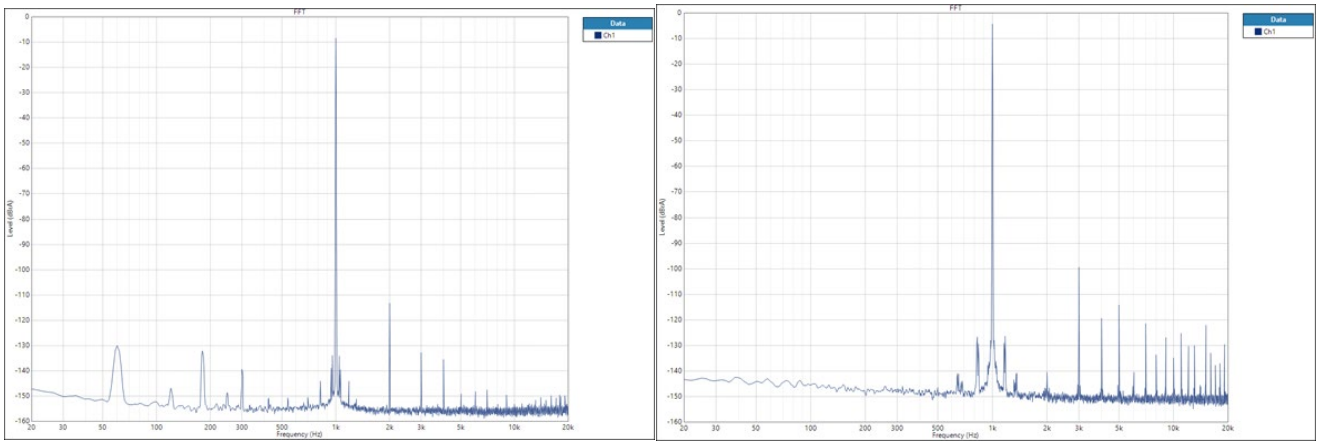


Figure 75: 1 kHz, -1 dBFS S0 to ASRC to AD1955

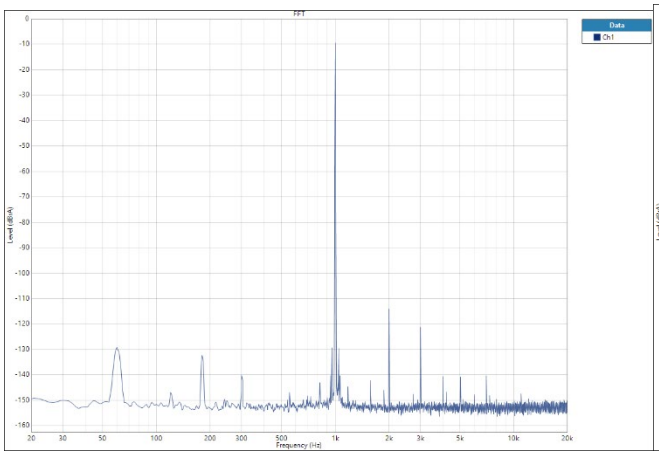


Figure 76: 1 kHz, -1 dBFS S0 to ASRC to ADAU1966

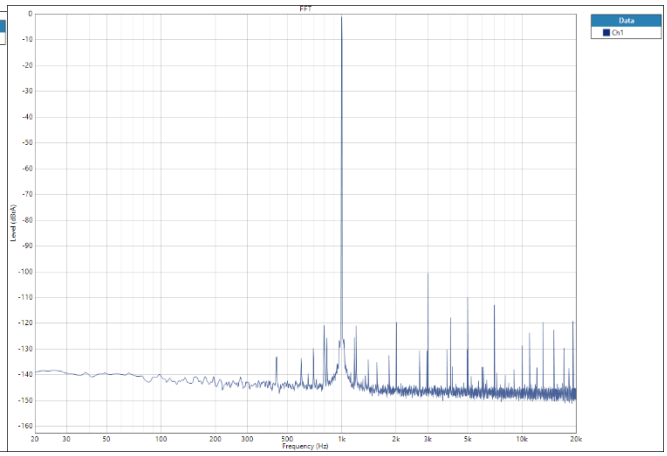


Figure 77: 1 kHz, -1 dBFS S4 to ASRC to AD1955

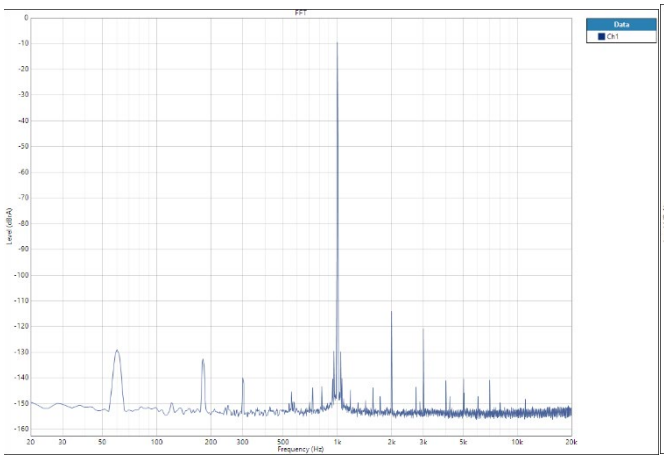


Figure 78: 1 kHz, -1 dBFS S4 to ASRC to ADAU1966

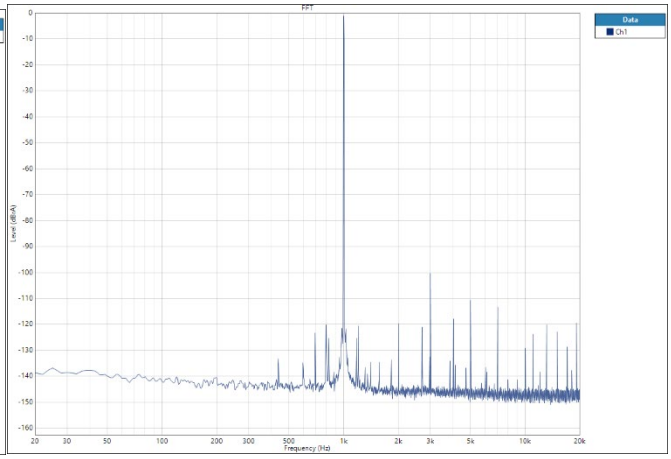


Figure 79: 1 kHz, -1 dBFS S8 to ASRC to AD1955

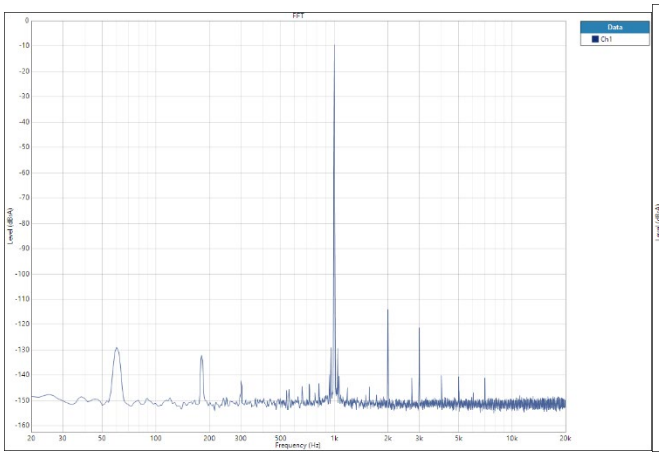


Figure 80: 1 kHz, -1 dBFS S8 to ASRC to ADAU1966

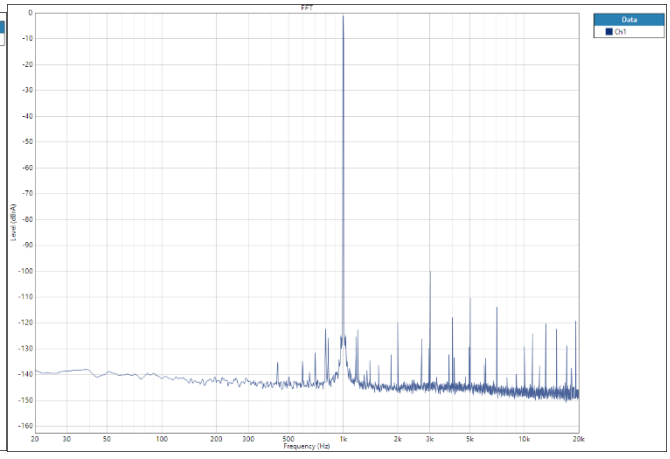


Figure 81: 1 kHz, -1 dBFS S12 to ASRC to AD1955

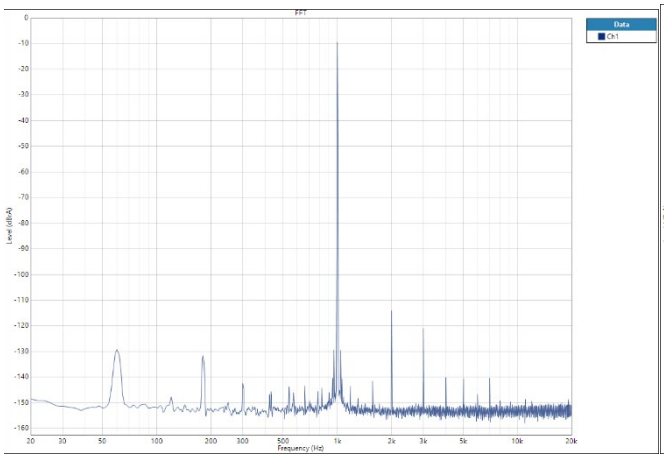


Figure 82: 1 kHz, -1 dBFS S12 to ASRC to ADAU1966

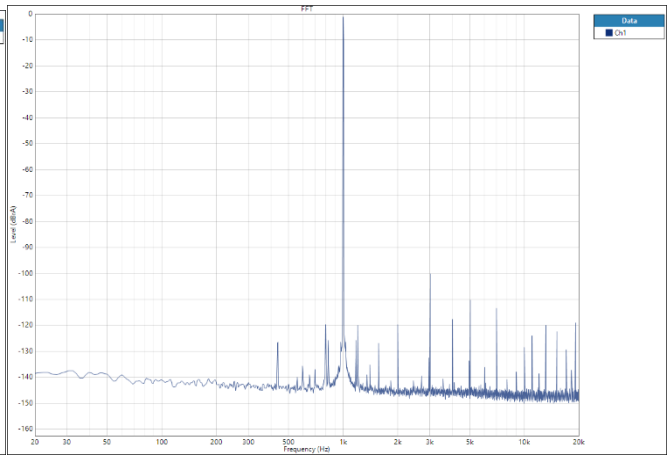


Figure 83: 1 kHz, -1 dBFS S15 to ASRC to AD1955

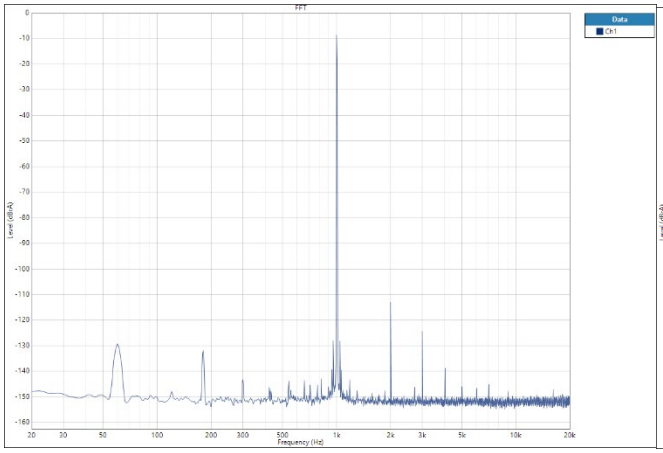


Figure 84: 1 kHz, -1 dBFS S15 to ASRC to ADAU1966

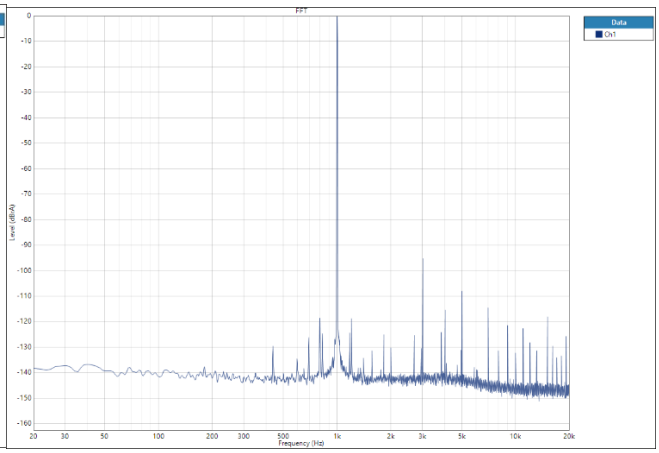


Figure 73 through Figure 84 Observations. The resampling of the audio data to a local I^2S master clock has improved the noise floor significantly for all sub nodes, matching characteristics of the spectrum of the direct I^2S connection of the audio source to the DAC. The effects of removing the jitter from the A^2B bus recovered clocks with the ASRC connected between the sub node and the DAC achieve favorable results.

AD1955 and ADAU1966 -40 dBFS Test Results with ADAU1952 ASRC0 Added Before DAC

Figure 85 through Figure 96 are the supporting FFT spectrum analysis plots for the direct I^2S, plus the sub node zero, sub node four, sub node eight, sub node twelve, and sub node fifteen A^2B bus configurations, with an 11 kHz input sine wave at -1 dBFS:

Figure 85: 11 kHz, -1 dBFS AP I²S out to AD1955 Only

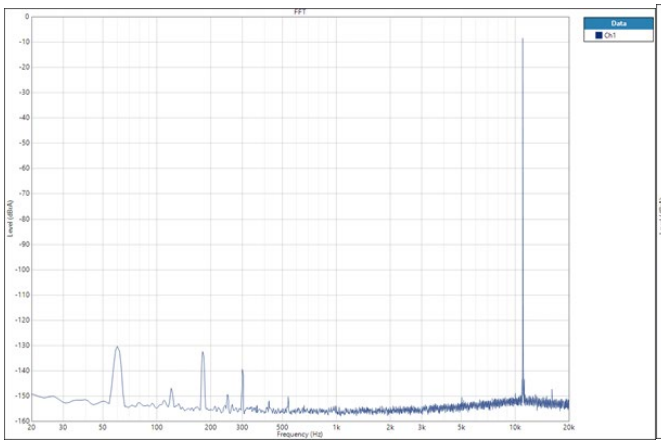


Figure 86: 11 kHz, -1 dBFS AP I²S out to ADAU1966

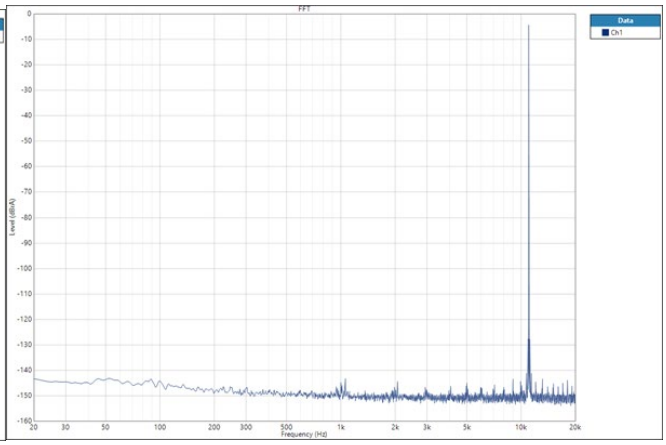


Figure 87: 11 kHz, -1 dBFS S0 I²S to AD1955 Only

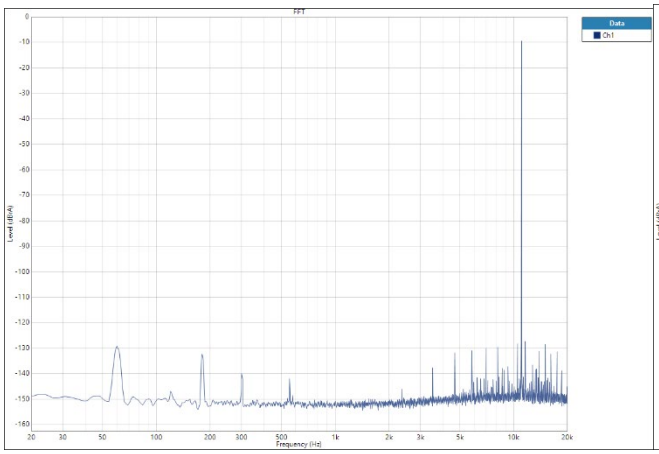


Figure 88: 11 kHz, -1 dBFS S0 I²S to ADAU1966

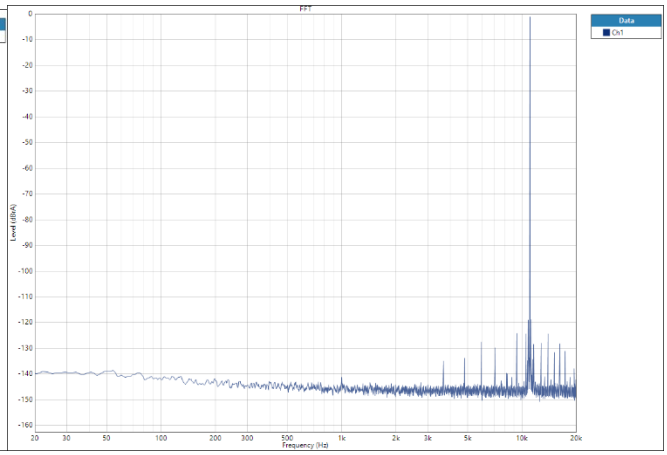


Figure 89: 11 kHz, -1 dBFS S4 I²S to AD1955 Only

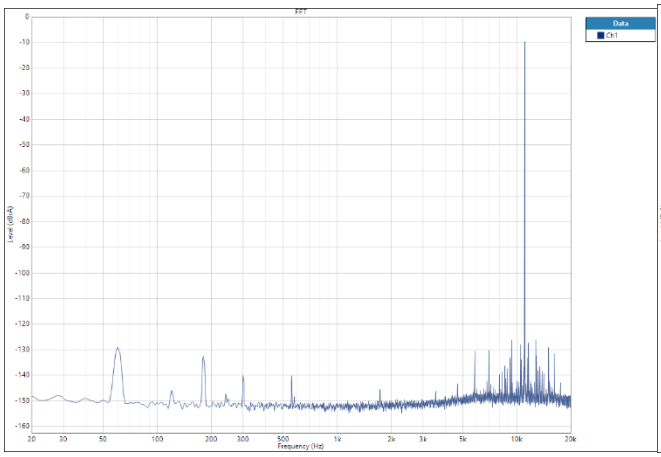


Figure 90: 11 kHz, -1 dBFS S4 I²S to ADAU1966

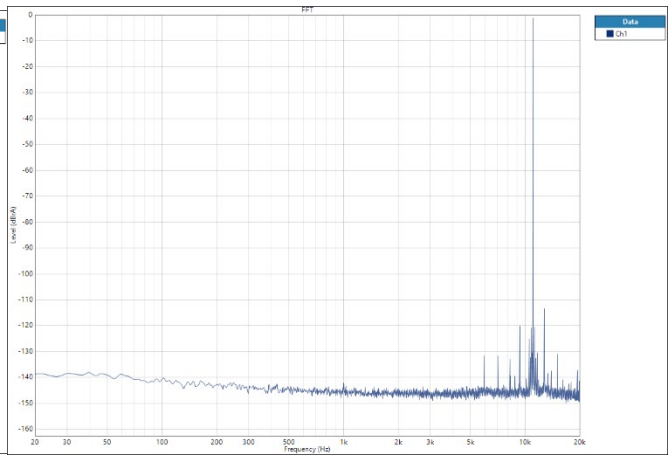


Figure 91: 1 kHz, -1 dBFS S8 I²S to AD1955 Only

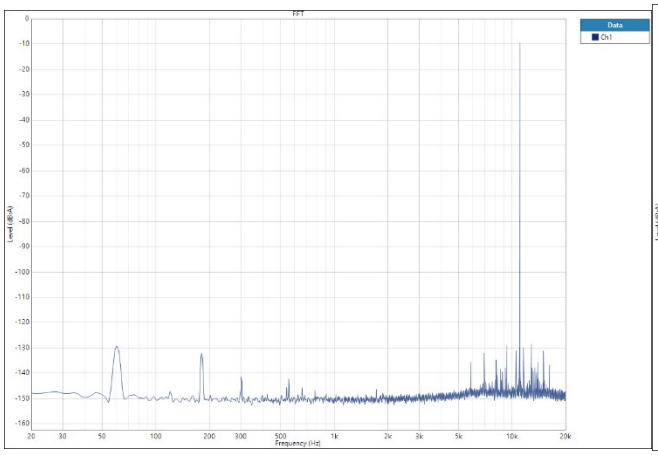


Figure 92: 1 kHz, -1 dBFS S8 I²S to ADAU1966

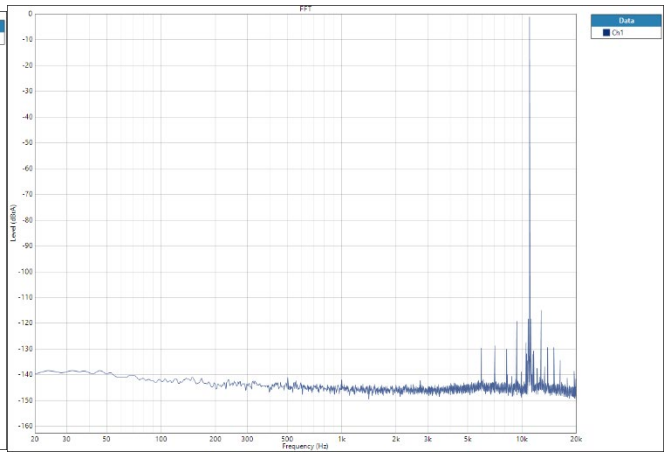


Figure 93: 11 kHz, -1 dBFS S12 I²S to AD1955 Only

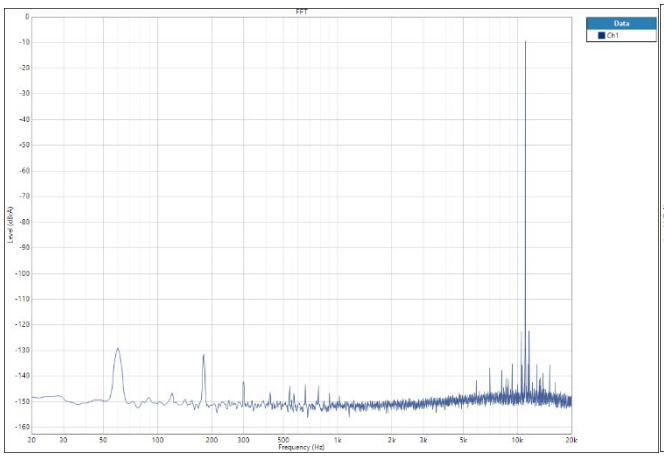


Figure 94: 11 kHz, -1 dBFS S12 I²S to ADAU1966

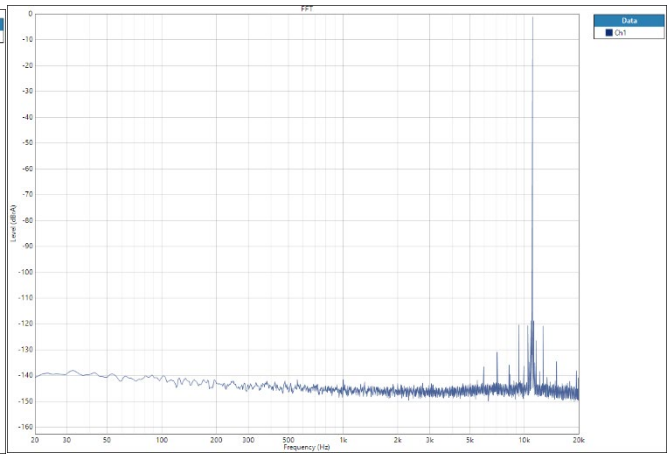


Figure 95: 11 kHz, -1 dBFS S15 I²S to AD1955 Only

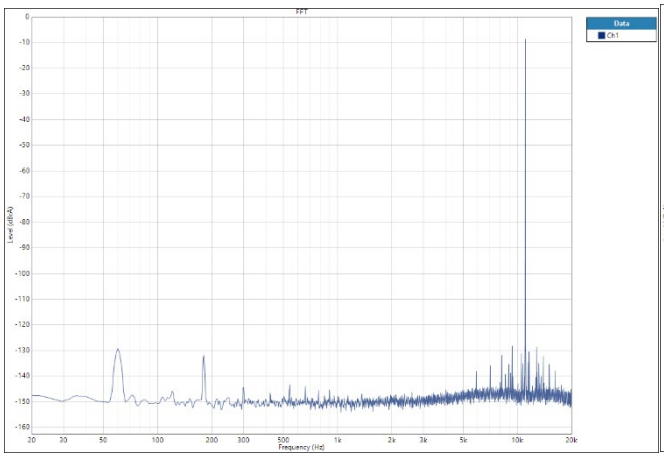


Figure 96: 11 kHz, -1 dBFS S15 I²S to ADAU1966

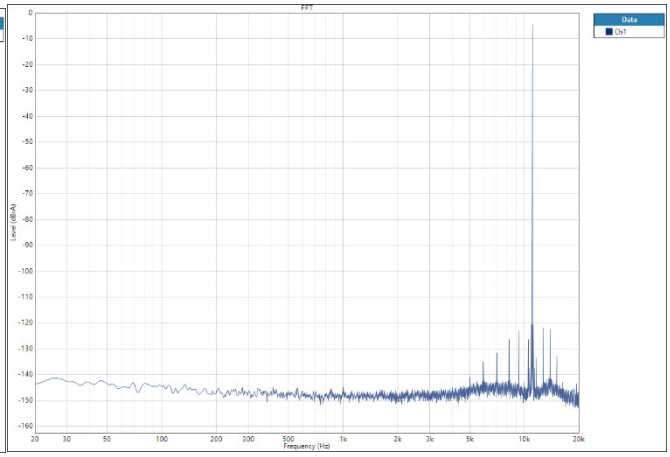


Figure 85 through Figure 96 Observations. The resampling of the audio data to a local I²S master clock has improved the noise floor and THD+N significantly for all sub nodes. Spurious noise centered close to the fundamental harmonic was observed. This noise was caused by the sample rate converter algorithm, but these do not exceed -140 dB (which matches the older AD1890/1 product specifications, so this is expected). These artifacts are unperceived by the listener and are at -120 dB or less levels. For higher frequencies, the effects of removing the jitter from the A²B bus recovered clocks with the ASRC connected between the sub node and the DAC achieve favorable results (an improved THD+N).

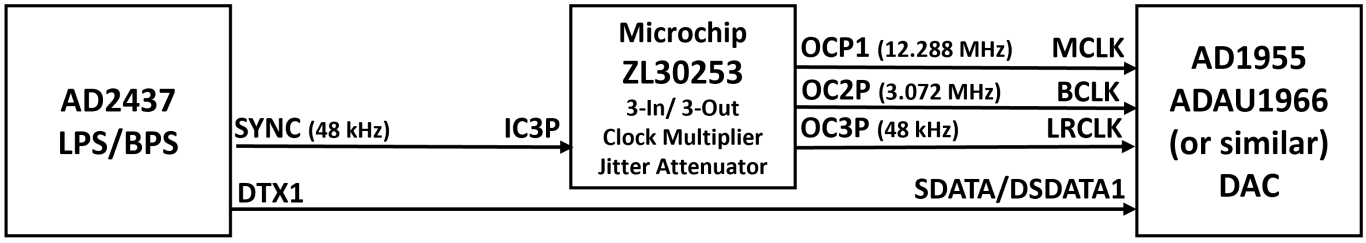
Analog Devices offered a discrete hardware asynchronous sample rate converter solution back in the 1990s with products such as the AD1890 and AD1891. (See *AD1890/AD1891 SamplePort Stereo Asynchronous Sample Rate Converters Datasheet*[14] for more details.) These ASRC hardware blocks have since been integrated in many larger ADI audio processors. For example, the SHARC® processors and SigmaDSP® audio processors integrate multiple hardware ASRCs that allow rate conversion of multiple A²B streams for a given A²B sub node. The ADAU1452 SigmaDSP offers a convenient option to evaluate hardware sample rate conversion that can be used to test jitter reduction and improvements on THN+N performance. The ADAU1452 device is already included in some of the local-powered sub node A²B evaluation kits provided by Analog Devices. The setup and programming of the ADAU1452 can be accomplished using the same SigmaStudio+ software tools as the AD2437.

SOLUTION #2 – Using a Jitter Attenuator with a Low-Jitter Fractional PLL on A²B I²S Clocks

Another option to remove the jitter from the recovered A²B clocks is to use a jitter attenuator (JA) containing a low-jitter, low-bandwidth phase-locked loop. Combined clock multiplier and jitter attenuation devices such as the Microchip ZL30253 (formerly Microsemi, see *ZL30252, ZL30253 3-Input, 3-Output Any-to-Any Clock Multiplier and Jitter Attenuator ICs Datasheet*[6]) are great options to eliminate accumulated-node jitter from an A²B-recovered I²S clock sources. This device can take a maximum of three clock inputs and generate output frequencies for three outputs. There are other options in the ZL3025x family that can also be considered.

The block diagram in Figure 97 shows an example system configuration where the 48 kHz SYNC (I²S left/right clock) feeds into the JA and uses the clock multipliers to generate the necessary I²S output clocks with less than 0.3 picoseconds of RMS jitter. For 24 bit stereo I²S data received from an A²B sub mode, the ZL30253 needs to generate a 12.288 MHz MCLK, a 3.072 MHz BCLK, and a 48 kHz LRCLK that is required to clock an audio DAC, such as an AD1955 or ADAU1966. The output 48 kHz I²S left/right clock can be phase aligned to the 48 kHz SYNC from the AD2437. This also would guarantee phase alignment of the 3.072 MHz BCLK and 12.288 MHz MCLK as they are integer multiples of 48 kHz.

Figure 97. Block Diagram for Connecting the AD2437 to a DAC Using a ZL30253 JA to Remove SYNC Jitter



Another benefit of this family of JAs is a holdover feature where it continues to generate the output clocks when there is a loss of the input clock. This added feature is useful in an A^2B system when there is a system reset or rediscovery of the A^2B bus. The ZL3025x JA can still maintain the I^2S clocks to the DACs and prevent issues like audible clicks or pops on output speakers, and the DAC outputs can be muted until the A^2B bus is rediscovered.

The benefits of the ZL3025x JA device are:

- Offer jitter reduction of the A^2B -recovered I^2S clocks
- Hold over and maintain the input reference clock when the A^2B main node clock is temporarily disabled, removing audible glitches in the system. Contact Microchip for more information regarding other lower-cost variants of this JA/clock multiplier family.

Conclusion

The AD2437 is a novel solution that provides distribution of professional level quality audio at a maximum distance of 300 meters. It is ideal for stage sound installations and distributed audio using standard CAT-5 and XLR cabling. In these commercial A^2B systems, node-to-node jitter is unavoidable. These audio-networked systems accumulate jitter at each subordinate node, but typical amounts of such error are generally lower than those incurred by a DAC or ADC. Because overall system audio performance appears to be dominated by the DAC performance, THD+N measurements can be significantly influenced by the harmonic distortion introduced by the DAC at higher signal levels with the degradation quickly falling off as the amplitude is reduced. Thus, higher levels of clock jitter can begin to have an impact on the performance of the analog audio output of the system. However, the resulting degradation effect on audio performance seen at the downstream A^2B bus nodes can be reduced by selecting a converter with a low-bandwidth PLL to remove the upper frequency components of the jitter on the recovered clock. Jitter Attenuator devices are also another option to remove the jitter from the recovered clocks and prevent signal degradation. Lastly, audio degradation can even be further reduced or eliminated with processors containing HW ASRC blocks, since the resampled audio data is instead driven from clocks derived from a clean local clock oscillator source.

References

[1] *AD2437 A²B Transceiver Datasheet (Revision 0), July 2023. Analog Devices, Inc.* https://www.analog.com/media/en/technical-documentation/data-sheets/ad2437.pdf

[2] *AD2437 A²B Transceiver Technical Reference, Revision 0.2, July 2023. Analog Devices Inc.* https://www.analog.com/media/en/technical-documentation/user-guides/ad2437-trm.pdf

[3] *EVAL-AD2437A1MZ Manual, Revision 2.1, August 2023. Analog Devices Inc.* https://www.analog.com/media/en/technical-documentation/user-guides/eval-ad2437a1mz_manual.pdf

[4] *EVAL-AD2437B1MZ Manual, Revision 2.1, August 2023. Analog Devices Inc.* https://www.analog.com/media/en/technical-documentation/user-guides/eval-ad2437b1mz_manual.pdf

[5] *AD1955 High Performance Multibit Sigma-Delta DAC with SACD Playback Datasheet, Revision 0, 2002. Analog Devices, Inc.* https://www.analog.com/media/en/technical-documentation/data-sheets/AD1955.pdf

[6] *ZL30252, ZL30253 3-Input, 3-Output Any-to-Any Clock Multiplier and Jitter Attenuator ICs Datasheet, January 2018, Microsemi.* https://ww1.microchip.com/downloads/en/DeviceDoc/ZL30252,_ZL30253_data_sheet_012318.pdf

[7] *Evaluating the AD1955 High Performance, Multibit Sigma-Delta DAC with SACD Playback, Evaluation Board User Guide/UG-048, February 2010. Analog Devices, Inc.* https://www.analog.com/media/en/technical-documentation/user-guides/UG-048.pdf

[8] *ADAU1966 16-Channel High Performance Differential Output, 192 kHz, 24-Bit DAC Datasheet, Revision E, March 2016. Analog Devices, Inc.* https://www.analog.com/media/en/technical-documentation/data-sheets/ADAU1966.pdf

[9] *Evaluating the ADAU1962/ADAU1966 High Performance, Low Power, Multibit Sigma-Delta DACs, Evaluation Board User Guide/UG-416. Revision A, January 2014. Analog Devices, Inc.* https://www.analog.com/media/en/technical-documentation/user-guides/UG-416.pdf

Further Reading

[10] *Technote 008-A²B I²S Clock Jitter, Revision 2, July 2020. Clockworks Signal Processing, LLC.* https://clk.works/wp-content/uploads/TechNotes/TN008_A2B_jitter.r2.pdf

[11] *Technote 010-AK4619 ADC and DAC Performance - Evaluation of the Impact of A²B I²S Clock Jitter, Revision 2. May 2023. Clockworks Signal Processing LLC.* https://clk.works/wp-content/uploads/TechNotes/TN010_A2B_ak4619_performance.r2.pdf

[12] *Appnote 001 - Measuring Jitter Spectrum with a DSO, Revision 1.0b, July 2020. Clockworks Signal Processing LLC.* https://clk.works/wp-content/uploads/AppNotes/AP001jitter_measurement.r1b.pdf

[13] *N. Rocchi, A. Toscani, G. Chiorboli, D. Pinardi, M. Binelli, and A. Farina, "Transducer Arrays Over A²B Networks in Industrial and Automotive Applications: Clock Propagation Measurements," in IEEE Access, vol. 9, pp. 118232-118241, 2021, doi: 10.1109/ACCESS.2021.3106710. Unverified link.*

https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=9520394

[14] *AD1890/AD1891 SamplePort Stereo Asynchronous Sample Rate Converters Datasheet, Revision 0, 1993, Analog Devices, Inc.* https://www.analog.com/media/en/technical-documentation/data-sheets/AD1890_1891.pdf

[15] *Robert Adams, Jitter Analysis of Asynchronous Sample-rate Conversion, Presented at 95th AES Convention, Oct 7-10, 1993. (Link to Purchase)* https://www.aes.org/e-lib/browse.cfm?elib=19086

[16] *Adams, Robert & Kwan, Tom, Theory and VLSI Architectures for Asynchronous Sample-Rate Converters, Journal of the Audio Engineering Society. JAES Volume 41 Issue 7/8 pp. 539-555; July 1993. (Link to Purchase)* https://secure.aes.org/forum/pubs/journal/?elib=6993

[17] *Kevin James McLaughlin and Robert Adams, An Asynchronous Sample Rate Converter with 120 dB THD+N Supporting Sample Rates up to 192 kHz. Analog Devices, Wilmington, MA, USA. Presented at the 109th AES Convention, September 2000. (Link to Purchase)* https://www.aes.org/e-lib/browse.cfm?elib=9147

[18] *Maury Wood, Analysis of Jitter Rejection of SRCs and DACs Using an NCO, Analog Devices Inc., Wilmington, USA, Presented at the 100th AES Convention, May 1996. (Link to Purchase)* https://www.aes.org/e-lib/browse.cfm?elib=7515

[19] *Boris Lerner and Aaron Lowenberger, EE-261: Understanding Jitter Requirements of PLL-Based Processors, Revision 1, January 2005, Analog Devices, Inc.* https://www.analog.com/media/en/technical-documentation/application-notes/EE-261.pdf

[20] *Chris Travis, Paul Lesso, Specifying the Jitter Performance of Audio Components, Presented at the 117th Convention, October 2004, USA Audio Engineering Society.* https://www.aes.org/tmpFiles/elib/20231107/12950.pdf

[21] *Dunn, Julian, Jitter and Digital Audio Performance Measurements. UK 9th Conference: Managing the Bit Budget, May 1994, Audio Engineering Society,* https://www.aes.org/e-lib/browse.cfm?elib=6111

[22] *Julian Dunn, Jitter Theory-Technote 23. Audio Precision, Inc. AudioPhilleo, LLC. Knowledge Base.* http://www.audiophilleo.com/zh_hk/docs/Dunn-AP-tn23.pdf

[23] *James A. S. Angus, A New Method for Analyzing the Effects of Jitter in Digital, Audio Systems, 103rd AES Convention, May 1998, Audio Engineering Society.* https://www.aes.org/e-lib/browse.cfm?elib=8464

[24] *Eric Benjamin and Benjamin Gannon, Theoretical and Audible Effects of Jitter on Digital Audio, Quality, Dolby Laboratories Inc. San Francisco, CA 94103, USA, Presented at the 105th AES Convention, September 1998, Audio Engineering Society.* https://www.aes.org/e-lib/browse.cfm?elib=8354

[25] *Bruno Putzeys and Renaud de Saint Moulin. Effects of Jitter on AD/DA Conversion. Specification of Clock Jitter Performance. Presented at the 116th Convention, May 2004, Audio Engineering Society. (Link to Purchase)* https://secure.aes.org/forum/pubs/conventions/?elib=12637

[26] *EVAL-ADAU1452 Obsolete Evaluation Board, Analog Devices, Inc.*
https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/eval-adau1452.html

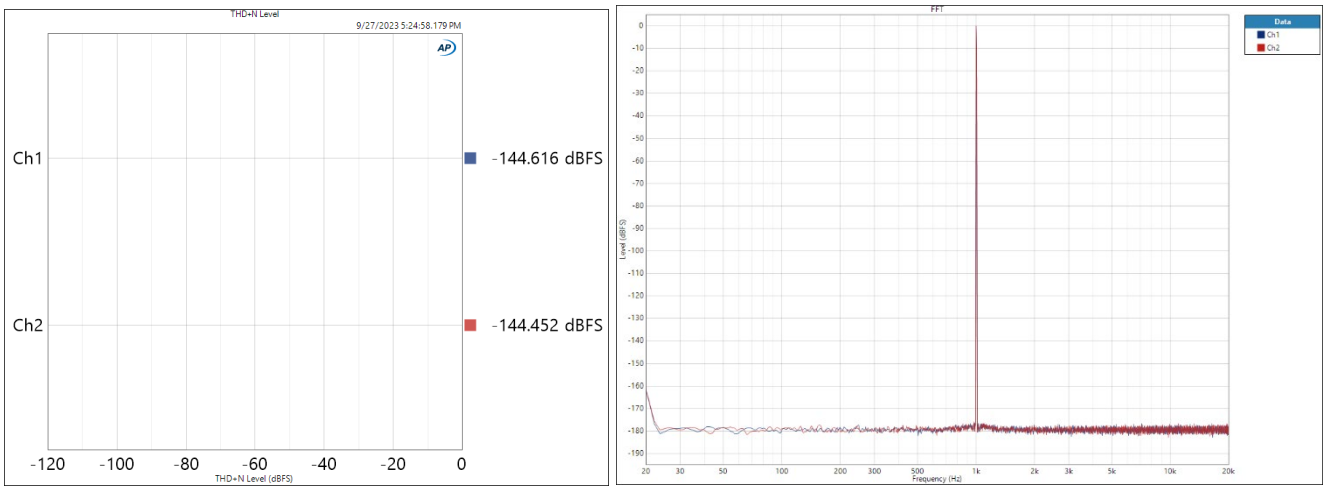
Document History

Revision	Description
Revision 1 – September 26, 2024 *by John Tomarakos*	Initial Release

Appendix A - Additional AD2437 SPDIF-to-Analog and Digital I²S Audio Loopback Tests Using the AD2437 A1MZ and B1MZ Evaluation Kits

The AD2437 EVAL-AD1937A1MZ main board evaluation kit provides an onboard SPDIF transmitter and receiver through the ADAU1452 SigmaDSP. This interface is a convenient way to inject test tones into an A²B network for testing audio signal integrity and streams functionality. The SPDIF interfaces are often used for testing on Audio Precision test equipment. For example, it might be desirable to set up a quick test stream to test a digital loopback of A²B data on a given sub node in the A²B network, and then resend the signal back to the main node. Figure 98 shows the results of the THD+N testing are shown for APx555 SPDIF loopback, AD2437 SPDIF A1MZ loopback, and SPDIF loopback through a B1MZ sub node (using a digital I²S or analog loopback with the ADAU170). Before performing a SPDIF loopback using asynchronous sample rate conversion through an A²B network, first measure a baseline SPDIF (Figure 98) loopback using the APx555.

Figure 98. APx555 Baseline SPDIF THD+N Test Results (THD+N = -144.5 dBFS)

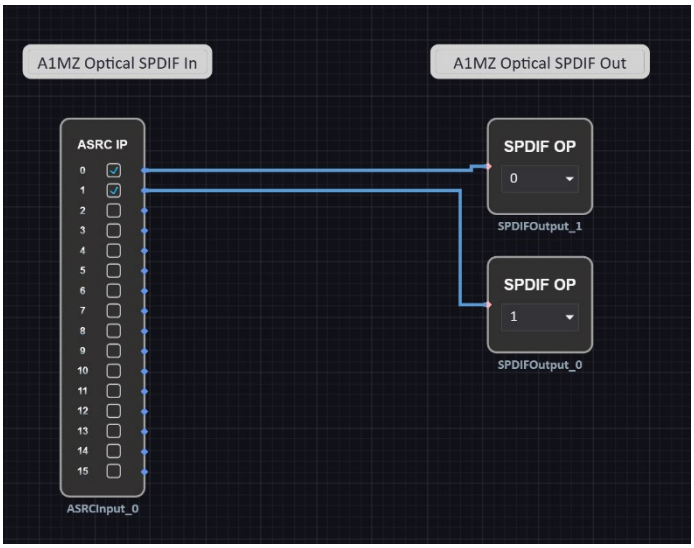


The input test signal from the APx555 SPDIF transmitter was a 1 kHz tone at 0 dBFS, resulting in a THD+N of -132.5 dBFS.

Second, a SPDIF loopback was performed on the EVAL-AD2437A1MZ Main Node only through the hardware ASRC block on the ADAU1452 (Figure 99). In this case no audio data is transmitted on the A²B node. The primary objective here is to test and evaluate the performance of the asynchronous sample rate conversion block on the ADAU1452. Also, test the audio data received on the integrated SPDIF receiver and to determine its effects on the audio quality of the incoming signal.

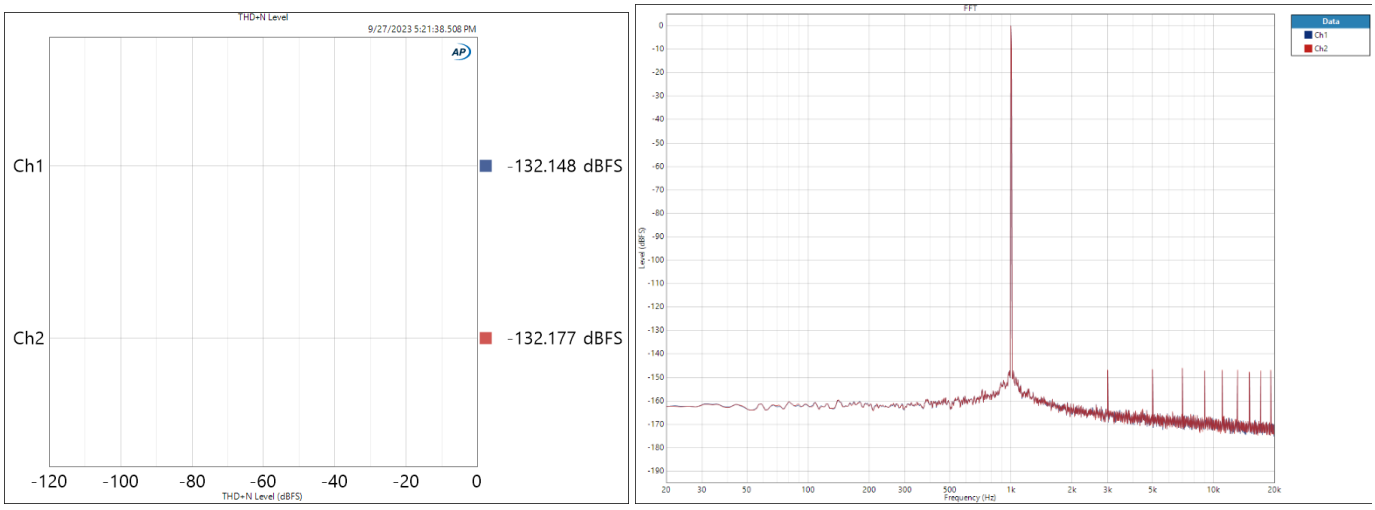
The input test signal again from the APx555 SPDIF transmitter was a 1 kHz tone at 0 dBFS, resulting in THD+N of -132.5 dBFS. Figure 100 shows the noise floor raised with some higher harmonics introduced, however, still less than the -120 dB noise floor.

Figure 99. EVAL-AD2437A1MZ SPDIF Loopback Test Through ASRC0



The input test signal again from the APx555 SPDIF transmitter was a 1 kHz tone at 0 dBFS, resulting in THD+N of -132.5 dBFS. Figure 100 shows the noise floor raised with some higher harmonics introduced, however, still less than the -120 dB noise floor.

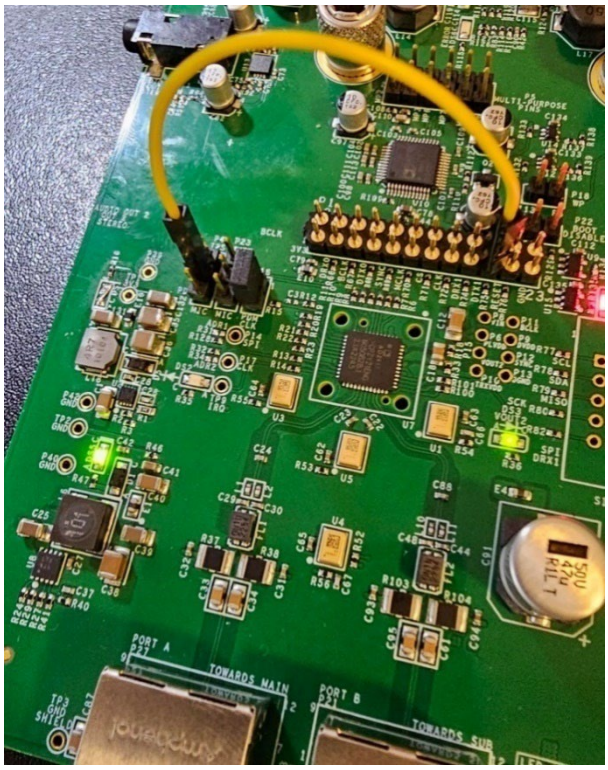
Figure 100. AD2437 Main Node (only) SPDIF Loopback Test Results (THD+N = -132.5 dB)



Third, a measurement to test the integrity of the I^{2}S connection on a far-end EVAL-AD1937B1MZ was performed. The sub node AD2437 I^{2}S output data is looped back to its I^{2}S input pin and streamed back to the main node, where it is sent to the ADAU1452 SPDIF transmitter output back to the APx555. Once again, the tone that is injected into the SPDIF receiver of the ADAU1452 requires use of a HW ASRC to align and synchronize the SPDIF data with the I^{2}S master clock source for the main node AD2437.

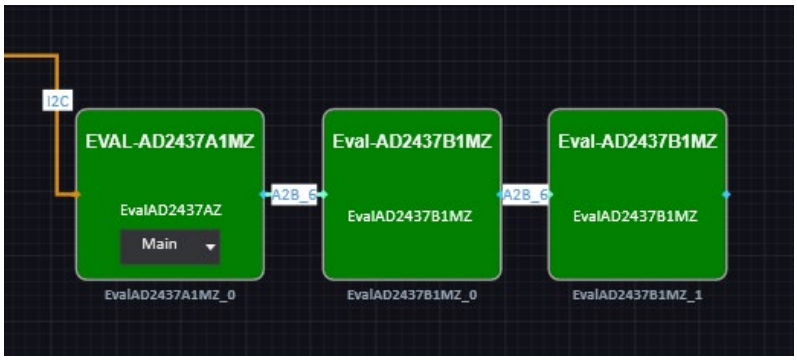
To permit a direct digital I²S transmission on the sub node I²S pins, isolate the I²S DRX0/SIO0 pin from the ADAU1701 on the B1MZ board. This can be done by removing jumper P4 and directly connect pin 3 (DRX0) to either DTX0 (pin 8) or DTX1 (pin 19) on the P1 header with a small jumper wire (Figure 101).

Figure 101. Connection of P4 pin 2 (DRX1) to P1 Header Pin 19 (DTX1) that Disconnects the ADAU1701



In this example the I²S audio is externally on the second sub node. The SigmaStudio+ schematic in Figure 102 shows the system configuration, where there is a stream from the main node to sub node 1 and a second stream from sub node 1 back to the main board. In this test, the main board programs the ADAU1452 during discovery to enable the incoming and outgoing streams using the SPDIF TX/RX for the APx555.

Figure 102. Three Node I2S Loopback Test – SigmaStudio + 2.0 Schematic



The result of the I^{2}S loopback through sub node 1 back to the main SPDIF output shows an identical frequency spectrum plot and THD+N result (Figure 103) as the SPDIF RX-to-ASRC0-to-SPDIF TX loopback test. Last, a verification of the ADAU1701 ADCs performance can be done on the B1MZ sub nodes by connecting the 1/8th inch analog cable from the line to the line outputs. The result of the THD+N measurement was -83 dBFS, which matches exactly the ADU1701 datasheet specification (Figure 104).

Figure 103. AD2437 Sub Node 1 to Main SPDIF Loopback Test Results (THD+N = -132.5 dB)

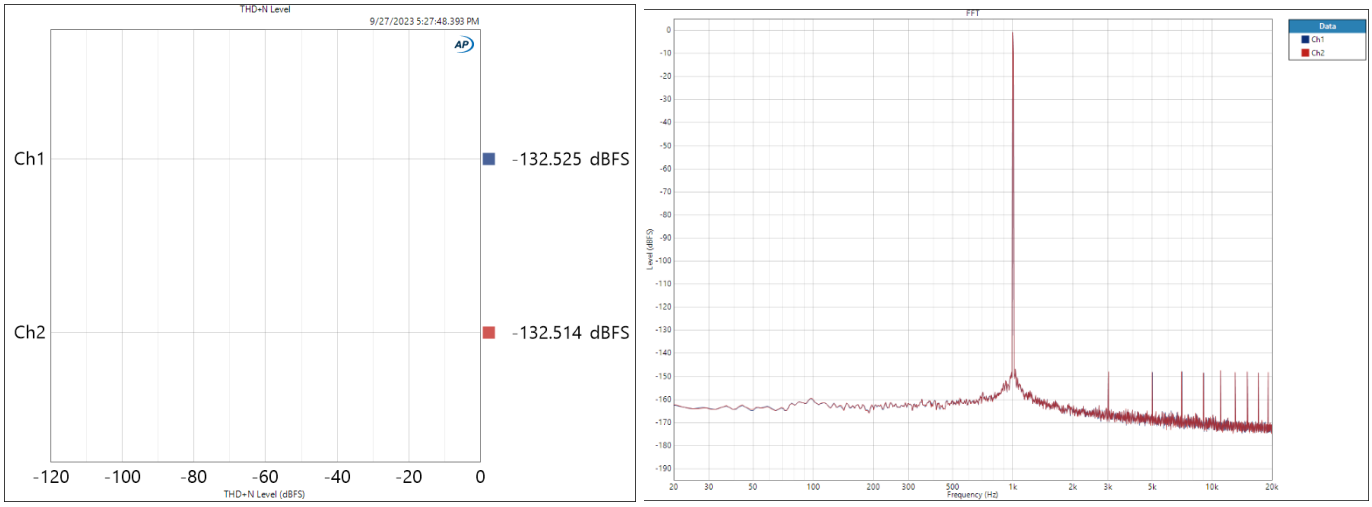
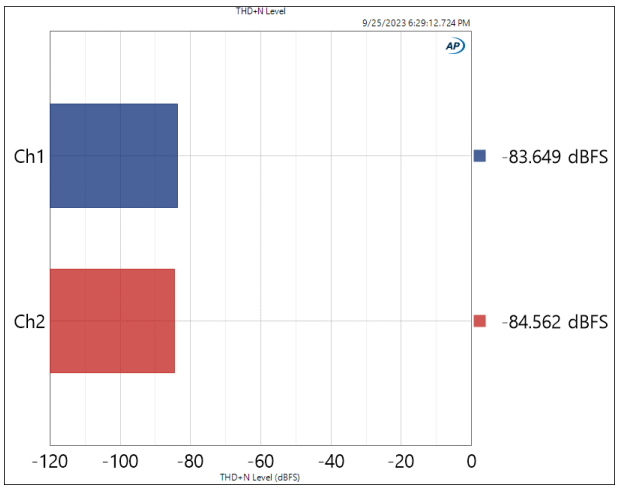
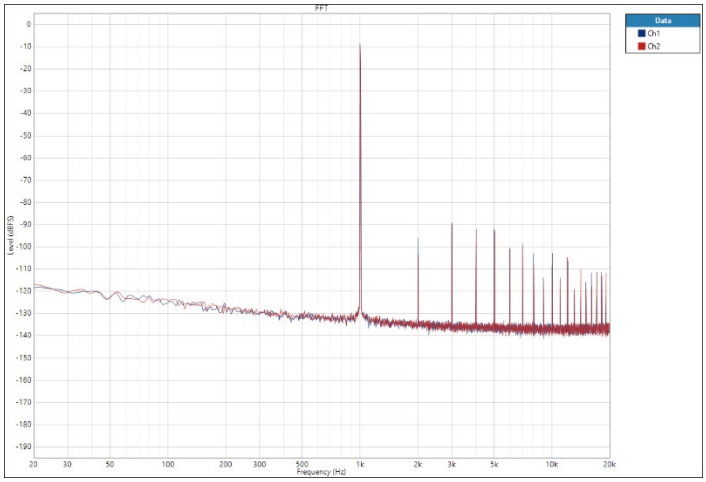


Figure 104. B1MZ Loopback through ADAU1701 ADCs (Line In) and DACs (Line Out). THD+N Result = -83 dB





ANALOG DEVICES

SigmaDSP 28-/56-Bit Audio Processor with Two ADCs and Four DACs

Data Sheet **ADAU1701**

FEATURES

28-/56-bit, 50 MIPS digital audio processor
2 ADCs: SNR of 100 dB, THD + N of −83 dB
4 DACs: SNR of 104 dB, THD + N of −90 dB

GENERAL DESCRIPTION

The ADAU1701 is a complete single-chip audio system with a 28-/56-bit audio DSP, ADCs, DACs, and microcontroller-like control interfaces. Signal processing includes equalization, cross-