AN-1436
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

# Solving IEC System Protection for Analog Inputs Using the ADG5412F

by David Forde, David Aherne, and Jeffrey Ryan

## INTRODUCTION

Electronic systems that operate in harsh electromagnetic environments require that the input and output ports be protected to specific standard levels to safeguard devices against electrostatic discharge (ESD), electrical fast transients (EFT/burst), and surge events.

This application note describes how the Analog Devices, Inc., next generation, fault protected family of switches with integrated overvoltage protection (OVP), combined with minimal external components, expedites the process of designing a protection architecture for the IEC 61000-4 standards for ESD, EFTs, and surge events. This application note provides an overview of overvoltage fault protection as well as the circuits used to achieve standard IEC levels of robustness.

The transient voltage suppressor (TVS) design window concept described in this application note provides greater flexibility to the system designer in terms of component choice, and drives higher precision with less system complexity.

This application note addresses how this IEC level protection solution reduces the downstream protection requirements to the equivalent of a 1 kV human body model (HBM) ESD level.

## ELECTROMAGNETIC COMPATIBILITY

The IEC 61000 specifications define the set of electromagnetic compatibility (EMC) immunity requirements that apply to electrical and electronic equipment used in residential, commercial, and light industrial environments. Within this set of specifications, there are three key high voltage transient specifications:

- IEC 61000-4-2 ESD
- IEC 61000-4-4 EFT
- IEC 61000-4-5 surge immunity

Each of these specifications defines a test method to assess the immunity of electronic and electrical equipment against the defined phenomenon.

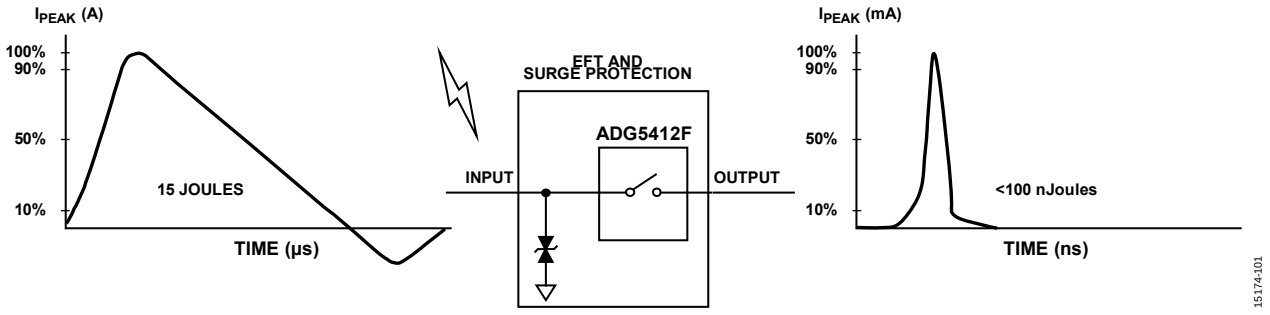


*Figure 1. Complete Protection Solution*

# TABLE OF CONTENTS



## REVISION HISTORY

**7/2017—Revision 0: Initial Version**

# OVERVOLTAGE FAULT PROTECTION

Analog Devices portfolio of robust, fault protected switches and multiplexers (ADG5208F and ADG5412F) provides OVP up to ±55 V. The devices also have power off protection up to ±55 V, overvoltage fault detection, guaranteed latch-up immunity, and high HBM ESD ratings of up to 5.5 kV. As well as achieving industry leading robustness, the overvoltage protected switches maintain industry leading analog performance for both high impedance and low impedance systems.

Loss of power, hot swap connections, power supply sequencing issues, and miswiring are all common causes of persistent dc or transient overvoltages. Placing an overvoltage protected switch at the input or output node on a system protects the system input and output from overvoltages up to ±55 V in both powered and unpowered conditions. The switch isolates the fault and disconnects the input from the rest of the circuit. The switch also has the advantage of protecting downstream circuitry because the fault is not propagated into the system via clamping diodes.

Traditional complementary metal-oxide semiconductor (CMOS) architectures for devices such as switches, amplifiers, analog-to-digital converters (ADCs), and digital-to-analog converters (DACs) include ESD protection diodes on both the input and the output nodes of the device. Figure 2 shows the functional block diagram of an Analog Devices OVP switch. The traditional input protection ESD diodes are replaced with a bidirectional ESD protection cell at the input node (Sx) to the switch, which has a trigger voltage of approximately 70 V. Therefore, during an overvoltage event, the voltage level on the input node of the switch is no longer clamped to the supply rails, and the input to the switch can withstand voltages up to ±55 V. The bidirectional ESD protection cell provides excellent ESD protection up to 5.5 kV HBM.

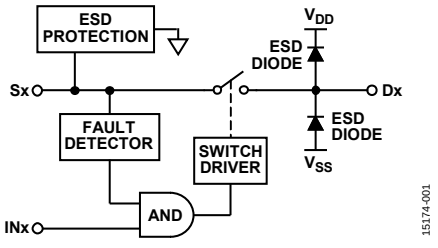


*Figure 2. Functional Block Diagram of an OVP Switch*

The internal fault detector circuitry of the switch constantly monitors the voltage level on the input and compares it to the fault reference level (usually $V_{DD}$ and $V_{SS}$). When the input detects an overvoltage condition, the affected channel turns off after approximately ~500 ns and the input goes high impedance, fully isolating the fault from any sensitive downstream circuitry. During the 500 ns duration it takes the switch to react, the up and down diodes on the output node of the switch clamp the output voltage, again protecting the downstream circuitry. Figure 3 shows this output voltage protection over time.

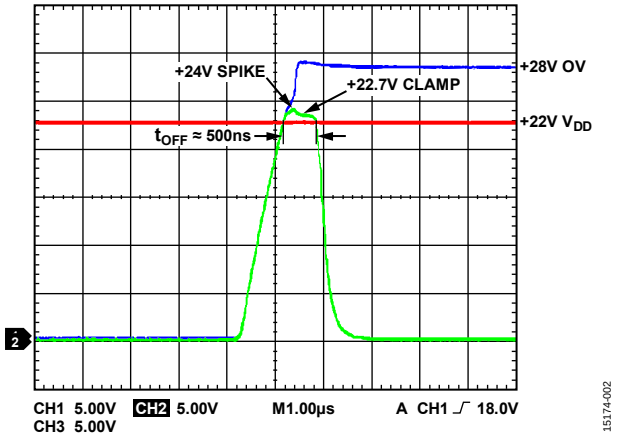


*Figure 3. Output Voltage Over Time*

The robustness features of the switch are as follows:

- ±55 V ac and persistent dc OVP
- Power off protection up to ±55 V
- Overvoltage fault detection
- Immunity from latch-up under any circumstances
- 5.5 kV HBM ESD rating

## SYSTEM LEVEL PROTECTION CIRCUIT

At the system level, OVP, latch-up prevention, and EMC protection (ESD, EFT, and surge) are typically catered to by a host of discrete devices, all of which can contribute to a degradation in system level performance and accuracy due to leakage and extra resistance in the signal path.

Using the robustness of Analog Devices overvoltage fault protection devices, combined with a single transient voltage suppressor (TVS) and a low value resistor (≤30 Ω), the ADG5412F can withstand high voltage transients of up to 16 kV IEC ESD (air discharge), 8 kV IEC ESD (contact discharge), 4 kV EFT, and 4 kV surge. Figure 4 shows the protection circuit.

Under normal operating conditions, the TVS device has a high impedance to ground. When a transient voltage larger than the breakdown voltage of the TVS is applied to the input of the system, the voltage at the input is clamped as the TVS breaks down and provides a low impedance path to ground, diverting the transient current away from the switch input to ground. Important parameters of the TVS device include working peak reverse voltage, which is the voltage below which no significant conduction occurs; breakdown voltage, which is the voltage at which some specified conduction occurs; and maximum clamping voltage, which is the maximum voltage across the device when conducting the maximum current specified.

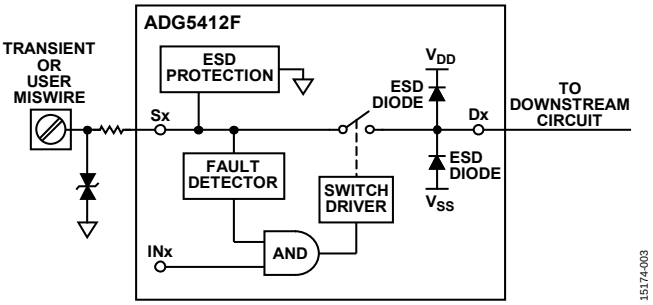


*Figure 4. Protection Circuit Diagram*

This circuit was tested to the IEC61000-4-2, IEC61000-4-4, and IEC61000-4-5 standards and the ADG5412F device was found to withstand very high levels of IEC ESD, EFT, and surge.

Table 1 shows the results achieved by the ADG5412F with various combinations of TVS devices and resistors.

**Table 1. Test Results for Various Combinations of TVS Devices and Resistors.**

| Protection | IEC ESD Contact (kV) | IEC ESD Air (kV) | EFT (kV) | Surge (kV) |
|---|---|---|---|---|
| 33 V TVS and 0 Ω Resistor | 5 | Not tested | 3 | 4 |
| 33 V TVS and 10 Ω Resistor | 8 | 16 | 4 | 4 |
| 45 V TVS and 0 Ω Resistor | 4 | Not tested | 2 | 4 |
| 45 V TVS and 15 Ω Resistor | 8 | 16 | 4 | 4 |
| 54 V TVS and 30 Ω Resistor | 8 | 16 | 4 | 4 |

The transient for an ESD and EFT event has a very fast rise time, after an initial overshoot the transient is clamped by the TVS device. The overshoot is caused by the TVS not reacting fast enough to the very fast rise time of the ESD/EFT pulse; therefore, a small value resistor is required to increase the ESD/EFT levels, as shown in Table 1.

## TVS SELECTION

When selecting a TVS device, it is important to ensure that the maximum working voltage is greater than both the normal operating range of the pins to be protected and any known system overvoltage that may be present due to miswiring. Combining the TVS maximum working voltage with the integrated ±55 V OVP of the ADG5412F provides a wide design window for TVS selection.

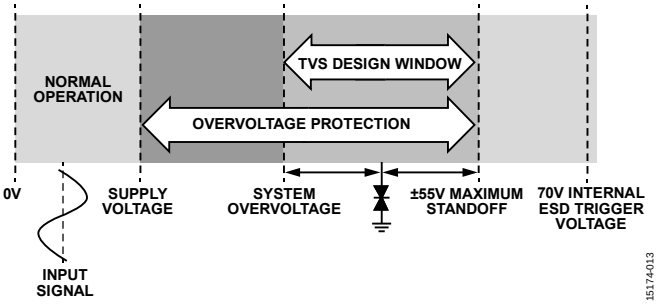


*Figure 5. TVS Design Window*

Figure 5 shows the regions of operation for a system input that interfaces with the outside world. The leftmost region represents normal operation, where the input voltage is between the supply voltage ranges. The second region from the left represents the range of possible persistent dc or long duration ac overvoltages presented to the input due to loss of power, miswiring, or short circuits. Also included in the diagram, on the far right hand side, is the trigger voltage for the internal ESD protection diodes of the ADG5412F.

The TVS design window region is created by the ±55 V OVP of the switch. The window is defined by the difference between the maximum standoff voltage of the OVP switch and the maximum overvoltage possible in the system. To protect the system input and sensitive downstream circuitry against the IEC standard and to stay within the operational range of the OVP switch, select a TVS with a breakdown voltage inside the TVS design window region. This design window concept provides the system designer with the flexibility to choose a TVS breakdown voltage anywhere within this wide voltage range.

Another TVS parameter to consider when selecting a device is the maximum clamping voltage of the TVS. During a surge event, as an increasing current is flowing through the TVS device, the clamping voltage of the TVS can increase up to its maximum clamping voltage. This maximum clamping voltage for a TVS is higher than the breakdown voltage. With a high breakdown voltage TVS, for example, 54 V, the maximum clamping voltage is above the ±55 V dc absolute maximum ratings specified in the data sheet for the ADG5412F source pin. However, the Surge Testing, IEC61000-4-5 section proves that the ADG5412F can withstand voltages greater than the dc maximum rating for the duration of the surge transient; this is because the surge transient has a much slower rise time than an ESD pulse and, therefore, the internal ESD protection on the ADG5412F does not trigger for the duration of the surge transient.

## SYSTEM LEVEL PROTECTION

In the circuit shown in Figure 4, the discrete TVS and resistor devices provide protection for the ADG5412F from IEC ESD, EFT, and surge events. The ADG5412F provides protection from overvoltage faults, latch-up, and hot swap events. To fully protect a system input from ESD, EFT, and surge events, it is important to not only make sure the OVP component (the ADG5412F) survives the transient voltages, but to also ensure that the energy levels exiting the switch at the drain side of the ADG5412F (Dx) are suppressed sufficiently so that any downstream devices are not damaged.

Figure 6 shows the setup used to quantify the energy levels from the output of the ADG5412F during an IEC ESD, EFT, and surge event.

The test setup replicates a typical system where the ADG5412F protects the input of a downstream component. The up and down diodes represent the input ESD protection diodes that exist in any downstream circuitry, for example, an amplifier or an ADC. During a transient event, the ADG5412F is effective in reducing the energy that reaches the downstream device; this is shown by the data in the next sections. The input ESD protection diodes of the downstream devices remove the minor residual energy at the output of the protection circuit, just as they normally do during a HBM ESD event.

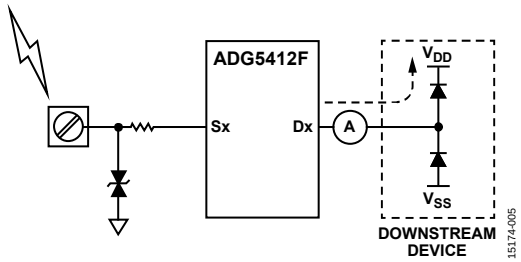


*Figure 6. Test Setup*

# ELECTROSTATIC DISCHARGE (ESD)

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused by near contact or induced by an electric field. ESD has the characteristics of high current flow for a short time period.

The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. IEC 61000-4-2 specifies testing using two coupling methods: contact discharge and air gap discharge. Contact discharge indicates that the discharge gun is placed in direct connection with the unit. Air gap discharge uses a higher test voltage, but does not make direct contact with the unit under test.

During air discharge testing, the charged electrode of the discharge gun moves toward the unit under test until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the unit. A number of factors affect the results and repeatability of the air discharge test, including humidity, temperature, barometric pressure, distance, and rate of approach to the unit. The air discharge method is a better representation of an actual ESD event than the contact discharge method, but it is not as repeatable.

Figure 7 shows the 8 kV contact discharge current waveform as described in the specification. Some of the key waveform parameters to note are fast rise times of less than 1 ns, a short pulse width of approximately 60 ns, and a peak current of 30 A.

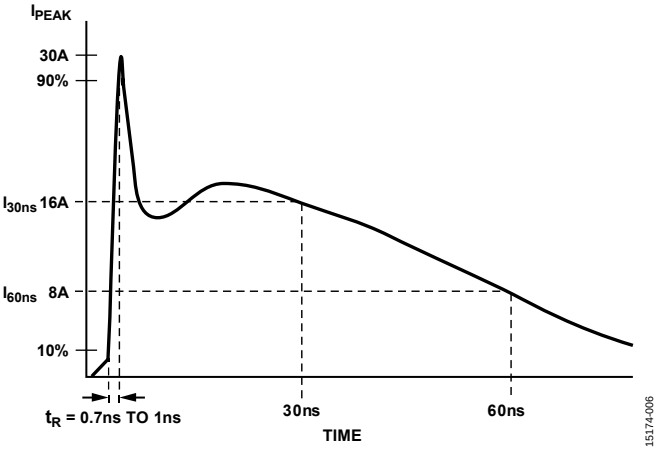


*Figure 7. IEC 61000-4-2 ESD Waveform (8 kV)*

The test is performed with single discharges. The test point is subjected to at least 10 positive and 10 negative discharges. A 1 sec interval between discharges is recommended.

When the ESD pulse is applied to the input of the protection circuit, after an initial overshoot, the voltage at the input is clamped at 54 V by the TVS device (SMAJ54CA). Because the pulse duration is very short, approximately 60 ns, the OVP circuitry within the ADG5412F does not have time to react and isolate the downstream circuitry from the ESD event. However, the internal protection diodes on the output of the ADG5412F become forward biased and clamp the output voltage of the ADG5412F at $V_{DD}$ + 0.7 V.

These internal diodes on the output are robust enough to take the majority of the current away from the downstream devices, thus protecting the system from the initial 8 kV ESD event.

## ELECTROSTATIC DISCHARGE TESTING IEC61000-4-2

Figure 8 shows the current paths through the circuit during an IEC transient event. The majority of the current is shunted to ground through the TVS device (Path $I_1$). Path $I_2$ shows the current that is dissipated during the 500 ns it takes for the switch to turn off. Finally, the current in the Path $I_3$ is the level that the downstream components must withstand.

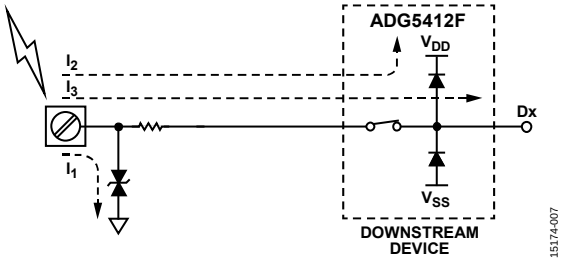


*Figure 8. Current Paths During an ESD Event*

Figure 9 shows the current measured at the output of the switch, with an ±8 kV IEC ESD contact discharge pulse applied to the input of an ADG5412F with a 54 V TVS (Bourns SMAJ54CA) and a 30 Ω series resistor. Before the TVS clamps the transient voltage there is an initial overshoot (see the TVS Selection section) to avoid triggering the internal ESD protection of the ADG5412F (the 30 Ω resistor is required).The peak current measured at the output (Dx) of the ADG5412F during the IEC ESD event is just 678 mA.

The peak current measured at the output can be correlated to a short duration pulse of approximately 60 ns with peak currents used to classify HBM ESD events. An HBM ESD strike of 1 kV has a peak current of approximately 660 mA and a duration of 500 ns. Therefore, using the ADG5412F in the configuration described in Figure 4 an 8 kV IEC ESD strike is attenuated to less than the equivalent of a 1 kV HBM ESD event. This can be compared to HBM ESD ratings data for the downstream components.

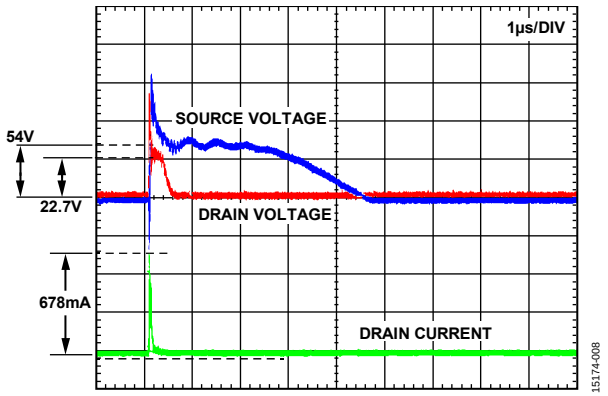


*Figure 9. Drain Voltage and Output Current at the Drain (Dx) During an 8 kV Event*

Similarly, Figure 10 shows the current measured at the output of the switch, with an ±16 kV IEC ESD air discharge pulse applied to the input of an ADG5412F with a 54 V TVS (Bourns SMAJ54CA) and a 30 Ω series resistor.

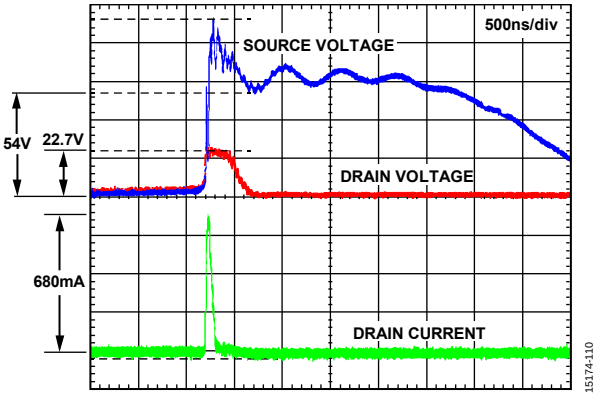


*Figure 10. Drain Voltage and Output Current at the Drain (Dx) During a 16 kV Air Discharge Event*

The peak current measured at the output of the ADG5412F during the IEC ESD event is just 680 mA, which is almost identical to the results achieved for the 8 kV contact discharge test.

# ELECTRICAL FAST TRANSIENTS (EFTs)

EFT testing involves coupling a number of extremely fast transient impulses onto the signal lines to represent transient disturbances associated with external switching circuits that are capacitively coupled onto the signal lines. This testing reflects switch contact bounce or transients originating from the switching of inductive or capacitive loads, all of which are common in industrial environments. The EFT test defined in IEC 61000-4-4 attempts to simulate the interference resulting from these types of events.

Figure 11 shows the EFT waveform. The output waveform consists of repetitive bursts of 5 kHz high voltage transients. The bursts are spaced 300 ms apart, and each burst has a duration of 15 ms. Each individual pulse has a rise time ($t_R$) of 5 ns and a pulse duration ($t_D$) of 50 ns, measured between the 50% point on the rising and falling edges of the waveform. Similar to the ESD transient, an individual EFT pulse has the characteristics of fast rise time and short pulse width. The total energy in one single pulse is similar to that of an ESD pulse.

IEC 61000-4-4 specifies that these fast burst transients are coupled onto the input lines using a capacitive clamp. The EFT is capacitively coupled onto the input lines by the clamp rather than direct contact. To replicate this coupling plate at the system level test, a 0.5 µF coupling capacitor is connected to the input of the IC. This follows the IEC 62215 standard, which describes the IC level version of the IEC61000-4-4 standard.

When these EFT pulses are applied to the input of the protection circuit, the current is suppressed in a similar way to the ESD event. After the initial overshoot, the 4 kV EFT voltage is clamped by the 54 V TVS device and the majority of the residual current that is not directed through the TVS is taken by the robust internal diodes on the output of the ADG5412F. This protection action is repeated for each individual pulse in each burst.

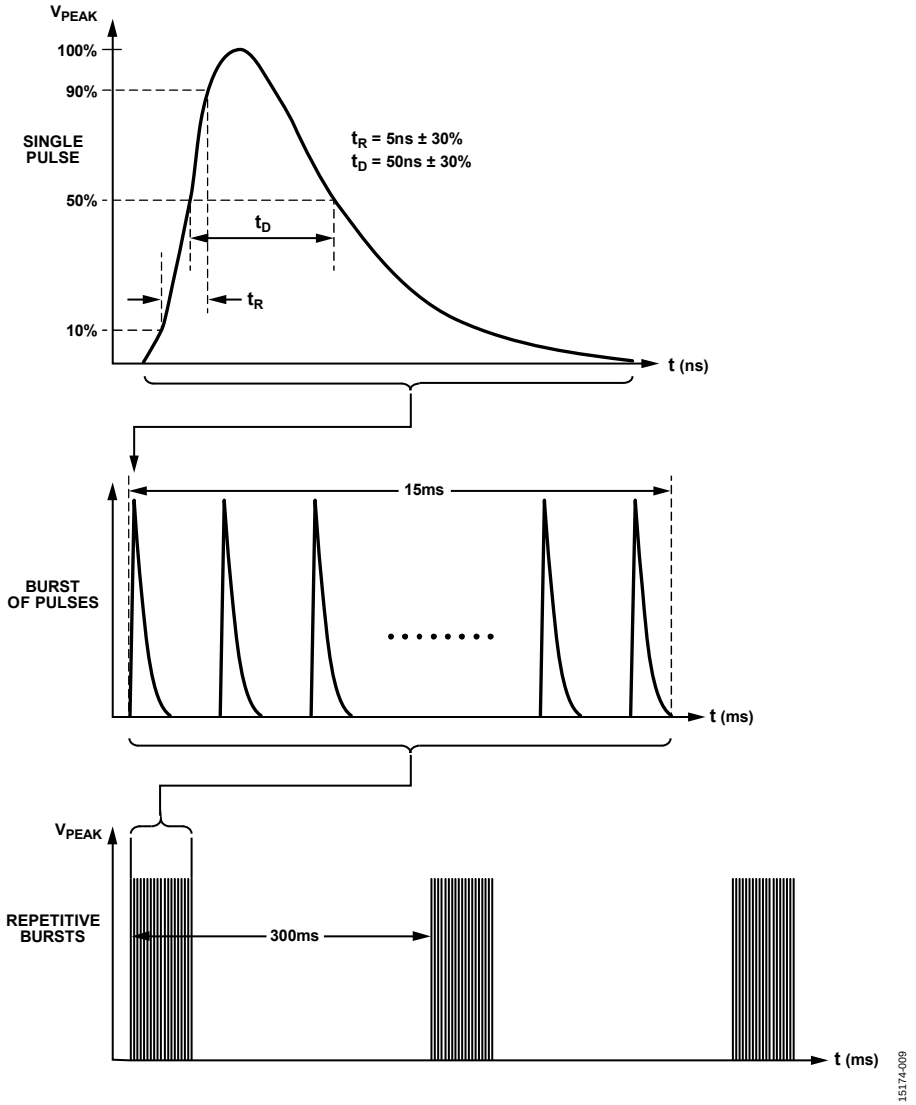


*Figure 11. IEC 61000-4-4 EFT Waveform*

## EFTs TESTING, IEC61000-4-4

Figure 12 shows a ±4 kV IEC EFT pulse applied to the input of an ADG5412F device with a 54 V TVS and a 30 Ω series resistor. The peak current measured at the output during one of the pulses in an EFT burst at the output is just 420 mA.

Similar to the ESD event, this value can be used to compare this short duration pulse of approximately 60 ns with peak currents used to classify HBM ESD events. A HBM ESD strike of 750 V has a peak current of approximately 500 mA and a duration of 500 ns. Therefore, using the ADG5412F in the configuration shown in Figure 5 can attenuate a single pulse from a 4 kV IEC EFT strike to less than the equivalent of a 750 V HBM ESD event, which most modern ICs are able to withstand.

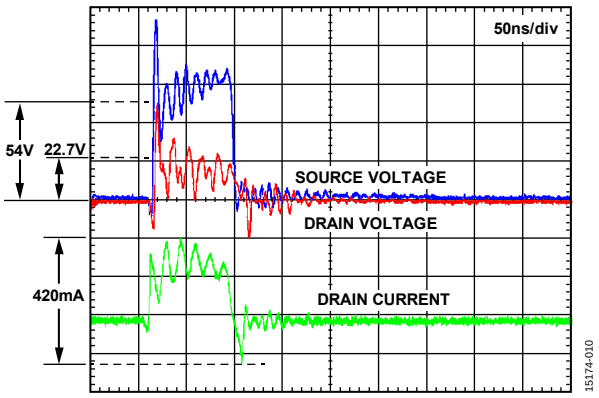


*Figure 12. EFT Current for a Single Pulse*

# SURGE

Surge transients are caused by overvoltages from switching or lightning transients. Switching transients can result from power system switching, load changes in power distribution systems, or various system faults, such as short circuits and arcing faults to the grounding system of the installation. Lightning transients can be a result of high currents and voltages injected into the circuit from nearby lightning strikes. IEC 61000-4-5 defines waveforms, test methods, and test levels for evaluating the immunity of electrical and electronic equipment when subjected to these surges.

The waveforms are specified as the outputs of a waveform generator in terms of open-circuit voltage and short-circuit current. Two waveforms are described. The 10 µs/700 µs combination waveform is used to test ports intended for connection to symmetrical communication lines, for example, telephone exchange lines. The 1.2 µs/50 µs combination waveform is used in all other cases, in particular short distance signal connections.

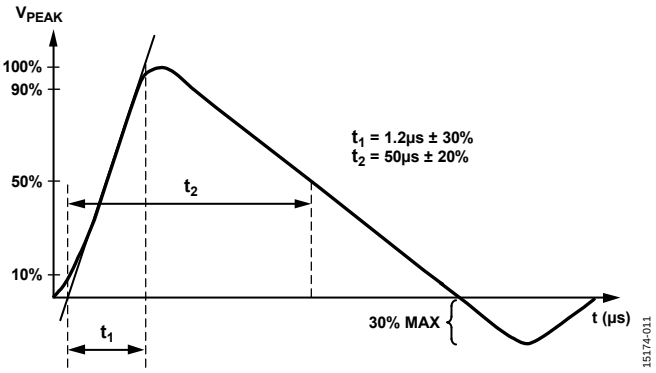


*Figure 13. IEC 61000-4-5 Surge 1.2 µs/50 µs Waveform*

Figure 13 shows the 1.2 µs/50 µs surge transient waveform. ESD and EFT have similar rise times, pulse widths, and energy levels. However, with surge, the rise time of the pulse is much slower at just 1.2 µs and the duration is much longer; the pulse width is 50 µs, and both values are far greater than the ESD pulse and the individual pulse of the EFT. The surge pulse can have energy levels that are three to four orders of magnitude larger than the energy in an ESD or EFT pulse. Therefore, the surge transient is considered the most severe of the EMC transient specifications. During a surge event voltage on the input is clamped by the TVS device. Because the surge event duration is 50 µs, there is adequate time for the OVP of the switch to react and isolate the downstream circuitry. After just 500 ns, the OVP of the ADG5412F isolates the downstream devices from the transient. In effect, this turns a 50 µs surge input into a 500 ns pulse, drastically reducing the energy transmitted to downstream components.

## SURGE TESTING, IEC61000-4-5

When a ±4 kV surge pulse is applied to the input of an ADG5412F with a 54 V TVS and a 30 Ω series resistor, the peak current measured at the output is 616 mA.

This protection circuit shown in Figure 4 attenuates a potentially destructive long duration high current surge event to a short, less than 500 ns duration event with a peak current of 608 mA. By comparison, an HBM ESD event of 1 kV has a peak current of approximately 660 mA and a duration of 500 ns.

Figure 14 shows the actuation of the switch after 500 ns, isolating the drain from the surge event.

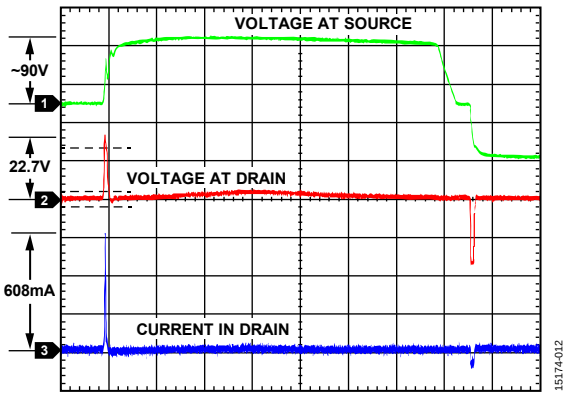


*Figure 14. Operation of OVP During a Surge Event*

## CONCLUSION

The protection architecture discussed in this application note shows how the use of the ADG5412F, combined with a single TVS device and a low value series resistor, protects a system input or output node against transient voltages of up to 16 kV IEC ESD, 4 kV EFT, and 4 kV surge. This application note also discusses how the protection architecture described reduces the protection needs of downstream circuitry to just a level equivalent to 1 kV HBM ESD. This information provides system designers with the knowledge required to design protection circuitry for system inputs and outputs while achieving the following benefits:

- Ease of protection design.
- Faster time to market.
- Higher protection circuit performance due to reduced number of discrete components required.
- Reduced values of series resistance in the signal path.
- Ease of TVS selection due to wide TVS design window.
- System level protection for the following standards:
  - IEC61000-4-2 16 kV air discharge.
  - IEC61000-4-2 8 kV contact discharge.
  - IEC61000-4-4 4 kV.
  - IEC61000-4-5 4 kV.
- AC and persistent dc overvoltage protection up to ±55 V.
- Power off protection up to ±55 V.

## REFERENCES

*Electromagnetic Compatibility (EMC) Part 4-2*: "Testing and Measurement Techniques—Electrostatic Discharge Immunity Test" (IEC 61000-4-2:2008, Edition 2.0).

*Electromagnetic Compatibility (EMC) Part 4-4*: "Testing and Measurement Techniques—Electrical Fast Transient/Burst Immunity Test" (IEC 61000-4-4:2012, Edition 3.0).

*Electromagnetic Compatibility (EMC) Part 4-5*: "Testing and Measurement Techniques—Surge Immunity Test" (IEC 61000-4-5:2005, Edition 2.0).

*JEDEC JS-001*: "Human Body Model Electrostatic Discharge Testing Standard" (ESDA/JEDEC JTR001-01-12).

Manning, Michael. *Ask The Applications Engineer—40: Switch and Multiplexer Design Considerations for Hostile Environments* (Analog Dialogue, 2011).

O'Sullivan, Paul. *Replacing Discrete Protection Components with Overvoltage Fault Protected Analog Switches* (Analog Dialogue, 2016).