PoE Powered Device and 48V/850mA Active Clamp Forward DC-DC Converter Using the MAX5974C and MAX5969B

MAXREFDES1273

Introduction

The MAXREFDES1273 is a Power-over-Ethernet (PoE) powered device (PD) and an active clamp forward DC-DC converter (ACFC) that delivers up to 850mA at 48V from 39V to 57V supply voltage. It is designed for the PD system to comply with the IEEE® 802.3af/at standard in a PoE system. The MAXREFDES1273 illustrates techniques using the active clamp forward topology to generate isolated output. This document explains how the MAX5969B and MAX5974C can be used to design the PD to generate 48V from 39V to 57V input voltage. An overview of the design specification is shown in Table 1.

Power over Ethernet is a technology that allows network cables to deliver power to a PD through power sourcing equipment (PSE) or midspan and has many advantages over traditional methods of delivering power. The PoE technology allows power and data to be combined, removing the need for altering the AC mains infrastructure and can be installed by nonelectricians. Power over Ethernet is an intelligent system designed with protection at the forefront, preventing overload, underpowering, and installation errors, while allowing simple scalability and reliability.

The MAX5974C provides control for wide-input-voltage, active-clamped, current-mode pulse-width modulation (PWM), forward converters in PoE powered device applications. The MAX5974C is well-suited for universal or telecom input range.

Other features include the following:

- Programmable switching frequency from 100kHz to 600kHz
- Programmable frequency dithering for low-EMI, spread-spectrum operation
- Programmable dead time, PWM soft-start, current slope compensation
- Programmable feed-forward maximum duty-cycle clamp, 80% maximum limit
- Frequency foldback for high-efficiency light-load operation
- Internal bootstrap UVLO with large hysteresis
- 100µA (typ) startup supply current
- Fast cycle-by-cycle peak current-limit, 35ns typical propagation delay
- 115ns current-sense internal leading-edge blanking
- Output short-circuit protection with hiccup mode
- Reverse current limit to prevent transformer saturation due to reverse current

Table 1. Design Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Voltage	V_{IN}	39V	48V	57V
Frequency	f_{SW}		250kHz	
Maximum Efficiency	η		88%	
Output Voltage	V_{OUT}	47.52V	48V	48.48V
Output Voltage Riplle	ΔV_{OUT}		480mV	
Output Current Range	I_{OUT}	0A		850mA
Output Power	P_{OUT}	0W		40.8W

Hardware Specifications

This reference circuit consists of the MAX5969B PD controller and an isolated active forward DC-DC con-verter using the MAX5974C to demonstrate a 24V DC output application. A 1GbE RJ45 magnetic jack is also included along with two diode bridges for separating data and DC power provided by an endspan or midspan PoE system. The power supply delivers up to 1A at 24V. Table 1 is an overview of the design specifications.

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed technical guide to designing a complete interface for a PD to comply with the IEEE 802.3af/at standard in a PoE, class 4 system and an isolated ACFC using Maxim's MAX5974C controller. The power supply has been built and tested.

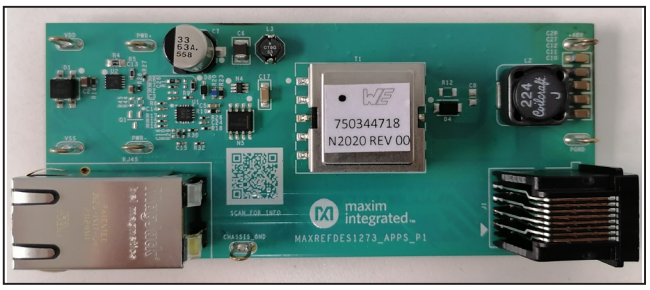

Figure 1. MAXREFDES1273 hardware.

MAX5969B PD Interface

A PoE system delivers power and data to an end device (PD) typically through an RJ45 cable power from an endspan (Power Sourcing Equipment [PSE]) (see Figure 2) or a midspan (see Figure 3). The power is separated from the data through diode bridges to deliver a typical 48V for efficient power transfer, which is low enough to be considered a safe voltage, and this removes the need to rewire AC mains, and saves cost.

Although this voltage is safe for humans, it still can damage equipment if not properly delivered. This is where MAX5969B classification is required, ensuring the equipment can handle the power delivery. Before the PSE can enable power to a connected Internet protocol (IP) camera or other PD, it must perform a signature detection.

Signature Detection

Signature detection uses a lower voltage to detect a characteristic signature of IEEE-compatible PDs (with a 24.9kΩ resistance). See Figure 4. Once this signature is detected, the PSE knows that higher voltages can be safely applied. The PSE applies two voltages on V_{IN} in the range of 1.4V to 10.1V (1V step minimum) and then records the current measurements at the two applied voltages. The PSE then computes the change in current when each voltage is applied (ΔV/ΔI) to ensure the presence of the 24.9kΩ signature resistor.

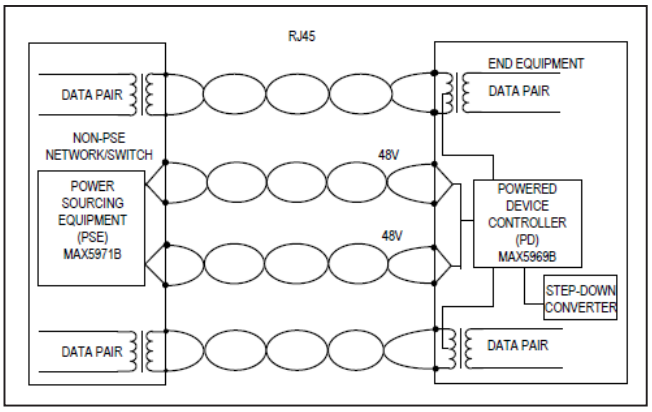

Figure 2. PoE endspan power injector.

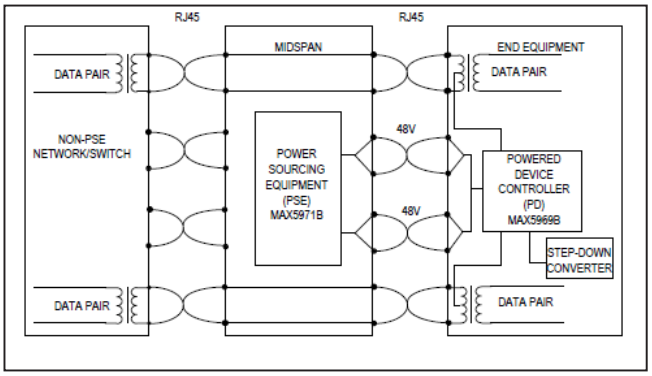

Figure 3. PoE midspan power injector.

Classification

In classification mode, the PSE classifies the PD based on the power consumption required. (The IEEE 802.3af/at standard defines only Class 0 to 4 and Class 5 for any special requirement.)

An external resistor (RCLS) of 30.9Ω connected from CLS to V_{SS} sets the classification current. The PSE determines the class of a PD by applying a voltage at the PD input and measuring the current sourced from the PSE. When the PSE applies a voltage between 12.6V and 20V, the MAX5969A/MAX5969B exhibit a current of 36mA to 44mA.

The PSE uses the classification current information to classify the power requirement of the PD (MAX5969B).

The classification current includes the current drawn by RCLS and the supply current of the MAX5969A/MAX5969B so the total current drawn by the PD is within the IEEE 802.3af/at standard figures. The classification current is turned off whenever the device is in power mode (see Figure 5).

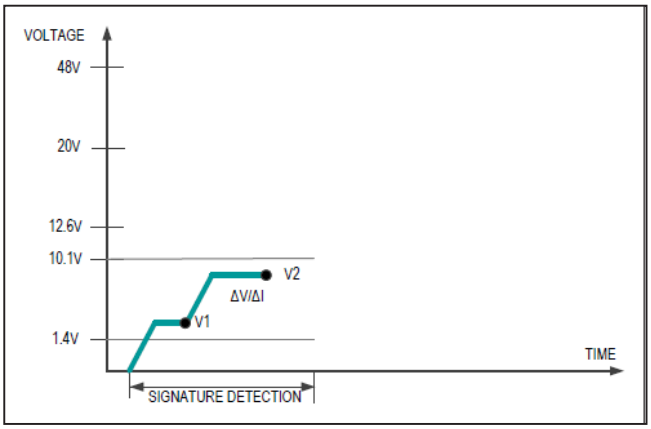

Figure 4. Signature detection.

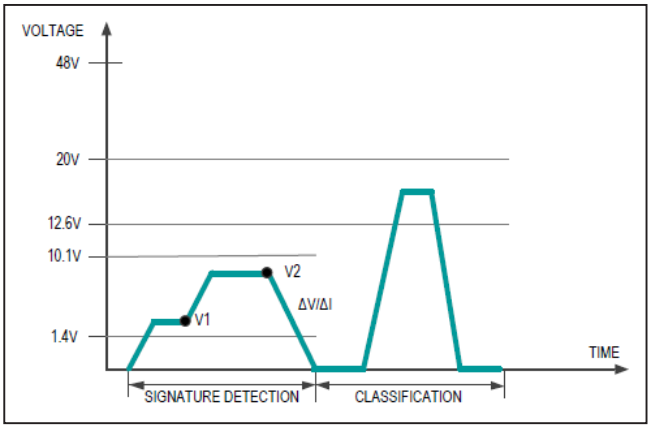

Figure 5. Classification.

Power Mode

The final stage after detection and classification of a newly connected PD is to enable power. The 48V supply from the PSE is connected to the PD through the RJ45 cable. Once enabled, the PSE continues to monitor how much current is being delivered to the PD and cuts power to the cable if the power drawn is not within the correct range. This protects the PSE against overload, underpowering and ensuring that the PSE is disconnected from the cable if the PD is unplugged or faulted. See Figure 6.

The MAX5969B enters power mode when V_{IN} rises above the undervoltage lockout (UVLO) threshold (V_{ON}). Note that V_{ON}/V_{OFF} = 38.6V/31V for the MAX5969B. When V_{IN} rises above V_{ON}, the MAX5969B turns on the internal n-channel isolation metal-oxide semiconductor field-effect transistor (MOSFET) to connect GND to RTN. The open-drain power-good (PG) output remains low for a minimum of t_{DELAY} until the power MOSFET fully turns on to keep the downstream DC-DC converter disabled during inrush. The open-drain PG output is also connected to three small-signal transistors to prevent the DC converters from powering up before the power from the PD is allowed.

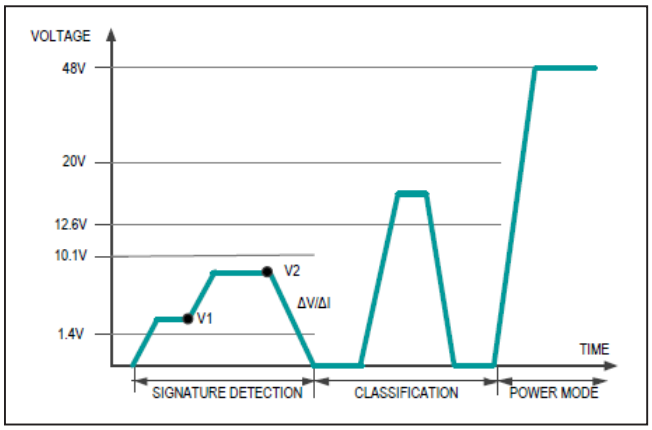

Figure 6. Power enabled.

Design Considerations for MAX5969B

Place the input capacitor, classification resistor, and transient voltage suppressor as close as possible to the MAX5969A/MAX5969B. Use large surface-mount technology (SMT) component pads for power dissipating devices such as the MAX5969A/MAX5969B and the external diodes. Use short and wide traces for high-power paths.

The MAX5969B enters UVLO when the input voltage drops below 31V. When the input drops below this value, the isolation MOSFET switches off, disconnecting the 48V from the buck converters. The MAX5969B exits UVLO when the input exceeds 38.6V, where the isolation MOSFET switches on again, connecting the MAX5974C forward converter.

The Active Clamp Forward Converter

The single ended forward converter has always been a favorite of designers for single and multiple output power supplies in the range from watts to kilowatts. In this topology, a second out-of-phase winding (reset winding) is used to reset the magnetic flux in the power transformers core during the time the secondary side freewheeling diode is conducting. If the number of turns on this winding is equal to the number of turns on the main transformers' primary winding the drain-source voltage of the main power switch is limited (excluding ringing due to leakage inductance and parasitic capacitance in the circuit) to two times the input voltage of the power supply but so too is the maximum duty cycle limited to less than 50%. This duty cycle limit can be extended above 50% to improve transformer utilization by increasing the number of turns on the reset winding but only at the expense of a higher drain-source voltage (increased voltage stress and switching power losses) on the main power switch.

These and other limitations of the forward converter can easily be overcome when the designer fully understands the operation and unique benefits of the ACFC topology.

Table 2. Setting Classification Current

CLASS	MAXIMUM POWER USED BY PD (W)	R_{CLS} (Ω)	V_{IN}* (V)	CLASS CURRENT SEEN AT V_{IN} (mA)		IEEE 802.3af/at PSE CLASSIFICATION CURRENT SPECIFICATIONS (mA)	
				MIN	MAX	MIN	MAX
0	0.44 to 12.95	619	12.6 to 20	0	4	0	5
1	0.44 to 3.94	117	12.6 to 20	9	12	8	13
2	3.84 to 6.49	66.5	12.6 to 20	17	20	16	21
3	6.49 to 12.95	43.7	12.6 to 20	26	30	25	31
4	12.95 to 25.5	30.9	12.6 to 20	36	44	35	45
5	> 25.5	21.3	12.6 to 20	52	64	—	—

The main components of an ACFC are shown in Figure 7. The active clamp consists of a P-channel MOSFET (Q_{AUX}) and a clamp capacitor (C_{CLAMP}). The difference between the traditional forward converter and the ACFC occurs when the main power MOSFET (Q_{MAIN}) is off. The reset winding and diode of the traditional forward converter clamps the drain-source voltage of QMAIN to approximately twice the power supply input voltage during the first half of the interval when Q_{MAIN} is off whereas in the ACFC the drain-source voltage of Q_{MAIN} is clamped to an intermediate voltage between V_{IN} and $2V_{IN}$ for the full interval when Q_{MAIN} is off.

The benefits of the ACFC topology go far beyond reducing the voltage stress on the main power MOSFET and increasing the duty cycle limit.

Further benefits provided by the ACFC topology are as follows:

- Zero voltage switching (ZVS) can be achieved for Q_{MAIN} and Q_{AUX} over the full load range by careful design thus significantly improving power supply efficiency.
- A smaller output inductance can be used due to higher operating duty cycle.
- Operating at higher than 50% duty cycle allows a higher secondary to primary turns ratio on thetransformer leading to a lower reflected current from secondary to primary and thus a lower peak current in the main power MOSFET.
- There is lower electromagnetic interference (EMI) due to the ZVS nature of the switching.
- Figure 8 shows the main steady state waveforms of the ACFC. It is very important to understand what is happening during one complete switching cycle of the converter.

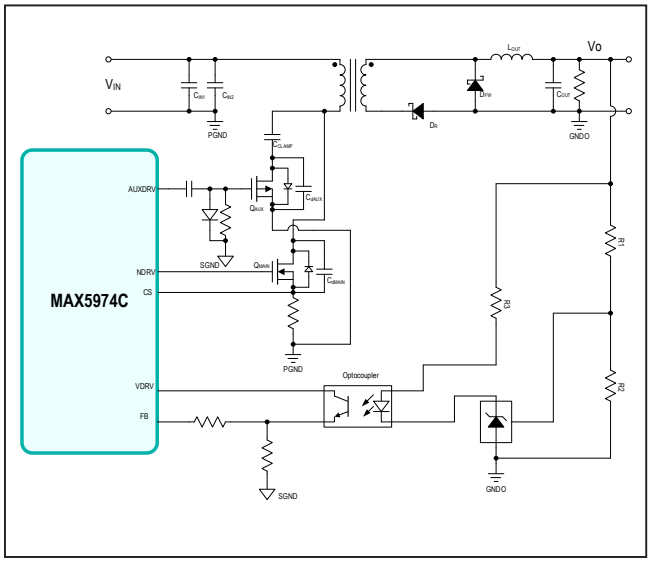

Figure 7. Active clamp forward converter topology.

Time Interval t_0 to t_1

Q_{MAIN} turns on at t_0 Q_{AUX} remains off. The primary current IP, which is the sum of the transformer magnetizing I_{MAG} and the reflected secondary current I_{SEN}, flows through the primary of the transformer and Q_{MAIN}. I_P ramps up linearly while Q_{MAIN} is on. Current also flows on the secondary side through the rectifying diode D_R while Q_{MAIN} is on. No current flows through Q_{AUX} during this interval.

Time Interval t_1 to t_2

Q_{MAIN} turns on at t_1. D_R is now reverse biased so the reflected secondary current component of I_P is zero. I_P is now only the transformer magnetizing current. It decreases toward zero charging the drain capacitance of Q_{MAIN}, C_{dMAIN}.

Time Interval t_2 to t_3

At t_2, the drain voltage of Q_{MAIN} reaches the same voltage level as the voltage across C_{CLAMP}, the body diode of Q_{AUX} becomes forward biased, and the voltage across C_{CLAMP} increases. The rate of increase of the drain voltage of Q_{MAIN} is now much lower since C_{CLAMP} >> C_{dMAIN}.

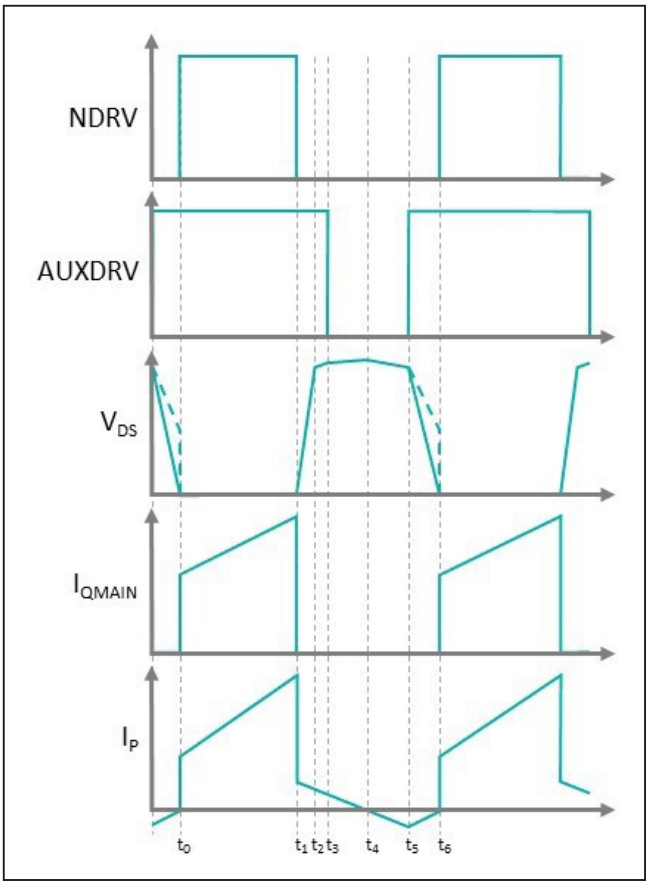

Figure 8. ACFC waveforms.

Time Interval t_3 to t_4

At t_3, Q_{AUX} turns on. Q_{AUX} switches under the ZVS condition providing it turns on after its body diode starts conducting (at t_2) and before I_P goes negative (at t_4). Q_{AUX} must turn on before t4 otherwise IP has no path to go negative at t_4.

Time Interval t_4 to t_5

At t_4, I_P is now negative and is discharging C_{CLAMP} through Q_{AUX}, which is on. I_P continues to become more negative and the drain voltage of Q_{MAIN} decreases.

Time Interval t_5 to t_6

Q_{AUX} turns off at t_5 and the voltage across C_{CLAMP} stops decreasing. The only current path now available for the negative I_P to flow is out of C_{dMAIN}. The voltage across C_{dMAIN} keeps decreasing until I_P reaches zero. V_{DS} decays to zero by t_6 providing the energy stored in the magnetizing and leakage inductance at t_5 is greater than the energy stored in C_{dMAIN} at t5. ZVS occurs if this condition is met otherwise Q_{MAIN} switches on at t_6 at some intermediate voltage between zero and V_{DSMAX}.

IMPORTANT: Reducing L_{MAG} increases the inductive energy stored in L_{MAG} so if L_{MAG} is too big ZVS does not occur as shown by the dashed line on the V_{DS} graph.

Design Procedure for the ACFC

Now that the principle of operation of the ACFC is understood, a practical design example can be illustrated. The converter design process can be divided into several stages: power stage design, setup of the MAX5974C ACFC current mode controller, and the feedback loop. This document is primarily concerned with the power stage design, and the feedback loop is intended to complement the information contained in the MAX5974C data sheet for details on how to set up supervisory and protection functions of the controller.

The following design parameters are used throughout:

PARAMETER	VALUE
V_{IN}	Input Voltage
V_{OUT}	Output Voltage
ΔV_{OUT}	Output Ripple Voltage
I_{OUT}	Output Current
P_{OUT}	Output Power
η	Target Maximum Efficiency
P_{IN}	Input Power
f_{SW}	Switching Frequency
D	Duty Cycle
n	Primary-Secondary Turns Ratio
N_P	Turns of Primary Winding
N_S	Turns of Secondary Winding
N_{AUX}	Turns of Tertiary Winding

The above symbols are sometimes followed by parentheses to indicate whether minimum or maximum values of the parameters are intended; for example, minimum input voltage is intended by the symbol $V_{IN(MIN)}$. Otherwise, typical values are intended.

In addition, through the design, procedure reference is made to the schematic in another document.

Step 1: Choosing a Suitable Switching Frequency

The MAX5974C can operate at a switching frequency between 100kHz and 600kHz. A lower switching frequency optimizes the design for efficiency, whereas a higher frequency allows for smaller inductive and capacitive components as well as lower costs. A switching frequency of 250kHz was chosen for this design. R15 sets the switching frequency according to the following expression:

$$R15 = \frac{8.7 \times 10^9}{f_{SW}} = \frac{8.7 \times 10^9}{250 \times 10^3 Hz} = 34.8k\Omega$$

Step 2: Setting the Maximum Duty Cycle

One advantage of using the MAX5974C for the ACFC is the maximum allowable duty cycle. If the duty cycle is not clamped at some maximum value, transformer saturation can occur, resulting in catastrophic failure, and Q_{MAIN} can be subjected to increased voltage stress. A maximum duty cycle of 80% is recommended at switching frequencies up to 400kHz. An initial choice of 62% allows for some design margin.

$$D_{MAX} = 0.62$$

Step 3: Calculating the Transformer Turns Ratio

For the forward converter topology, the transformer turns ratio is given by the following expression:

$$n = \frac{V_{IN(MIN)} - V_{MDS(ON)}}{V_{DR(F)} + V_{LOUT} + \frac{V_{OUT}}{D_{MAX}}}$$

where $V_{MDS(ON)}$ is the drain-source voltage of Q_{MAIN} in the on state, $V_{DR(F)}$ is the forward voltage drop of D_R, and V_{LOUT} is the resistive DC voltage drop across the output inductor winding. D_{MAX} occurs at $V_{IN(MIN)}$. Assuming $V_{MDS(ON)}$ = 0.2V, $V_{DR(F)}$ = 0.5V, and V_{LOUT} = 0.2V, then

$$n = \frac{N_P}{N_S} = \frac{39V - 0.2V}{0.5V + 0.2V + \frac{48V}{0.62}} = 0.4967$$

Step 4: Calculating Turns of Primary Winding N_P, Secondary Winding N_S, and Tertiary Winding N_{AUX}

For the forward converter topology, the transformer turns of the primary winding is given by the following expression:

$$N_P = \frac{V_{IN(MIN)} \times D_{MAX}}{\Delta B \times Ae \times f_{SW}} \times 10^4$$

where Δ_B is the flux density deviation of the transformer, which should be below or equal to 2000GS, Ae is the effective magnetic cross-section of the transformer core. Considering the maximum output power and the size of this design, we chose EFD20 as the transformer core. If the effective magnetic cross of EFD20 is 0.31cm^2, then

$$N_P = \frac{39V \times 0.62}{2000GS \times 0.31 \times 10^{-4} m^2 \times 250kHz} \times 10^4 = 15.6T \approx 16T$$

We use 16 turns for the primary winding; for the secondary turns,

$$N_S = \frac{N_P}{n} = \frac{16T}{0.4967} = 32.21T \approx 32T$$

If we use 32 turns for the secondary winding, then

$$n = \frac{N_P}{N_S} = \frac{16T}{32T} = 0.5$$

During normal operation, the voltage at IN is normally derived from a tertiary winding of the transformer. For the tertiary winding turns,

$$N_{AUX} = N_S \times \frac{V_{AUX}}{V_{OUT}} = 32T \times \frac{12}{48} = 8T$$

We use 8 turns for the tertiary winding.

Step 5: Calculate D at $V_{IN(MIN)}$, $V_{IN(TYP)}$, and $V_{IN(MAX)}$

Re-arranging the expression in Step 3 gives

$$D = \frac{V_{OUT}}{\left(\frac{V_{IN} - V_{MDS(ON)}}{n}\right) - V_{DR(F)} - V_{LOUT}}$$

And,

D_{MIN}	D_{TYP}	D_{MAX}
0.425	0.5058	0.624

Step 6: Calculate $V_{MDS(MAX)}$ of Q_{MAIN} at DMIN, DTYP, and D_{MAX}

For the forward converter topology, V_{MDS} is given by the following expression:

$$V_{MDS} = \frac{V_{IN}}{1 - D}$$

Given the D_{MAX} occurs at $V_{IN(MIN)}$, D_{TYP} occurs at $V_{IN(TYP)}$, and D_{MIN} occurs at $V_{IN(MAX)}$, we have

V_{MDS} at $V_{IN(MAX)}$	V_{MDS} at $V_{IN(TYP)}$	V_{MDS} at $V_{IN(MIN)}$
99.13V	97.13V	103.72V

The critical operating parameters of the converter are now fixed, so it is possible to continue the design process of calculating and selecting suitable components for the power train.

Step 7: Calculating and Selecting L_{OUT}

The output inductance is calculated assuming a maximum peak-to-peak output ripple (ΔI_{SEC}), which occurs at maximum input voltage. The output inductance can be calculated as follows:

$$L_{OUT} = \frac{\left(V_{OUT} - V_{DFW(F)}\right) \times \left(1 - D_{MIN}\right)}{I_{OUT} \times \%\Delta I_{SEC} \times f_{SW}}$$

Where $V_{DFW(F)}$ is the forward voltage drop of the secondary freewheeling diode and $\%\Delta I_{SEC}$ (0.6, typical) is the ratio of peak-to-peak output inductor current ripple to the average output current at maximum input voltage. We have

$$L_{OUT} = \frac{(48V - 0.5V) \times (1 - 0.425)}{0.85A \times 0.6 \times 250kHz} = 214.22uH$$

Where I_{OUT} = 850mA and $V_{DFW(F)}$ = 0.5V. In this design, we can choose a standard ±20% tolerance 220µH inductor. Finally, we must choose an output inductor with a DC winding resistance that is sufficiently low to ensure that V_{LOUT} is less than 0.2V at $I_{O(MAX)}$ because this is the value we have used for VLOUT in the preceding calculations. We should choose an inductor with

$$R_{LDC} < \frac{V_{LOUT}}{I_{OUT(MAX)}} = \frac{0.2V}{85A} = 0.24\Omega$$

The final inductor value chosen for this design is a 10% tolerance 220µH/1.42A/335mΩ inductor MSS1260-224KL from Coilcraft®.

Step 8: Calculate the Transformer Magnetizing Inductance L_{MAG} and the Secondary and Primary Peak Winding Currents, $I_{S(PK)}$ and $I_{P(PK)}$

The physical design of the power transformer is outside the scope of this document; however, it is necessary to calculate the critical parameters of the transformer.

We must first calculate the minimum output inductor ripple current by rearranging the expression in Step 7 and remembering that minimum ripple occurs at D_{MAX} as follows:

$$\Delta I_{L(MIN)} = \frac{\left(V_{OUT} - V_{DFW(F)}\right) \times \left(1 - D_{MAX}\right)}{L_{OUT(MAX)} \times f_{SW}}$$

$L_{OUT(MAX)}$ for the selected ±20% 100µH inductor is 120µH. So,

$$\Delta I_{L(MIN)} = \frac{(48V - 0.5V) \times (1 - 0.624)}{242\mu H \times 250kHz} = 0.295A$$

For the MAX5974C ACFC current mode controller to function properly, the maximum magnetizing current referred to the primary side of the transformer must be less than the minimum output inductor ripple current reflected to the primary side of the transformer. So,

$$I_{MAG(MAX)} < \frac{\Delta I_{L(MIN)}}{n}$$

And,

$$I_{MAG(MAX)} < \frac{0.295A}{0.5} = 0.59A$$

To allow for design margin, we chose a value for I_{MAG} = 0.5A (85% of $I_{MAG(MAX)}$). The next step is to calculate a minimum magnetizing inductance that ensures that $I_{MAG(MAX)}$ < 0.5A. The following expression is used to calculate $L_{MAG(MIN)}$:

$$L_{MAG(MIN)} = \frac{\left(V_{IN(MAX)} - V_{DS(ON)}\right) \times D_{MIN}}{I_{MAG(MAX)} \times f_{SW}}$$

So,

$$L_{MAG(MIN)} = \frac{(57V - 0.2V) \times 0.425}{0.5A \times 250kHz} = 193.12\mu H$$

Allowing for a ±30% tolerance for the magnetizing inductance, we can choose L_{MAG} = 300µH±30%.

Figure 9 illustrates the output inductor current I_L, the secondary transformer current I_S, primary transformer current I_P, and the current flowing in main power MOSFET, I_{QMAIN}.

Although I_P appears linear when both Q_{MAIN} and Q_{AUS} are off (t_1 to t_3 and t_5 to t_6), there is a resonance between the two end points, which makes ZVS possible.

The peak current in the secondary winding $I_{S(PK)}$ is equal to the peak current in the output inductor $I_{L(PK)}$. The peak current $I_{L(PK)}$ is a maximum at $V_{IN(MAX)}$ and $I_{O(MAX)}$, therefore:

$$I_{L(PK)} = I_{O(MAX)} + \frac{\left(V_{OUT} - V_{DFW(F)}\right) \times \left(1 - D_{MIN}\right)}{2 \times L_{OUT(MIN)} \times f_{SW}}$$

And,

$$I_{S(PK)} = I_{L(PK)}$$

So,

$$I_{S(PK)} = 0.85A + \frac{(48V - 0.5V) \times (1 - 0.425)}{2 \times 198\mu H \times 250kHz} = 1.13A$$

The peak current in the primary winding $I_{P(PK)}$ is the peak current in the secondary winding reflected back to the primary side of the transformer plus I_{MAG}. Therefore,

$$I_{P(PK)} = \frac{I_{S(PK)}}{n} + I_{MAG}$$

So,

$$I_{P(PK)} = \frac{1.13A}{2} + 0.5A = 2.76A$$

The transformer must not saturate at a magnetizing force of (N_P x $I_{P(PK)}$) where NP is the number of turns on the primary winding.

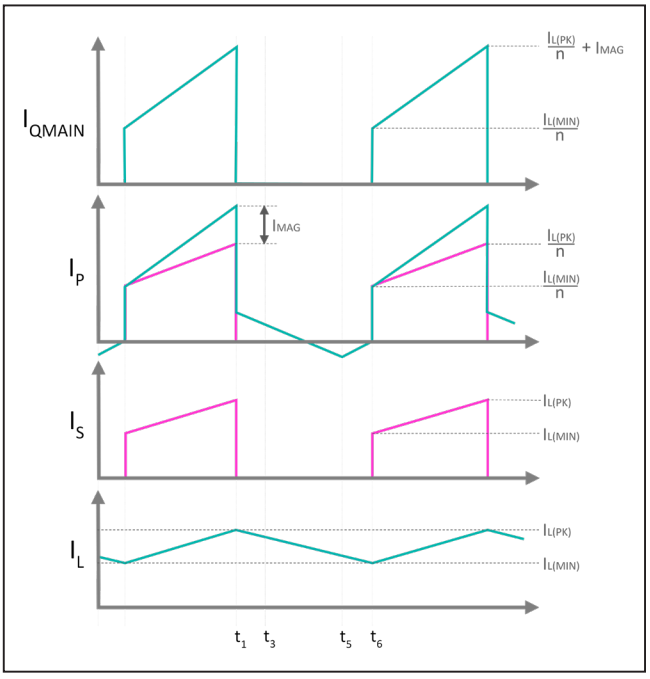

Figure 9. Current waveforms.

Step 9: Calculate the Maximum RMS Currents in the Transformer Secondary and Primary Windings, $I_{S(RMS)}$ and $I_{P(RMS)}$

The maximum root mean square (RMS) currents in the transformer primary and secondary windings occur at $V_{IN(MIN)}$ and $I_{OUT(MAX)}$, i.e., at D_{MAX}. To calculate $I_{S(PK)}$ at $V_{IN(MIN)}$, we must first calculate $I_{L(PK)}$ in the output inductor at $V_{IN(MIN)}$.

Following the process of Step 8 we have,

At $V_{IN(MIN)}$,

$$I_{L(PK)} = I_{O(MAX)} + \frac{\left(V_{OUT} - V_{DFW(F)}\right) \times \left(1 - D_{MAX}\right)}{2 \times L_{OUT(MIN)} \times f_{SW}}$$

And,

$$I_{S(PK)} = I_{L(PK)}$$

So,

$$I_{S(PK)} = 0.85A + \frac{(48V - 0.5V) \times (1 - 0.624)}{2 \times 198\mu H \times 250kHz} = 1.03A$$

The current at which the secondary rectifying diode D_R starts to conduct $I_{S(V)}$, corresponds to $I_{L(MIN)}$.

So,

$$I_{S(V)} = 0.85A - \frac{(48V - 0.5V) \times (1 - 0.624)}{2 \times 198\mu H \times 250kHz} = 0.67A$$

We can now calculate the maximum RMS current in the secondary winding as follows:

$$I_{S(RMS)} = \sqrt{D_{MAX} \times \frac{I_{S(PK)}^2 + I_{S(PK)} \times I_{S(V)} + I_{S(V)}^2}{3}}$$

So,

$$I_{S(RMS)} = \sqrt{0.624 \times \frac{1.03^2 + 1.03 \times 0.67 + 0.67^2}{3}} = 0.534A$$

Referring to Figure 8, we can calculate the instantaneous current in Q_{MAIN} at turn-on and turn-off, $I_{QM(t\text{-}on)}$ and $I_{QM(t\text{-}off)}$, respectively.

$$I_{QM(t-on)} = \frac{I_{SV}}{n} = \frac{0.67A}{0.5} = 1.34A$$

$$I_{QM(t-off)} = \frac{I_{S(PK)}}{n} + I_{MAG} = \frac{1.13A}{0.5} + 0.5A = 2.76A$$

The maximum RMS current in Q_{MAIN} can now be calculated as follows:

$$I_{QM(RMS)} = \sqrt{0.624 \times \frac{1.34^2 + 1.34 \times 2.76 + 2.76^2}{3}} = 1.65A$$

The transformer primary current I_P, as shown in Figure 9, is a more complex waveform than I_{QM}. IP is a superposition of I_{QM} and I_{QA}, and the resonant currents that flow during the time intervals when both Q_{MAIN} and Q_{AUX} are off. Nevertheless, it is reasonable to use the approximation that

$$I_{P(RMS)} = I_{QM(RMS)}$$

We now have all the critical parameters of the transformer, as detailed in the following table.

PARAMETER	SYMBOL	VALUE
Primary Magnetizing Inductance	L_{MAG}	300µH±30%
Primary Peak Current	$I_{P(PK)}$	2.76A
Primary RMS Current	$I_{P(RMS)}$	1.65A
Turns Ratio (N_P/N_S)	n	0.5
Primary Turns	N_P	16T
Secondary Turns	N_S	32T
Tertiary Turns	N_{AUX}	8T
Secondary Peak Current	$I_{S(PK)}$	1.13A
Secondary RMS Current	$I_{S(RMS)}$	0.534A

Using these parameters in the table, a suitable transformer can be designed.

Step 10: Choose a Suitable MOSFET for Q_{MAIN}

All the necessary parameters for selecting a suitable QM have already been calculated.

From Step 6,

$$V_{DS(MAX)} = 103.72V$$

From Step 8,

$$I_{QM(PK)} = I_{P(PK)} = 2.76A$$

And,

$$I_{QM(RMS)} = 1.65A$$

Allowing for reasonable design margin, Fairchild part number FDC86242 was chosen for this design with the following specifications:

Maximum D-S Voltage	150V
Continuous Drain Current	3.3A
D-S Resistance at VGS = 4.5V	98mΩ
Total Gate Charge Qg	13nC

Step 11: Choose Suitable Rectifying and Freewheeling Diode for D_R and D_{FW}, Respectively

Almost all the necessary parameters for selecting a suitable D_R have already been calculated. In Step 8, we calculated $I_{S(PK)}$, the same peak current that flows in D_R.

So,

$$I_{DR(PK)} = I_{S(PK)} = 1.13A$$

In Step 9, we calculated the maximum RMS current in the transformer secondary winding $I_{S(RMS)}$, the same RMS current that flows in D_R.

So,

$$I_{DR(RMS)} = I_{S(RMS)} = 0.534A$$

The peak reverse voltage seen by D_R is given by

$$V_{DR(R)} = \frac{V_{IN(MIN)} \times D_{MAX}}{n \times (1 - D_{MAX})}$$

So,

$$V_{DR(R)} = \frac{39V \times 0.624}{0.5 \times (1 - 0.624)} = 129.45V$$

For the freewheeling diode D_{FW}, we have

$$I_{FW(PK)} = I_{S(PK)} = 1.13A$$

The maximum RMS current in the freewheeling diode occurs at $V_{IN(MAX)}$ and is calculated using

$$I_{FW(RMS)} = \sqrt{(1 - D_{MIN}) \times \frac{I_{FW(PK)}^2 + I_{FW(PK)} \times I_{FW(V)} + I_{FW(V)}^2}{3}}$$

where

$$I_{FW(V)} = I_{O(MAX)} - \frac{(V_{OUT} - V_{DFW}) \times (1 - D_{MIN})}{2 \times L_{OUT(MIN)} \times f_{SW}} = 0.574A$$

So,

$$I_{FW(RMS)} = 0.66A$$

Finally, the peak reverse voltage seen by D_{FW} is given by

$$V_{DFW(R)} = \frac{(V_{IN(MAX)} - V_{DR(F)})}{n} = \frac{(57V - 0.5V)}{0.5} = 113V$$

Allowing for a reasonable design margin, a Schottky diode, part number RB068LAM150TF, was selected for both D_R and D_{FW}.

Step 12: Choose Suitable P-Channel MOSFET for the Active Clamp Switch Q_{AUX}

Only a portion of the primary magnetizing current flows in the drain of the active clamp switch during the interval between t_3 and t_5. If we assume as the worst case that all the magnetizing current flows in Q_{AUX}, then we can estimate the RMS current flowing in the drain of Q_{AUX} as follows:

$$I_{MAG(RMS)} = \sqrt{D_{MAX} \times \frac{I_{MAG}^2}{3}} = \sqrt{0.624 \times \frac{0.5^2}{3}} = 0.23A$$

At such a low RMS current, conduction losses are very low, so choosing a MOSFET with a low gate charge should be the primary consideration, with low $R_{DS(ON)}$ being only a secondary concern. In addition to conduction losses being very low, switching losses are also negligible, because the body diode of Q_{AUX} is conducting before Q_A turns on. The repetitive peak current in Q_{AUX} is the maximum primary magnetizing current:

$$I_{QA(PK)} = I_{MAG} = 0.5A$$

The active clamp switch experiences the same voltage stress as the main power switch; referring to Step 6 this is as follows:

$$V_{DS(QA)} = V_{DS(QM)} = \frac{V_{IN(MAX)}}{1 - D_{MIN}} = 99.13V$$

Allowing for reasonable design margin, Vishay P-Channel MOSFET, SI1411DH-T1-GE3, was chosen for this design, with the following specifications:

Maximum D-S Voltage	150V
Peak Repetitive Drain Current	0.42A
D-S Resistance at V_{GS} = 7V	2.05Ω

Step 13: Choose a Suitable Clamp Capacitor C17

The clamp capacitor (C17) helps in resetting the flux in the transformer core as well absorbing leakage inductance energy, and it forms a complex pole-zero pair with the magnetizing inductance (L_{MAG}) of the transformer at a frequency f_R.

$$f_R = \frac{1 - D_{MAX}}{2\pi \times \sqrt{L_{MAG} \times C17}}$$

The value of the clamp capacitor for a 20% voltage ripple is calculated as:

$$C17 = \frac{I_{MAG} \times (1 - D_{MIN})^2}{1.6 \times V_{IN(MAX)} \times f_{SW}} = \frac{0.5A \times (1 - 0.425)^2}{1.6 \times 57V \times 250kHz} = 7.25nF$$

We chose 4.7nF as the clamp capacitor.

The voltage stress on the clamp capacitor can be calculated as:

$$V_{C17} = \frac{V_{IN}}{1-D}$$

The C17 should be rated for at least 1.4x the calculated worst-case V_{C12} stress.

Step 14: Calculate and Choose the Output Capacitor C_{OUT}

Output capacitance value can be calculated based on either steady-state voltage ripple or transient voltage ripple. If the design consideration is the transient steady-state voltage ripple, then the output capacitor is usually sized to support a step load of 25% of the rated output current (I_{OUT}) in isolated applications so that the output-voltage deviation is contained to 3% of the rated output voltage. The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

where C_{OUT} is the total capacitance required at the output, I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, and ΔV_{OUT} is the allowable output voltage deviation during the load transient.

Response time of the controller $t_{RESPONSE}$ is given as

$$t_{RESPONSE} = \frac{0.33}{f_C} + \frac{1}{f_{SW}}$$

The complex pole-zero pair frequency formed due to clamp capacitor and magnetizing inductance of the converter is given as

$$f_R = \frac{1-D_{MAX}}{2\pi \times \sqrt{L_{MAG} \times C17}} = \frac{1-0.624}{2\pi \times \sqrt{300\mu H \times 4.7nF}} = 50.42kHz$$

f_C is the target closed-loop crossover frequency, which is given as

$$f_C = \frac{f_R}{5} = \frac{50.42kHz}{5} = 10.084kHz$$

So, the response time of the controller $t_{RESPONSE}$ is given as

$$t_{RESPONSE} = \frac{0.33}{10.084kHz} + \frac{1}{250kHz} = 36.73\mu s$$

Choose I_{STEP} equal to 25% of output current, I_{STEP} = 0.2125A, ΔV_{OUT} = 3% of output voltage, which is equal to 1440mV.

So, the output capacitance is given as

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}} = \frac{0.2125A \times 36.73\mu s}{2 \times 1.44V} = 2.71\mu F$$

In this design, to get smaller output voltage ripple, 5 x 2.2µF ceramic capacitors are used. Considering 20% derating of the ceramic capacitors, the total ceramic output capacitance would be 5 × 2.2µF × 0.8 = 8.8µF.

Step 15: Calculate and Choose the Input Capacitor C_{IN}

Capacitor selection is based on switching ripple. The maximum average input current drawn from the input power supply at minimum input voltage can be calculated as

$$I_{IN(AVG)} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} = \frac{48V \times 0.85A}{0.91 \times 39V} = 1.15A$$

The voltage ripple present on the input capacitor is 2% of the minimum input voltage and is given as

$$\Delta V_{IN(RIPPLE)} = 0.02 \times V_{IN(MIN)} = 0.02 \times 39V = 0.78V$$

The value of the input ceramic capacitor with the above assumed ripple voltage can be calculated as follows:

$$C_{IN} = \frac{I_{IN(AVG)} \times (1-D_{MAX})}{\Delta V_{IN(RIPPLE)} \times f_{SW}} = \frac{1.15A \times (1-0.624)}{0.78V \times 250kHz} = 2.12\mu F$$

In this design, 2 × 1µF ceramic capacitors and one 33µF electrolytic capacitor are used for the input capacitor.

Step 16: Calculating and Selecting the Peak Current Limit Resistors (R21 and R25)

The current-sense resistor (R_{CS} in the Typical Application Circuits), connected between the source of the n-channel MOSFET and PGND, sets the current limit. The current limit comparator has a voltage trip level ($V_{CS-PEAK}$) of 400mV. Use the following equation to calculate the value of R_{CS}:

$$R21 + R25 = \frac{400mV}{I_{P(PK)}} = \frac{400mV}{2.76A} = 145m\Omega$$

Two standard 100mΩ current-sense resistors are used in the design. Low-inductance current-sense resistors should be used for R21 and R25.

Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/21	Initial release	—