Single Output Flyback Converter Using MAX17596

MAXREFDES1251

Introduction

The MAX17596 is a peak-current-mode controller for designing the wide input-voltage flyback regulators. The device offers input thresholds suitable for low-voltage DC-DC applications (4.5V–36V) and contains a built-in gate driver for an external n-channel metal-oxide semiconductor field-effect transistor (MOSFET). The MAX17596 houses an internal error amplifier with 1% accurate reference, eliminating the need for an external reference. The switching frequency is programmable from 100kHz to 1MHz with an accuracy of 8%, allowing optimization of magnetic and filter components, resulting in compact and cost-effective power conversion. For electromagnetic interference (EMI)-sensitive applications, the MAX17596 incorporates a programmable frequency dithering scheme, enabling low-EMI spread-spectrum operation. Users can start the power supply precisely at the desired input voltage, implement input overvoltage protection, and program soft-start time. A programmable slope compensation scheme is provided to ensure stability of the peak current-mode control scheme. Hiccup-mode overcurrent protection and thermal shutdown are provided to minimize dissipation in overcurrent and over-temperature fault conditions.

Hardware Specifications

A DC input discontinuous conduction mode (DCM) flyback converter using the MAX17596 is demonstrated for a 3.3V DC output application. The power supply delivers up to 500mA at 3.3V. Table 1 shows an overview of the design specifications.

Table 1. Design Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX
DC Input Voltage	V_{IN}	10.5V	14V	17V
AC Input Voltage	V_{AC}	10V		12V
Frequency	f_{SW}		100kHz	
Maximum Efficiency	η			
Output Voltage	V_{OUT}		3.3V	
Output Voltage Ripple	ΔV_{OUT}			
Output Current	I_{OUT}	0	500mA	
Output Power	P_{OUT}		1.65W	

Designed–Built–Tested

This reference design document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing a DC-DC DCM flyback using Maxim's MAX17596 current-mode controller. The power supply has been built and tested, details of which follow later in this document.

Figure 1. MAXREFDES1251 hardware.

Quick Start

Required Equipment

- AC-DC Power Supply: Chroma Systems 62015L-60-6
- Electronic Load: Keithley® 2380-120-60
- Oscilloscope: Teledyne® LeCroy® WaveSurfer 3024z
- Multimeter: FLUKE117

Procedure

The reference design is fully assembled and tested. The steps to verify the board operation are as follows:

1) The reference design is fully assembled and tested.
2) Set the power-supply voltage to 14V and current limit to 500mA.
3) Connect the positive terminal of the power supply to the V_{IN} pad and the negative terminal to the PGND pad. Connect the positive terminal of the electronic load to the V_{OUT} pad and the negative terminal to the nearest GND0 pad.
4) Verify that V_{OUT} is approximately 3.3V using the DMM.

Generic Isolated Power Supply

Figure 2 shows a generic isolated power-supply block diagram. It consists of a power stage, an isolated transformer, rectifier, secondary-side error amplifier, and optocoupler to provide a feedback for the primary side control. Isolated power supplies are different depending upon how the transformer is being used in them

Flyback Principle

A transformer in a flyback configuration acts differently than its usual operation of transformation of energy from primary to secondary. During a transformer's usual operation, both primary and secondary windings conduct together simultaneously to make the transfer of energy possible from primary to secondary. In a flyback configuration, the primary and secondary windings do not conduct simultaneously, and the transformer acts more like a coupled inductor. Note that in this document the following notations for the transformer turns ratio have been used:

$$K = \frac{N_P}{N_S}$$

$$k = \frac{N_S}{N_P}$$

This means a capital K for primary turns/secondary turns and a small k for secondary turns/primary turns.

Figure 3 shows a simple flyback topology that consists of a transformer whose primary winding is connected to the drain of a switching MOSFET. The source of the MOSFET is connected to ground. The secondary winding is connected to the output capacitor through a rectifier diode.

In this flyback configuration, the current flows into the primary winding during the on-time of the switching period and flows into the secondary winding during the off-time of the switching period.

During the on-time when the primary switch is closed, a current, IP, flows through the primary winding as shown in Figure 4. IP can be written as follows:

$$I_P(t) = \frac{1}{L_P}\int_0^t V_{IN}dt = \frac{1}{L_P}V_{IN}t$$

The Peak current magnitude of the primary current can be written as follows:

$$I_{P-P} = \frac{1}{L_P}\int_0^{t_{ON}} V_{IN}dt = \frac{1}{L_P}V_{IN}t_{ON}$$

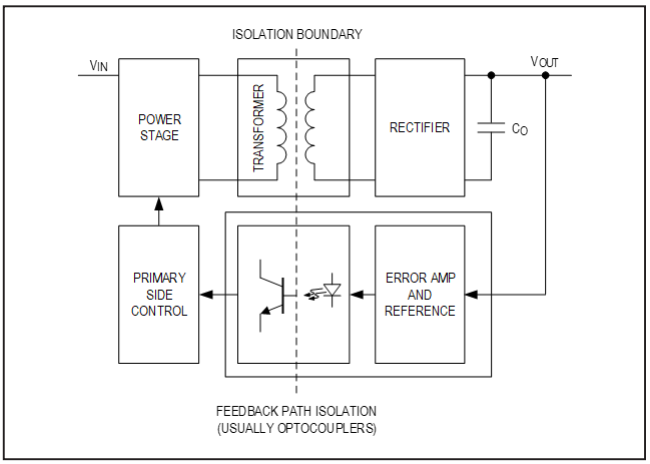

Figure 2. Generic isolated power supply.

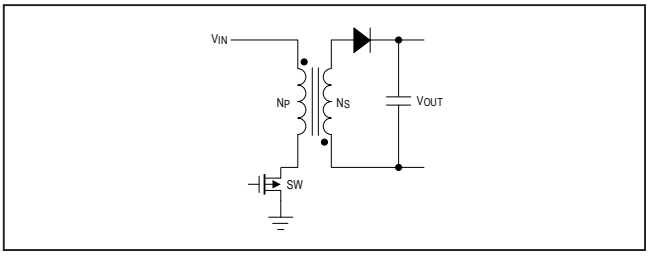

Figure 3. Simple flyback topology.

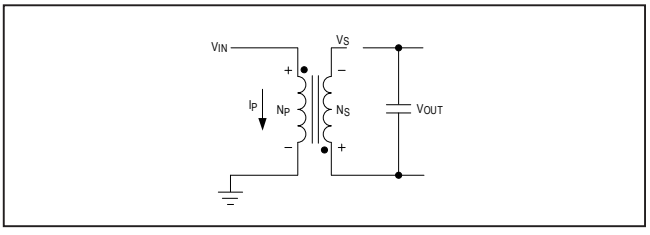

Figure 4. Flyback topology during on-time, t_{ON}.

In the secondary winding, a negative voltage is induced due to the current flowing into the primary winding. The rectifier diode is reverse-biased, and no current is flowing in the secondary windings. The induced voltage in the primary winding is written as follows:

$$V_S(t) = L_S \times \frac{dI_P(t)}{dt}$$

During the off-time when the primary switch opens as shown in Figure 5, the magnetic field in the primary winding collapses and the voltage at the winding reverses, while the current keeps flowing in the same direction until the field fades away.

The secondary current IS flows and the secondary rectifier diode is forward-biased. Output voltage (V_{OUT}) is now available across the secondary coil if the forward voltage drop of the rectifier diode is ignored. The secondary winding voltage is now flown away to primary side as K × V_{OUT}. This voltage is present across the switch until the current in the secondary winding decays to zero. The total voltage available across the switch during the off–time can be written as follows:

$$V_{SW} = V_{IN} + K \times V_{OUT}$$

This voltage also causes the breakdown of the magnetic flux in the primary winding (no current is flowing in the primary winding after this reset). Unlike a typical transformer action where the current flows in both the windings simultaneously, in a flyback transformer the current flows into the primary winding during the on-time and into the secondary winding during the off-time. This is why the term “coupled storage inductor” is used for transformers in the flyback operation, though it should be noted that mechanically these transformers are like any transformer. Use in flyback operations makes transformers act differently as coupled inductors. The required duty cycle for a given input voltage and output voltage can be calculated from:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}}$$

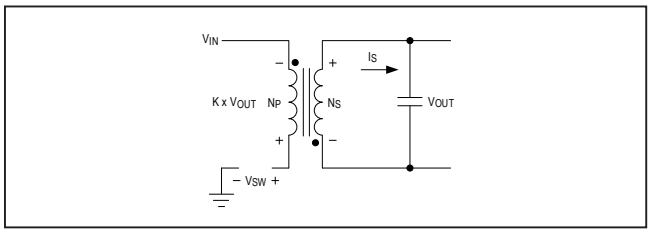

Figure 5. Flyback topology during off-time, t_{OFF}.

where:

$$V_{OUT} = (V_{OUT} + V_F) \times \frac{N_P}{N_S}$$

Figure 6 shows a typical continuous conduction mode (CCM) mode flyback primary and secondary winding current, and Figure 7 shows a typical DCM mode flyback topology waveform.

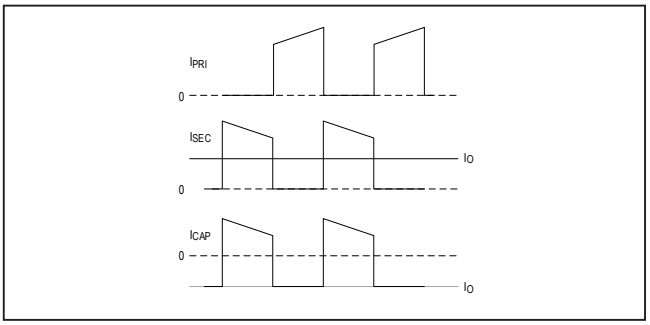

Figure 6. A typical CCM mode flyback primary and secondary winding current.

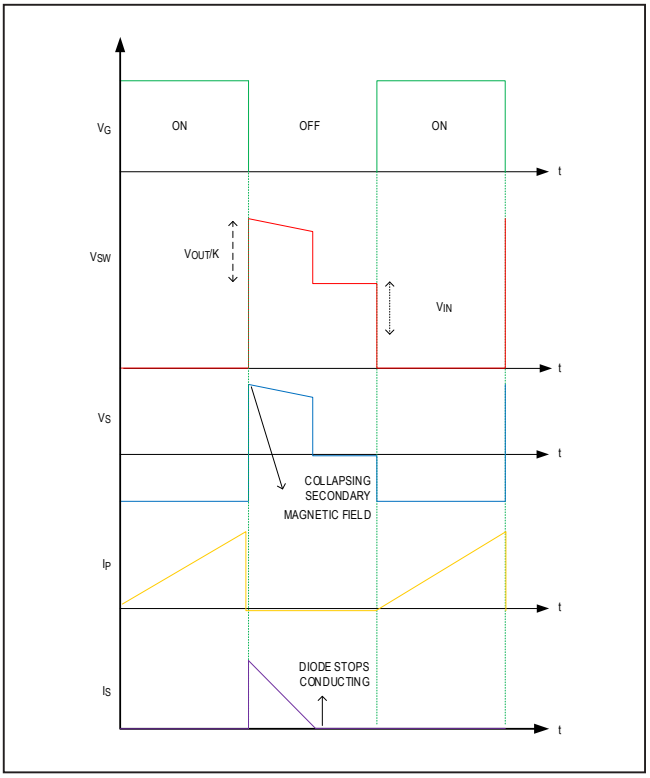

Figure 7. A typical DCM mode flyback topology waveform.

Design Procedure for DC-DC Flyback Using MAX17596

Now that the basic principle of the DCM flyback is understood, a practical design is illustrated. The design parameters are obtained by using expressions given in Application Note 5504: Designing Flyback Converters Using Peak-Current-Mode Controllers. This application note document is primarily concerned with the power stage and the feedback loop design and is intended to complement the information contained in the MAX17596 data sheet.

Flyback converters can be operated in DCM or CCM. The component choices, stress level in power devices, and controller design vary depending on the operating mode of the converter. The design discussed in this document is a DCM design and expressions for calculating component values and ratings are presented to achieve the design goals.

Step 1: Switching Frequency

For this design, a 100kHz switching frequency is selected. The MAX17596 switching frequency is programmable between 100kHz and 1000kHz with R6 resistor connected between the RT and SGND pins. The R6 resistor value is calculated as follows:

$$R_{RT} = \frac{10^{10}}{f_{sw}} \Omega$$

$$R_{RT} = \frac{10^{10}}{100k} = 100k\Omega$$

A standard 100kΩ resistor is selected for R6.

Step 2: Transformer Magnetizing Inductance and Turns Ratio

In a DCM flyback converter, the energy stored in the primary inductance of the flyback transformer is delivered entirely to the output. The maximum primary inductance value for which the converter remains in DCM in all operating conditions can be calculated as follows:

$$L_{PRI} = \frac{0.4 \times (V_{IN(MIN)} \times D_{MAX})^2}{(V_{OUT} + V_D) \times I_{OUT} \times f_{sw}}$$

where:

D_{MAX} = 0.49

V_D = 0.4 which is forward voltage drop of the selected rectifier diode

In this application, the DC input voltage varies from 10.5V DC to 17V DC. Substitute the values in the expression of LPRI as follows:

$$L_{PRI} = \frac{0.4 \times (16.171V \times 0.49)^2}{(3.3V + 0.4V) \times 0.5A \times 100kHz} = 80\mu H$$

For this design, LPRI is chosen as 80µH, LPRI = 80µH.

The leakage inductance of the transformer should be targeted as low as possible. For this design, a leakage inductance of 3.0µH, LLKG = 3.0µH is achieved. A customized transformer 750344517 from Würth Elektronik® is used in this design. This transformer also fulfills the specification of turns ratio and primary/secondary current requirement of the design that is calculated step by step in this document. The transformer has dielectric isolation specification of 4000 VAC.

Step 3: Maximum Duty-Cycle Calculation with Selected LPRI

Use the following expressions to calculate the maximum duty cycle of the converter for the selected frequency and magnetizing inductance:

$$D_{NEW} = \frac{\sqrt{2.5 \times L_{PRI} \times V_{OUT} \times I_{OUT} \times f_{sw}}}{V_{IN(MIN)}}$$

$$D_{NEW} = \frac{\sqrt{2.5 \times 80\mu H \times 3.3V \times 0.5A \times 100kHz}}{12.464V} = 0.49$$

Calculate the required transformer turns ratio (k) using the expressions as follows:

$$k = \frac{N_s}{N_p} = \frac{(V_{OUT} + V_D) \times (1 - D_{NEW})}{D_{NEW} \times V_{IN(MIN)}}$$

$$k = \frac{N_s}{N_p} = \frac{(3.3V + 0.4V) \times (1 - 0.49)}{0.49 \times 12.464V} = 0.309$$

For this design, k is chosen as 1:0.309.

Step 4: Calculation of Peak/RMS Current

The primary and secondary RMS and primary peak current calculation are needed to design the transformer in switched-mode power supplies. Also, the primary peak current is used in setting the current limit. Use the following expressions to calculate the primary and secondary peak and RMS currents:

$$I_{PRIPEAK} = \frac{V_{IN(MIN)} \times D_{NEW}}{L_{PRI} \times f_{sw}} = \frac{12.464V \times 0.49}{80\mu H \times 100kHz} = 0.757A$$

$$I_{PRIRMS} = I_{PRIPEAK} \times \sqrt{\frac{D_{NEW}}{3}}$$

$$I_{PRIRMS} = 0.757A \times \sqrt{\frac{0.49}{3}} = 0.306A$$

$$I_{SECPEAK} = \frac{I_{PRIPEAK}}{k} = \frac{0.757A}{0.309} = 2.451A$$

$$I_{SECRMS} = \sqrt{\frac{2 \times I_{OUT} \times I_{PRIPEAK}}{3 \times k}}$$

$$= \sqrt{\frac{2 \times 0.5A \times 0.757A}{3 \times 0.309}} = 0.904A$$

Step 5: Current-Limit Resistor Calculation

For the current-limit setting, the peak current can be calculated as follows:

$$I_{LIM} = 1.2 \times I_{PRIPEAK} = 1.2 \times 0.757A = 0.909A$$

The device includes a robust overcurrent protection scheme that protects the device under overload and short-circuit conditions. A current-sense resistor connected between the source of the MOSFET and the PGND pin sets the peak current limit. The current-limit comparator has a voltage trip level ($V_{CS-PEAK}$) of 300mV. Use the following equation to calculate the value of R11:

$$R_{CS} = \frac{300m}{I_{MOSFET}} = \frac{300m}{0.909A} = 0.33\Omega$$

where:

I_{MOSFET} is the peak current flowing through the MOSFET. A typical 330mΩ current-sense resistor is selected, R11= 330mΩ.

Step 6: MOSFET Selection

The MOSFET selection criteria include maximum drain voltage, peak/RMS current in the primary, and the maximum allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum VDS rating must be higher than the worst-case drain voltage as follows:

$$V_{DS(MAX)} = V_{IN(MAX)} + \left(\frac{2.5 \times (V_{OUT} + V_D)}{k}\right)$$

$$V_{DS(MAX)} = 17V + \left(\frac{2.5 \times (3.3V + 0.4V)}{0.309}\right) = 46.909V$$

For this application, the Diode Inc. DMN10H220LE 100V, 2.3A n-channel MOSFET is chosen as the primary MOSFET.

Step 7: Secondary Diode Selection

The maximum operating reverse voltage rating of the secondary rectifier diode must be higher than the sum of the output voltage and the reflected input voltage. The following expression is used to calculate the secondary diode voltage rating:

$$V_{SEC} = 1.25 \times \left(k \times V_{IN(MAX)} + V_{OUT}\right)$$

The ROHM Semiconductor RB051LAM-40 20V, 3A diode is selected as the secondary side rectifier diode.

$$V_{SEC} = 1.25 \times (0.309 \times 17V + 3.3V) = 10.69V$$

Step 8: Feedback Resistor Selection

A standard 15kΩ resistor is selected, R20 = 15 kΩ

$$R_U = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_B$$

where V_{REF} is the reference set by the secondary-side controller (V_{REF} = 1.24V for TLV431BSN1T1G is used in this design).

$$R_U = \left(\frac{3.3V}{1/24V} - 1\right) \times 15k\Omega = 24.9k\Omega$$

A standard 24.9kΩ resistor is selected, R19 = 24.9kΩ.

Step 9: Soft-Start Capacitor

The soft-start period for the devices can be programmed by selecting the value of the C6 capacitor connected from the SS pin to the SGND pin. Capacitor C6 is calculated as follows:

$$C_{SS} = 8.264 \times 0.33 \times t_{SS}$$

where t_{SS} is expressed in ms and the resultant value of C6 is in nF.

$$C_{SS} = 8.264 \times 0.33 \times 5 = 13.6nF$$

A standard 15nF is selected as the soft-start capacitor, C6 = 15nF.

Step 10: Input Capacitor Selection

For the flyback converter, the input capacitor supplies the input current when the diode rectifier is off. The voltage discharge on the input capacitor, due to the input average current, should be within the limits specified.

Assuming 25% ripple present on the input DC capacitor, the input capacitor can be calculated as follows:

$$C_{IN} = \frac{0.045 \times V_{OUT} \times I_{OUT}}{Eff \times 2 \times V_{ACMIN}^2}$$

$$C_{IN} = \frac{0.045 \times 3.3V \times 0.5A}{80\% \times 2 \times 10V^2} = 464\mu F$$

The input capacitor is selected as 1500µF.

Step 11: Output Capacitor Selection

The output capacitor is usually sized to support a step load of a certain percentage of the rated output current so that the output voltage deviation is contained to 1% of the rated output voltage. The output capacitance can be calculated by using the following expressions:

$$t_{RESPONSE} = \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, and f_C is the target closed-loop crossover frequency. In this application, f_C = 5kHz is selected.

$$t_{RESPONSE} = \left(\frac{0.33}{5kHz} + \frac{1}{100kHz}\right) = 76\mu s$$

$$C_{OUT} = \frac{0.25A \times 76\mu s}{0.33V} = 575\mu F$$

The 2 x 680µF electrolytic capacitors are selected for this design. Capacitor values change with the temperature and applied voltage. Refer to the capacitor data sheets to select capacitors that guarantee the required output capacitance across the operating range. For design calculations, use the worst-case derated value of capacitance based on the temperature range and applied voltage.

For the flyback converter, the output capacitor supplies the load current when the main switch is on, and therefore the output voltage ripple is a function and duty cycle of the load current. Use the following expression to estimate the output capacitor ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times \left[I_{PRIPEAK} - (k \times I_{OUT})\right]^2}{I_{PRIPEAK}^2 \times f_{SW} \times C_{OUT}}$$

$$\Delta V_{COUT} = \frac{0.5A \times \left[0.757A - (0.309 \times 0.5A)\right]^2}{0.757^2 \times 100kHz \times 1360\mu F} = 5.5mV$$

Step 12: Loop Compensation

Optocoupler feedback is used in isolated flyback converter designs for precise control of isolated output voltage. Figure 8 shows the overall scheme of the optocoupler feedback.

Use R15= 475Ω (typ) for an optocoupler transistor current of 1mA. Select R13 = 49.9kΩ and R14 = 22.1kΩ (typical values) to use the full range of available COMP voltage. The U3 is a low-voltage adjustable shunt regulator with a 1.24V reference voltage. In this design, an ON Semiconductor TLV431BSN1T1G 1.24V shunt regulator is selected.

Three controller configurations are suggested in *Application Note 5504: Designing Flyback Converters Using Peak-Current-Mode Controllers* based on open-loop gain and the R16 value. For typical designs, the current transfer ratio (CTR) of the optocoupler designs can be assumed to be unity. It is known that the comparator and gate-driver delays associated with the input voltage variations affect the optocoupler CTR. Depending on the optocoupler selected, variations in CTR causes wide variations in bandwidth of the closed-loop system across the input-voltage operating range. It is recommended to select an optocoupler with less CTR variations across the operating range.

For this board, configuration 2 is selected and the compensator values that are selected using the EE-Sim® tool are as follows:

- Resistor(R12) value is selected, R12 = 17.4kΩ
- Capacitor(C13) is selected, C13 = 12nF
- Capacitor(C12) is selected, C12 = 330pF
- Capacitor(C15) is selected, C15 = 0.01µF

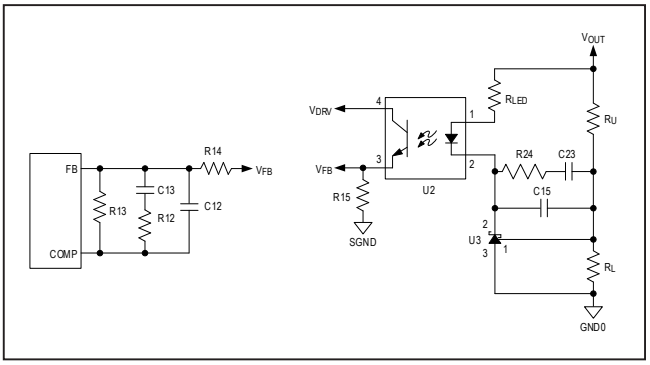

Figure 8. A typical optocoupler-based feedback compensation.

Step 13: EN/UVLO and OVI Setting

The device's EN/UVLO pin serves as an enable/disable input as well as an accurate programmable input UVLO pin. The device does not commence startup operation unless the EN/UVLO pin voltage exceeds 1.21V. The device turns off if the EN/UVLO pin voltage falls below 1.15V. A resistor-divider from the input DC bus to ground can be used to divide and apply a fraction of the input DC voltage (VDC) to the EN/UVLO pin. The values of the resistor-divider can be selected so the EN/UVLO pin voltage exceeds the 1.23V turn-on threshold at the desired input DC bus voltage. The same resistor-divider can be modified with an additional resistor (ROVI) to implement the input overvoltage protection in addition to the EN/UVLO functionality as shown in Figure 9.

When voltage at the OVI pin exceeds 1.21V, the device stops switching and resumes switching operations only if voltage at the OVI pin falls below 1.15V. For the given values of startup DC input voltage (V_{START}) and input overvoltage-protection voltage (V_{OVI}), the resistor values for the divider can be calculated as follows:

Select ROVI, R4 = 17.8kΩ

$$R_{EN} = R_{OVI} \times \left(\frac{V_{OVI}}{V_{START}} - 1 \right)$$

where V_{OVI} = maximum allowed overvoltage = 17.85V

$$R_{EN} = 17.9k\Omega \times \left(\frac{17.85V}{9.45V} - 1 \right) = 15.6k\Omega$$

A standard 16.2kΩ resistor (R_{EN}) is selected, R3 = 16.2kΩ.

$$R_{EN\_TOP} = \left[R_{OVI} + R_{EN} \right] \times \left[\frac{V_{START}}{1.21} - 1 \right]$$

$$R_{EN\_TOP} = \left[17.85k\Omega + 16.2k\Omega \right] \times \left[\frac{9.45V}{1.21} - 1 \right] = 231k\Omega$$

The same resistor-divider can be modified to implement input overvoltage protection. When the voltage at the OVI pin exceeds 1.215V (typ), the device stops switching. The device resumes switching operations only if the voltage at the OVI pin falls below 1.1V (typ).

A standard 226kΩ resistor (R_{EN_TOP}) is selected for R2.

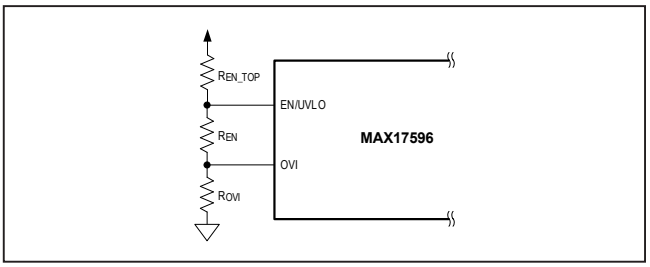

Figure 9. Programming EN/UVLO and OVI.

Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/20	Initial release	—