Miniature Universal Input 36W AC-DC Flyback Converter using the MAX17595

MAXREFDES1249

Introduction

Flyback converters are the preferred topology in the SMPS (switched-mode power supply) for medium- and low-power range applications because they are simple and economic. They have less components and are efficient in isolating the output from input. They are used in battery-powered applications, universal AC/DC converters, and industrial and telecommunication equipment. Isolated converters traditionally regulate the output voltage and current by utilizing a secondary side regulation (SSR) composed of an optocoupler and secondary error amplifier.

The MAXREFDES1249 is a universal input (86V to 305V AC) offline-isolated power supply that works across all geographical regions. It delivers 36W DC at 48V suitable for Power over Ethernet (PoE) and telecommunication applications.

The design uses a MAX17595 peak-current-mode controller operated in the discontinuous conduction mode (DCM) of the flyback topology. The architecture efficiently regulates the output by utilizing the feedback network and current-sense, and controlling the duty cycle of the switching MOSFET (metal-oxide semiconductor field-effect transistor) for compact and cost-effective power conversion. The MAX17595 has the following characteristics:

- Programmable frequency dithering for a low-EMI (electromagnetic interference) spread-spectrum operation
- Programmable switching frequency optimizes the magnetic and filter components for compact, cost-effective, and efficient isolated/non-isolated power supplies
- Isolation of 4000V AC between the primary and secondary sides
- EMI and EMC (electromagnetic compatibility) compliant design
- Programmable input enable/UVLO (undervoltage lockout) feature
- Programmable input overvoltage protection
- Adjustable soft-start
- Hiccup-mode, short-circuit protection
- Fast cycle-by-cycle peak current limit
- Thermal shutdown protection
- Space-saving, 16-pin, 3mm x 3mm TQFN (thin quad flat no-leads) package
- Operating temperature range of -40°C to +125°C

Hardware Specifications

The hardware is an offline DCM flyback converter using the MAX17595 for a 48V DC output application. The power supply delivers up to 750mA at 48V. Table 1 shows the design specification.

Table 1. Design Specifications

PARAMETER	SYMBOL	VALUE
Input Voltage	V_{IN}	86V AC to 305 V AC
Frequency	f_{SW}	125kHz
Maximum Efficiency	η	90%
Output Voltage	V_{OUT}	48V
Output Voltage ripple	ΔV_{OUT}	3%
Output Current	I_{OUT}	750mA
Output Power	P_{OUT}	36W

Designed–Built–Tested

This document describes the hardware in Figure 1. It is a detailed, systematic technical guide to design an isolated no-opto flyback DC-DC converter using Maxim's MAX17595 controller. The power supply was built and tested.

The Isolated Flyback Converter Topology

The isolated power supply, designed based on the flyback converter topology, uses the energy stored in the airgap in the core of the flyback transformer for efficient power conversion. Figure 2 is a simplified block diagram of the flyback topology. It has a controller, flyback transformer, and feedback circuit.

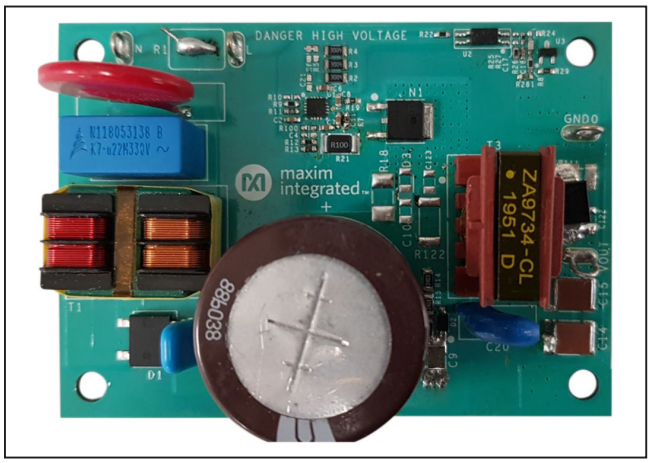

Figure 1a. MAXREFDES1249 hardware (top).

Figure 1b. MAXREFDES1249 hardware (bottom).

The flyback transformer primary winding dot convention is opposite to that in a magnetic coupling. The induced EMF in the secondary and auxiliary windings is opposite to the primary winding when the dot end of the primary end is connected to the ground. The respective rectifying diodes on the windings are reverse biased during the primary switch-on condition. The energy is stored in the transformer's air gap in the core. The flyback transformer sometimes requires two primary windings (primary and auxiliary/bias) for AC-DC conversions and high-voltage operations. The bias winding provides supply to the controller. The primary winding converts the high voltage.

The controller either adopts the voltage- or current-mode control to regulate the output voltage. A secondary-side rectifying diode or a synchronous MOSFET is used for an efficient flyback operation. The controller acquires information like the current-sense or feedback of the output voltage. It then drives the FET (field-effect transistor) with the required switching time (duty cycle). The energy stored in the primary is transferred to the secondary when the primary FET is off. The energy is drained into the output circuit.

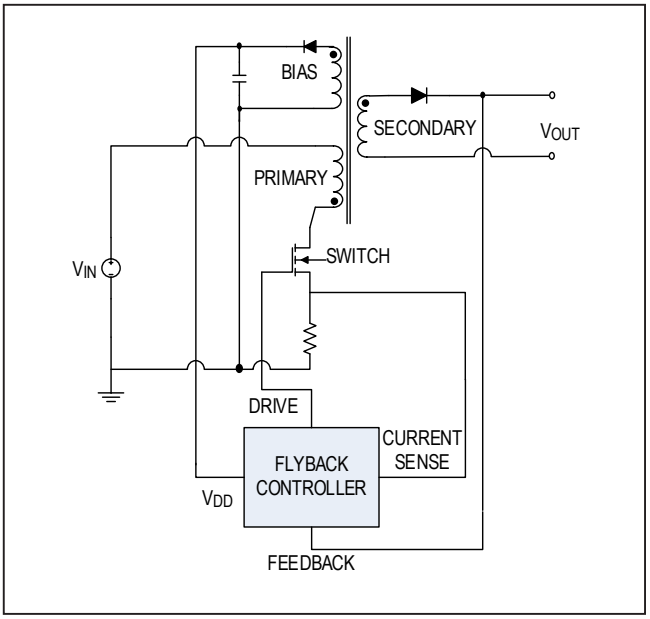

Figure 2. Block diagram of the flyback converter.

The Flyback Converter Operation

The flyback topology is referred to as a coupled inductor or buck-boost topology with a coupled inductor. The energy is stored here when the FET is on and decayed into the secondary when it is off. The energy builds across the primary winding when the primary FET turns on at a rate determined by the input voltage and primary magnetizing inductance (L_P) (Figure 3a). The current (I_{PRI}) flows from the input voltage source through the primary winding, magnetizing it, and storing the energy in the air gap. The dot convention of flyback transformers reverse biases the diodes of the secondary and/or auxiliary windings.

The energy transition occurs when the FET is off. The primary current transits to the secondary (I_S) (Figure 3b). A small amount of current flows for a short duration due to the leakage in the transformer's inductance, charging the FET's drain to source capacitance. The transformer's primary voltage starts increasing, and upon exceeding the input voltage, forward biases the secondary rectifying diode and clamps the voltage. This indicates a transfer of energy between the windings and transition of current from the primary to secondary.

Figure 3c depicts the flyback period where the secondary current (I_S) decays linearly. The voltage across the secondary winding is negative. The flyback voltage reflects across the drain to the source of the primary FET. The secondary current charges the capacitors to their respective potential and supplies the load. The leakage energy demagnetizes during this interval. All the energy stored in the transformer magnetizing winding transfers to the secondary in the discontinuous conduction mode (DCM) at the end of the flyback period. The secondary current decays to zero. All the energy does not transfer in the continuous conduction mode (CCM) as the primary current picks up before the secondary current decays to zero.

The resonance between the leakage energy of the magnetizing winding and parasitic capacitance at the switching node junction introduces ringing in the discontinuous conduction mode (DCM) at the end of the flyback interval. The output capacitors supply the load during this interval (Figure 3d).

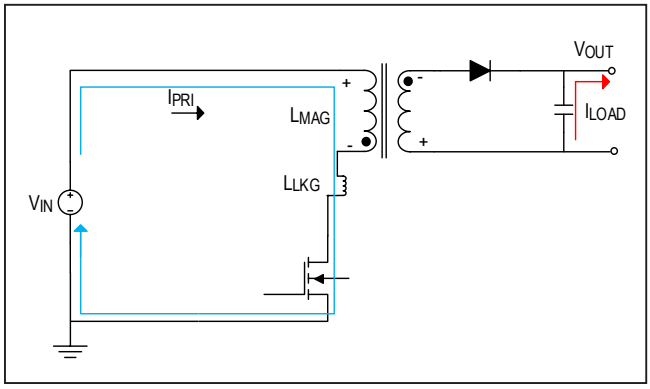

Figure 3a. Flyback converter operation when the primary FET is on.

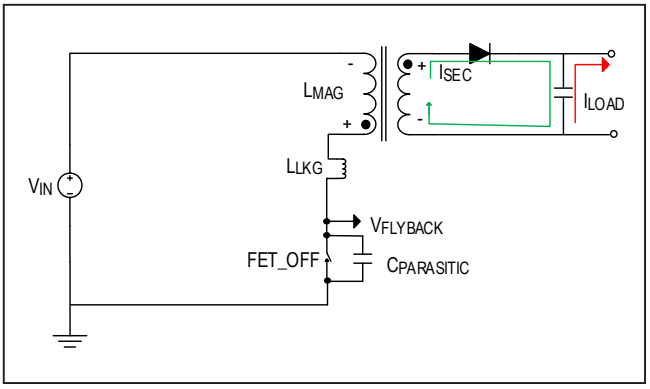

Figure 3c. Flyback converter operation during the secondary rectifier clamping and conduction interval (flyback interval).

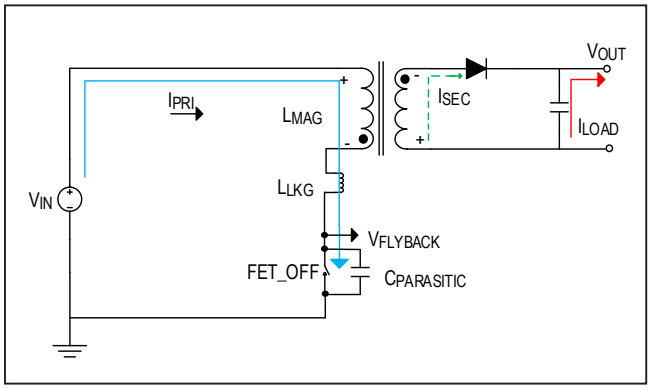

Figure 3b. Flyback converter operation when the primary FET is off.

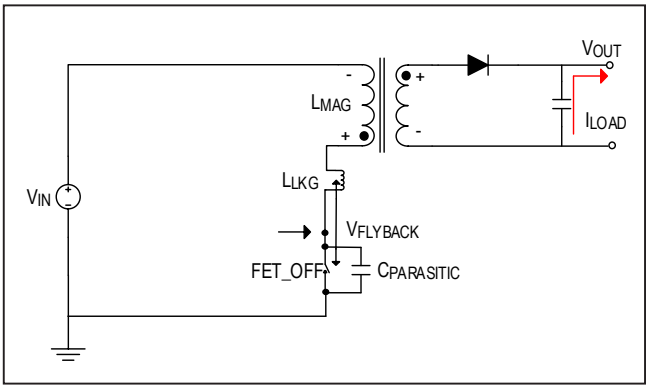

Figure 3d. Flyback converter operation during the DCM ringing interval.

Figure 4 shows the flyback DCM operation with the primary and secondary current. It also shows the voltage waveforms during one switching cycle of the primary FET. The primary current rises linearly when the FET is on. The primary current transits to the secondary when the FET is off. The current charges the parasitic capacitance due to leakage. The secondary current decays, feeding the output capacitor and load. Once the secondary current totally discharges, the magnetizing inductance rings with parasitic capacitance before the flyback voltage reaches zero.

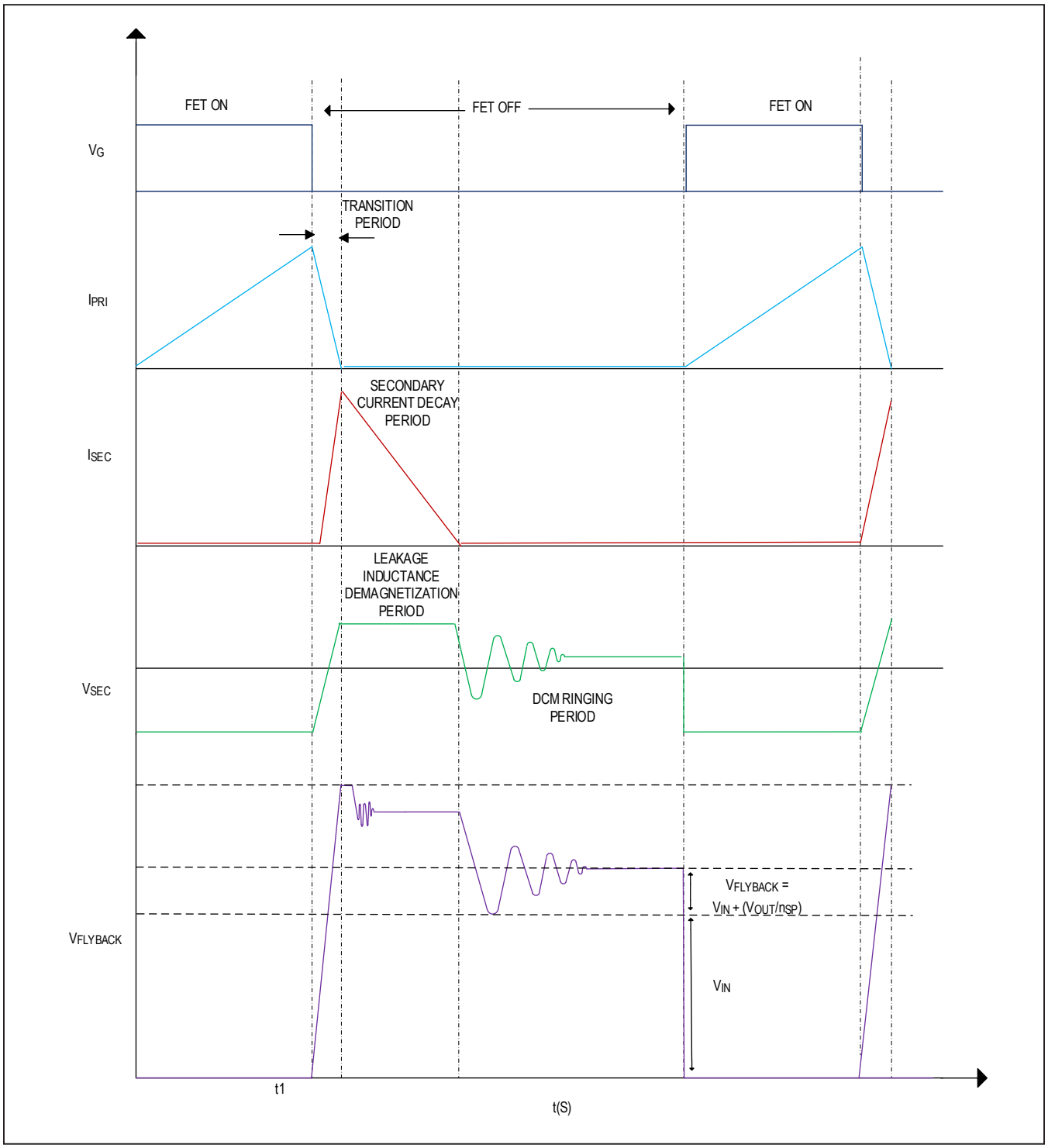

Figure 4. Typical current and voltage waveforms in the DCM during the flyback converter operation.

Design Procedure for the Offline Flyback Using the MAX17595

The basic principle of the flyback converter topology is understood now. The next step is to implement the principles of the design of a DCM flyback converter using the MAX17595, a peak-current-mode controller. Further in line are the implementation of the power stage, feedback network, and control loop. The respective sections also show how to calculate the component value, select the component, and other recommendations. This document complements the information in the *MAX17595 data sheet*. The following design parameters are used throughout this document:

Table 2. Design Parameters

PARAMETER	VALUE
AC Minimum Input Voltage	VAC_{INMIN}
AC Nominal Input Voltage	VAC_{INNOM}
AC Maximum Input Voltage	VAC_{INMAX}
DC Minimum Input Voltage	V_{INMIN}
DC Nominal Input Voltage	V_{INNOM}
DC Maximum Input Voltage	V_{INMAX}
Switching Frequency	f_{SW}
Maximum Efficiency	η
Output Voltage	V_{OUT}
Output Voltage Ripple	ΔV_{OUT}
Output Current	I_{OUT}
Output Power	P_{OUT}
Secondary-Primary Turns Ratio	n_{SP}
Duty Cycle	D

The MAX17595 can operate up to 125°C. Calculate the minimum number of turns required for the flyback transformer under a complex operating point of design, i.e., at a minimum input voltage.

Table 3. Predesign Specifications and Requirements (Some Quantities Required in the Later Parts of the Design)

FUNCTION	VALUE	DESCRIPTION
DC Minimum Input Voltage (VIN_{MIN})	121V	$VAC_{MIN} \times \sqrt{2}$
DC Nominal Input Voltage (VIN_{NOM})	311V	$VAC_{NOM} \times \sqrt{2}$
DC Maximum Input Voltage (VIN_{MAX})	432V	$VAC_{MAX} \times \sqrt{2}$
Line Frequency	50Hz to 60Hz	90%

Step 1. Calculating the Minimum Turns Ratio for the Flyback Converter

The flyback DC gain function relates the secondary-primary turns ratio (n_{SP}) and duty cycle (D) as:

$$n_{SP} = \frac{V_{OUT}}{V_{IN}} \times \left(\frac{1 - D}{D}\right)$$

The maximum duty cycle occurs when operating at a minimum input voltage delivering full load current. The transformer is designed based on factors like insulation type, pollution degree, safety characteristics, and insulation between the primary and secondary sides. The safety characteristics for the Maxim design are Class II EN62368-1 compliance, pollution degree II, and an isolation of $4KV_{RMS}$ between the primary and secondary.

The transformer, designed for high efficiency, must equally optimize the total power loss between the core and copper. The flyback transformer, secondary rectifier, primary switching MOSFET, and snubber circuit are the major components causing power loss in a flyback converter. The transformer must account for approximately 50% of the total power loss based on the predefined efficiency values. This factor optimizes the thermal management inside the transformer. It ensures the durability and stability of the overall design. The board is designed to support 60% of the full load at 80°C. The typical value of duty cycle for the MAX17595 is 48%, and allowing some margin, the recommended maximum limit is 43%. This ensures safe operation of the circuit. The minimum input voltage level to turn the circuit functionality on is set using the resistive divider circuit at the Undervoltage Lockout (UVLO) pin input of the MAX17595.

The IEEE519 recommends a ripple of 5% to 10% of the maximum input AC voltage. Select a 6.5% ripple (20V AC), which gives a UVLO value of 65V AC (90V DC). This value is the minimum value of input supply voltage to turn the circuit on and activate the functionality. Estimate the n_{SP} minimum with a D_{MAX} value of 43% and V_{IN} of 90V:

$$n_{SPMIN} = \frac{48}{90} \times \left(\frac{1 - 0.43}{0.43}\right)$$

$$n_{SPMIN} = 0.707$$

Step 2. Selecting the Switching Frequency

Selecting the switching frequency requires several considerations and trade-offs. The board design is a primary factor. A board designed for high efficiency and small size is expensive. It requires higher switching frequencies, special grades of transformers, and complex thermal management. Higher switching frequencies of more than 200kHz lead to electromagnetic interference and harmonics. A soft ferrite core with a standard switching frequency is a market-suitable and commonly available design.

It is economical and the usual choice unless there are special requirements. Select a frequency lower than 150kHz as it is the starting point of EMI conduction.

A switching frequency (f_{SW}) of 125kHz with frequency dithering reduces EMI issues. It is a trade-off between efficiency and cost.

Step 3. Estimating the Primary Magnetizing Inductance

PARAMETER	VALUE
Maximum Input Power	$P_{IN(MAX)}$
Maximum Output Power	$P_{OUT(MAX)}$
Switching Frequency	f_{SW}
Maximum Efficiency	η_{MAX}
Switching Period ($1/f_{SW}$)	t_{ON}

The energy stored in the primary magnetizing inductance (L_P) when the MOSFET is on gets transferred to the output when the MOSFET is off.

$$P_{IN(MAX)} = \frac{P_{OUT(MAX)}}{\eta_{MAX}} = \left(\frac{V_{OUT} \times I_{OUT}}{\eta_{MAX}}\right)$$

The current flows through the primary winding when the MOSFET is on, magnetizing it. The current is:

$$V_{IN} = L_P \times \frac{\Delta I_P}{\Delta \tau}$$

$$I_P(t) = \frac{1}{L_P}\int_0^t V_{IN}\, d\tau = \frac{1}{L_P} V_{IN}\, t$$

The peak magnitude of the primary current at the maximum duty cycle and minimum input voltage is:

$$I_{PRIPEAK} = \frac{1}{L_P}\int_0^t V_{IN}\, d\tau = \frac{1}{L_P} V_{IN(MIN)}\, t_{ON(MAX)}$$

The energy stored in the primary inductance when the MOSFET is on:

$$E_{IN(MAX)} = \frac{1}{2} \times L_P \times I_{PRIPEAK(MAX)}^2$$

$$E_{IN(MAX)} = \frac{1}{2} \times L_P \times \left(\frac{1}{L_P} V_{IN(MIN)} t_{ON}\right)^2$$

$$E_{IN(MAX)} = \frac{V_{IN(MIN)}^2 \times t_{ON(MAX)}^2}{2 \times L_P}$$

Maximum energy gets transferred and power is delivered to the output in one switching cycle:

$$E_{IN(MAX)} = P_{OUT(MAX)} \times \tau_{SW} = \left(\frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times f_{SW}}\right)$$

Substituting and equating the above equations of energy:

$$\frac{V_{IN(MIN)}^2 \times t_{ON(MAX)}^2}{2 \times L_P} = \left(\frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times f_{SW}}\right)$$

Rearranging the above equation, the inductance is:

$$L_P = \frac{\eta_{MAX} \times V_{IN(MIN)}^2 \times D_{(MAX)}^2}{2 \times V_{OUT} \times I_{OUT} \times f_{SW}}$$

The minimum inductance is estimated at a typical efficiency of 85%. The output voltage must also consider the drop across the rectifier diode on the secondary side.

$$L_P \le \frac{0.4 \times V_{IN(MIN)}^2 \times D_{(MAX)}^2}{(V_{OUT} + V_D) \times I_{OUT} \times f_{SW}}$$

The DC bus voltage varies from 121.6V DC to 431.3V DC. However, the actual minimum input operating voltage depends on the 100Hz ripple present on the DC bus capacitor. The ripple in this application is assumed as 30V DC. Hence, the minimum DC input to the converter is 90V, $V_{IN(MIN)}$ = 91V, D_{MAX} = 0.43, V_{OUT} = 48V, I_{OUT} = 750mA, V_D = 0.8V, f_{SW} = 125kHz because of frequency dithering and a dither of 5%. The inductance value L_P = 134µH. Assuming ±15% tolerance for the primary magnetizing inductance:

$$L_P = 114\mu H \pm 10\%$$

The leakage inductance of the transformer must be designed for the minimum. A good estimate for flyback designs is 1% to 3%. So, a transformer must be designed with L_P = 114µH ±10% and L_{LKG} = 1µH ±10%.

E or E-derived cores are generally preferred for these designs because of low-leakage inductance. Other core configurations like RM (rectangular mode) or PQ cores cause higher leakages, leading to narrower and thicker windings. The peak flux density equals maximum flux density swing due to standard switching frequencies, i.e., the power loss inside the transformer is mostly located in the windings. Ferrite cores saturate above 0.3T. So, choose a peak flux density of 0.25T.

Consult transformer manufacturers for standard transformer design values like area window product, saturation current limit, air-gap length, etc. Select a standard transformer after comparing the values from various manufacturers. The isolation between the primary and secondary must be 4000V AC. The clearance must be around 7mm to achieve this isolation.

The next section of configuring the MAX17595 shows how to implement the bias-winding configuration required to power up the IC with high voltages. The turns ratio and other components around it are described after the *configuration* section.

Step 4. Estimating the New Duty Cycle Based on the Calculated Inductance (L_P)

Rearranging the LP equation, the value for duty cycle is:

$$D_{MAX} = \frac{\sqrt{2.5 \times L_P \times V_{OUT} \times I_{OUT} \times f_{SW}}}{V_{IN(MIN)}}$$

Substituting the respective values, D_{MAX} = 0.392. Reestimating the turns ratio based on the new value of the duty cycle:

$$n_{SP} = \frac{(V_{OUT} + V_{OUT}) \times (1 - D_{NEW})}{V_{IN(MIN)} \times D_{NEW}}$$

Thus, n_{SP} = 0.83.

Select a transformer with a turns ratio of 0.875.

Step 5. Calculating the Peak and RMS Currents

The peak and RMS (root mean square) currents in the primary and secondary currents of the primary and secondary sides are:

$$I_{PRIPEAK} = \frac{V_{IN(MIN)} \times D_{NEW}}{L_P \times f_{SW}}$$

$$I_{PRIRMS} = I_{PRIPEAK} \times \sqrt{\frac{D_{NEW}}{3}}$$

$$I_{SECPEAK} = \frac{I_{PRIPEAK}}{n_{SP}}$$

$$I_{SECRMS} = \sqrt{\frac{2 \times I_{OUT} \times I_{PRIPEAK}}{3 \times n_{SP}}}$$

Substituting the respective values in the above equations, the values for current are:

Table 4. Current Values

PARAMETER	SYMBOL	VALUE
Primary Peak Current	$I_{PRIPEAK}$	2.516A
Primary RMS Current	I_{PRIRMS}	0.909A
Secondary Peak Current	$I_{SECPEAK}$	2.875A
Secondary RMS Current	I_{SECRMS}	1.19A
Primary Magnetizing Inductance	L_P	114µH
Turn Ratio (n_S/n_P)	n_{SP}	0.875
New Duty Cycle	D_{NEW}	0.395

Step 6. Selecting the MOSFET

Selecting the MOSFET(N1) is crucial in the flyback converter design. The peak-current rating, drain-source voltage rating, gate threshold, and thermal stress are the selection parameters.

The MOSFET is in series with the L_P. It experiences the same peak and RMS currents. Hence, it must be rated at least two times the primary peak current. The MOSFET experiences voltage stress during the turn-off period (flyback voltage). It must be able to withstand the voltage. The voltage value for which the MOSFET must be rated is:

$$V_{N1(MAX)} = V_{IN(MAX)} + \left(\frac{2.5 \times (V_{OUT} + V_D)}{n_{SP}} \right)$$

Here, $V_{IN(MAX)}$ is the maximum voltage rating of the MOSFET and V_D is the drop across the secondary rectifier diode during a reverse bias. Substituting the values, V_{INMAX} = 432V, V_{OUT} = 48V, V_D = 0.9V, n_{SP} = 0.875, the required voltage rating of the MOSFET N1, and V_{DSMAX} = 571V.

Infineon®'s IPD70R600P7S is a good MOSFET choice for this design. The selected MOSFET gate threshold satisfies the drive voltage of MAX17595 (V_{DRV} = 7V typ) and has optimized thermal characteristics.

The power loss in N1 is:

$$P_{TOT} = P_{CON} + P_{CDS} + P_{SW} + P_{GDRV}$$

P_{CON} is the conduction loss due to the current I_{PRIRMS} flowing through the drain source on the resistance of the MOSFET. Source the value of $R_{DS(ON)}$ from the MOSFET data sheet (R_{DS} = 0.49Ω):

$$P_{CON} = I_{(PEAKRMS)}^2 \times R_{DS(ON)} \approx 400mW$$

P_{SW} is the loss due to switching the MOSFET. It is the function of the load current and switching frequency. Source the drive current from the MAX17595 data sheet (I_{DRIVE} = 0.9A). Source the value of the gate to drive the charge Q_{GS} (1.6nC) and gate to source charge Q_{GD} (3.7nC) from the MOSFET data sheet:

$$P_{SW} = \left(\frac{V_{DSMAX} \times I_{OUT}}{2} \right) \left(\frac{f_{SW} \times (Q_{GS} + Q_{GD})}{I_{DRIVE}} \right) \approx 158mW$$

P_{DRV} is the gate drive loss to charge the total gate capacitance. A lower value reduces power loss and produces a faster switching time but contributes to the parasitic turn on of the secondary MOSFET. The power loss is (Q_{GT} = 10.5nC and V_{DRV} = 7.4V):

$$P_{GDRV} = Q_{GT} \times f_{SW} \times V_{DRV} \approx 9mW$$

P_{COSS} is the power to charge the output drain source capacitance of the MOSFET (C_{OSS} = 7pF):

$$P_{COSS} = \frac{1}{2} \times f_{SW} \times C_{OSS} \times V_{DSMAX}^2 \approx 143mW$$

The total loss in the MOSFET is P_{TOT} = 715mW. The MOSFET must be properly optimized for thermal stress. Insert the MOSFET in the PCB area recommended in the data sheet for the best results.

Step 7. Selecting the Secondary Rectifier Diode (D4)

The secondary rectification diode plays a crucial role in the flyback converter operation. The recovery time is an important factor in determining the duty cycle of the MOSFET operation. Select a PN junction or Schottky diode when operating the flyback in the DCM mode. The latter has a fast recovery time and low voltage drop. The diode must balance the voltage drop and junction capacitance. The ringing due to the leakage inductance and capacitance can cause the diode to be in conduction for a longer time at minimum input voltages. It leads to thermal issues and high voltage spikes. The maximum stress experienced by the diode is:

$$V_{SECDIODE} = (n_{SP} \times V_{INMAX} + V_{OUT})$$

The diode is rated for proper voltage with a safety margin of 25% to 35% higher than the calculated value. The current rating of the diode is estimated as two to three times the output current. Space is allotted for an RC snubber across the diode in the Maxim design. An RC snubber can be inserted if the design experiences high ringing. The value of RC components is estimated based on measured ringing with an oscilloscope, inserting a known value of capacitance (pF) across the diode, and checking if the frequency of ringing doubled. The best capacitance gives two times the ringing frequency across the diode after several iterations. Choose the resistor value based on the required cut-off frequency as low values increase the power loss. Choose the snubbing resistor across the diode as:

$$R_{SNUBDIODE} = \frac{3 \times T_{RINGING}}{2 \times \pi \times f_c \times C_{SNUBDIODE}}$$

Select a Micro-Commercial Co® US5K 800V, 5A rectifying diode.

Step 8. Configuring the RCD Clamp Circuit

The leakage inductance spreading across the air-gap has switching current through it as the transformer is designed with an air-gap between the windings. The leakage energy created due to this tends to charge the output capacitance (C_{OSS}) of the MOSFET (N1) if the coupling factor selected for the windings is poor. The leakage energy has no outward path. The C_{OSS} shares the same voltage as that of the MOSFET. The rectifier circuit (diode or synchronous FET) on the secondary conducts the secondary current when this voltage exceeds the input voltage. The device fails to function when the surge voltage across the drain to source exceeds the maximum voltage limit of N1.

There are several techniques to prevent this occurrence and reduce the voltage spikes. One way is to add a suitable resistor, capacitor, and diode (RCD) snubber circuit across the transformer's primary winding. It absorbs the energy dissipated in the resistor. It is vital to estimate the component values properly to ensure the efficient and safe operation of the design. Figure 5a shows the RCD network. The values of RCD are:

The voltage at Node A is:

$$V_{NODEA} = V_{SNUB} + V_{IN}$$

The voltage of Node B when the rectifying diode starts conducting is:

$$V_{NODEB} = V_{IN} + \frac{V_{OUT} + V_D}{n_{SP}}$$

So, the voltage across the leakage inductor is:

$$V_{LLK} = L_{LK} \times \frac{\Delta I_{SN}}{\Delta t_{SN}} = (V_{NODEA}) - (V_{NODEB})$$

$$L_{LK} \times \frac{\Delta I_{SN}}{\Delta t_{SN}} = (V_{SNUB} + V_{IN}) - \left(V_{IN} + \frac{V_{OUT} + V_D}{n_{SP}}\right)$$

$$\Delta t_{SN} = \frac{L_{LK} \times \Delta I_{SN}}{V_{SNUB} - \left(\frac{V_{OUT} + V_D}{n_{SP}}\right)}$$

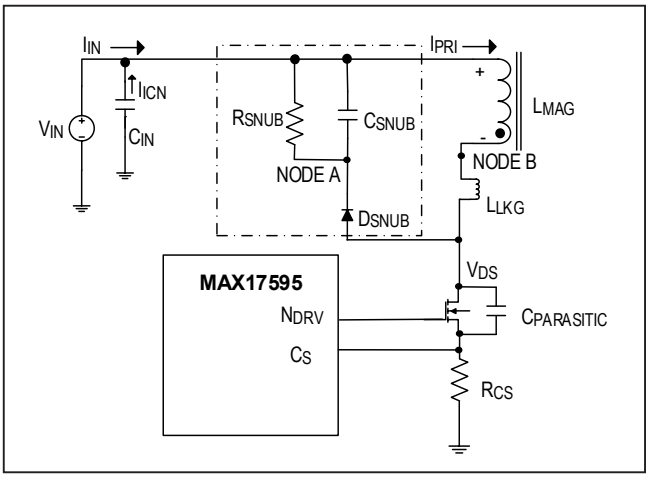

Figure 5a. The RCD snubber circuit.

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The stored leakage energy must be dissipated across the snubber network over one switching period. The balance between the maximum voltage must be allowed across MOSFET N1. The power dissipation across the resistor must be optimized. The average power dissipated in the snubber network is:

$$P_{SNUB} = V_{SNUB} \times \frac{\Delta I_{SN} \times \Delta t_{SN}}{2 \times \tau_{SW}}$$

$$P_{SNUB} = \frac{1}{2} \times V_{SNUB} \times \Delta I_{SN} \times f_{SW} \times \left(\frac{L_{LK} \times \Delta I_{SN}}{V_{SNUB} - \left(\frac{V_{OUT} + V_D}{n_{SP}} \right)} \right)$$

$$P_{SNUB} = \frac{1}{2} \times L_{LK} \times \Delta I_{SN}^{2} \times f_{SW} \times \left(\frac{V_{SNUB}}{V_{SNUB} - \left(\frac{V_{OUT} + V_D}{n_{SP}} \right)} \right)$$

Figure 5b shows V_{SNUB} as the voltage that appears on top of the maximum input voltage. The clamp voltage allowed on top of the flyback voltage must be under the safe operating region of the MOSFET. The snubbing voltage (V_{SNUB}) of around 2 to 2.5 times the reflected flyback voltage is a good estimate based on the safe margin of the MOSFET maximum voltage stress operation and other efficiency criteria (the snubber circuit is the power loss component) . Also, the clamp voltage that appears on top of the flyback voltage at the drain to source junction of the

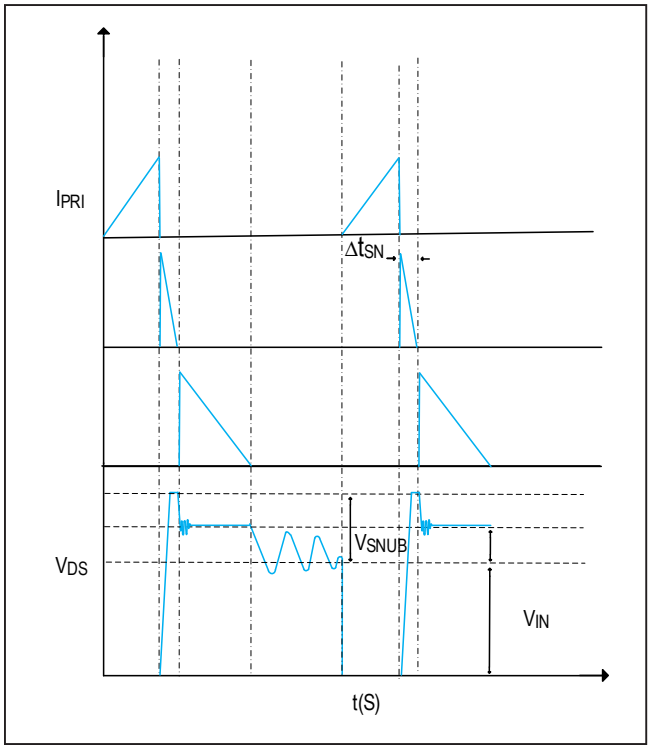

Figure 5b. The RCD snubber circuit waveform.

MOSFET must be around 1 to 1.5 times the reflected flyback voltage. The power dissipation must consider peak currents. Assuming $V_{SNUB} = 2.5$ (V_{OUT}/n_{SP}):

$$\frac{V_{SNUB}}{V_{SNUB} - \left(\frac{V_{OUT} + V_D}{n_{SP}} \right)} \approx 1.667$$

$$P_{SNUB} = 0.833 \times L_{LK} \times I_{PRIPEAK}^{2} \times f_{SW}$$

Estimate the value of the resistor from the power dissipation across the resistor:

$$P_{SNUB} = \frac{V_{SNUB}^{2}}{R_{SNUB}};$$

$$R_{SNUB} = \frac{V_{SNUB}^{2}}{P_{SNUB}}$$

The following expression is obtained when the V_{SNUB} value is 2.5 times the reflected voltage (V_{OUT}/n_{SP}). The drop across the rectifier diode compared to the square product value is negligible in the reflected voltage.

$$R_{SNUB} = \frac{\left(2.5 \times \left(\frac{V_{OUT}}{n_{SP}} \right) \right)^{2}}{P_{SNUB}}$$

$$R_{SNUB} = \frac{6.25 \times V_{OUT}^{2}}{n_{SP}^{2} \times P_{SNUB}}$$

The energy stored in the capacitor dissipates across the resistor. The average value of current in the capacitor over one switching period must almost be zero. The current charging the capacitor must flow into the resistor to discharge the capacitor.

$$\Delta I_{SN} = \frac{V_{SNUB}}{R_{SNUB}} = C_{SNUB} \times \frac{\Delta V_{SNUB}}{\tau_{SW}}$$

$$C_{SNUB} = \frac{V_{SNUB}}{\Delta V_{SNUB} \times R_{SNUB} \times f_{SW}}$$

$$C_{SNUB} = \frac{V_{SNUB}}{\Delta V_{SNUB}} \times \frac{1}{\left(\frac{6.25 \times V_{OUT}^{2}}{n_{SP}^{2} \times P_{SNUB}} \right) \times f_{SW}}$$

ΔV_{SNUB} is the ripple across the capacitor. The recommended value is around 5% to 15% of the V_{SNUB}. The capacitor values are estimated from the above equation after applying the suggested assumptions. The ripple is assumed to be around 7%. Rearranging the equation to obtain the capacitance value from the leakage inductance:

$$C_{SNUB} = \frac{14.285 \times n_{SP}^2 \times \left(0.833 \times L_{LK} \times I_{PRIPEAK}^2 \times f_{SW}\right)}{6.25 \times V_{OUT}^2 \times f_{SW}}$$

$$C_{SNUB} \approx \frac{2 \times n_{SP}^2 \times L_{LK} \times I_{PRIPEAK}^2}{V_{OUT}^2}$$

Applying the respective values in the following summarized equations, the values of the components become:

$$C_{SNUB} \approx \frac{2 \times n_{SP}^2 \times L_{LK} \times I_{PRIPEAK}^2}{V_{OUT}^2}$$

$$P_{SNUB} = 0.833 \times L_{LK} \times I_{PRIPEAK}^2 \times f_{SW}$$

$$R_{SNUB} = \frac{6.25 \times V_{OUT}^2}{n_{SP}^2 \times P_{SNUB}}$$

Consider the DC bias for the capacitor. Consider the power rating of the resistor value estimated from the above equations carefully when selecting the components.

Select the snubber diode rating (D3) properly as it experiences the same voltage stress as that of the MOSFET during a reverse bias. It must be of the same voltage rating as the MOSFET. It must have a very fast recovery time and must be rated for peak current.

Estimate the values based on the leakage and ringing across the MOSFET once the board is designed. The components of the snubber circuit are open in this design as the voltage stress across the MOSFET was under safe operating regions and the snubber circuit was not required.

Step 9. Selecting the Input Bulk (DC Link) Capacitor

Selecting the input DC capacitor is crucial in offline converter designs. The component and value selections play a major role in the efficiency, EMI, and proper operation of the converter. The input capacitor filters the low-frequency DC voltage and provides a smooth voltage to the circuit. The capacitor selection in AC/DC converter applications is based on the rectified line voltage ripple and holdup time (the time for which the capacitor supplies the current to the circuit when the AC supply is powered down).

The capacitor absorbs the high-frequency current. The pulsating current causes a voltage ripple across the capacitor (ΔV_{CIN}). The line current flowing through the capacitor charges and discharges at the line frequency. The average current across the input capacitor must be conserved. The DC link capacitor or bulk capacitor is:

$$I_{CIN} = C_{IN} \times \frac{\Delta V_{CIN}}{\Delta t}$$

$$I_{CIN[t_3 - t_2]} = C_{IN} \times \frac{\Delta V_{CIN}}{t_3 - t_2} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}}$$

$$C_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}} \times \frac{(t_3 - t_2)}{\Delta V_{CIN}}$$

The IEEE519 recommends a value of around 10% to 25% ripple of the maximum input voltage for rectifier applications. Choosing a very high value requires low capacitance but leads to a high duty cycle operation. Choosing a very low value requires a very bulky capacitor to support the application. This design does not implement the holdup time requirement. Figure 6 shows the waveform for the ripple for the line voltage. The capacitor must be able to support the input current requirement during the rectifier diode turn-off period and must regulate the input voltage. The charging period of the capacitor (t_2 - t_1) is estimated at around 10% to 20% of each cycle time period (t_4). It occurs twice over the line frequency.

Assuming 25% ripple and capacitor support time period (discharge time) of 0.85 times the time period (t4), during which the capacitor supports the input current requirement, the capacitor is:

$$t_{[t_3 - t_2]} = 0.85 \times T_4 = \frac{0.85}{2f_L} = \frac{0.85}{100} \approx 8.5\,ms$$

$$C_{IN} \geq \frac{P_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}} \times \frac{8.5m}{(25\%) \times V_{IN(MIN)}}$$

$$C_{IN} \geq \frac{0.034 \times P_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}^2}$$

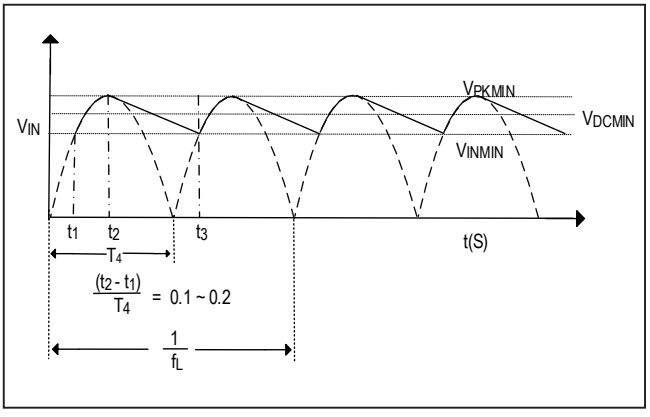

Figure 6. The input voltage waveform.

Some designs in the market use a generalized rule of 3µF/W for a 110V AC input and 0.8 µF/W for a 220V AC input, which means that a 3µF capacitance is used for every 1W of output power. Assuming 85% value of efficiency, V_{INMIN} = 121.6V, and P_{OUT} = 36W:

$$C_{IN} \geq \frac{0.034 \times P_{OUT}}{\eta_{MAX} \times V_{IN(MIN)}^2} \approx 97.4\mu F$$

$$I_{PRIRMS} = I_{PRIPEAK} \times \sqrt{\frac{D_{NEW}}{3}} \approx 0.909A$$

The capacitor is rated for at least 475V and the ESR (equivalent series resistance) must be low. The design is aimed at an ambient temperature of 80°C. Hence, the temperature of the selected capacitor is rated at 100°C. This design uses a 1µF 600V ceramic capacitor (C5) across the bulk capacitor to reduce the ESR of the capacitor set-up. The capacitor has a large diameter, but occupies less space compared to parallel capacitors.

C3 = C_{INSEL} = 120µF; 500V; 105°C

Step 10. Selecting the Output Capacitor

There are several methods to estimate the output capacitor. It is expressed in terms of either the support for a load-step response or the duty cycle of operation. High-frequency ripple current flows into the output capacitor, creating a ripple across the output capacitor. The selected capacitor is designed to support the load during the transient step response.

$$C_{OUT} = \frac{I_{STEP} \times \Delta t}{\Delta V_{OUT}}$$

The recharging time of the capacitor (Δt), also called the response time of the controller($\Delta t_{RESPONSE}$), is the time taken by the system to regulate the output. Select the capacitor charge and discharge bandwidth interval properly for a proper response from the overall system. The response time is the sum of 1/3rd of the crossover bandwidth interval and switching time period.

$$\Delta t_{RESPONSE} \cong \left(\frac{1}{3 \times f_C} + \frac{1}{f_{SW}} \right)$$

Select the crossover frequency (f_C) or open loop bandwidth at around 10% to 15% of the switching frequency. Assuming 10% for f_C, I_{STEP} of 50% of I_{OUT}, and ripple of 3 to 5% of V_{OUT}, the capacitance is:

$$\Delta t_{RESPONSE} \cong \left(\frac{1}{3 \times f_C} + \frac{1}{f_{SW}} \right) \cong \left(\frac{1}{3 \times 0.1 \times f_{SW}} + \frac{1}{f_{SW}} \right)$$

$$\Delta t_{RESPONSE} \cong 41\mu s$$

$$C_{OUT} \approx \frac{(50\% \times I_{OUT}) \times 41\mu}{3\% \times V_{OUT}} \approx 10.67\,\mu F$$

Select 10µF x 3 ceramic capacitors considering the derating and allowing a ripple of 300mV across the capacitor (0.6% to 1.5% of V_{OUT}). The bandwidth of the crossover frequency is altered based on the response time.

The capacitor must be able to withstand the ripple due to the high frequency current. It must be able to tolerate the RMS current that flows through it. The RMS requirement of the capacitor is:

$$I_{SEC} = I_{COUT} + I_{OUT}$$

$$I_{COUT(RMS)} = \sqrt{I_{SEC(RMS)}^2 - I_{OUT(RMS)}^2}$$

Thus,

$$I_{OUT(RMS)} = I_{OUT}$$

$$I_{SECRMS} = \sqrt{\frac{2 \times I_{OUT} \times I_{PRIPEAK}}{3 \times n_{SP}}}$$

Rearranging the equation of $I_{COUT(RMS)}$ with the respective values of the currents, the expression becomes:

$$I_{COUT(RMS)} = \sqrt{\frac{2 \times I_{OUT} \times I_{PRIPEAK}}{3 \times n_{SP}} - I_{OUT}^2}$$

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{2 \times I_{PRIPEAK}}{3 \times n_{SP} \times I_{OUT}} - 1}$$

Applying the respective values of variables in the equation:

$$I_{COUT(RMS)} = 0.935A_{RMS}$$

$$C_{OUT} = 3 \times 10\mu F; (C13, C14, C15)$$

Part II. Configuring the MAX17595 for the Design

The MAX17595 is a peak-current-mode controller use to design wide input voltage range flyback converters and boost regulators. The following sections show how to configure the MAX17595 for the design.

Step 11. Configuring the EN/ULVO and OVI Setting

The device incorporates a EN/UVLO pin as the enable/disable input on reaching a specified voltage. The device does not commence operation unless the EN/UVLO pin exceeds 1.21V. It turns off if the EN/UVLO falls below 1.15V. A resistive divider configuration is used to set the voltage threshold limits across the EN/UVLO pin to 1.23V. An additional resistance is added to limit the over voltage (OVI) to the circuit across the OVI pin. The device stops switching when the OVI pin exceeds 1.21V. It resumes operation when the voltage falls below 1.15V.

The startup voltage is V_{START} = 91V, V_{OVI} = 438V, and the R_{OVI} is 24.9kΩ.

$$R_{EN} = R_{OVI} \times \left(\frac{V_{OVI}}{V_{START}} - 1 \right)$$

$$R_{SUM} = \left[R_{OVI} + R_{EN} \right] \times \left(\frac{V_{START}}{1.21} - 1 \right)$$

Substituting the specified values:

$R_{OVI} = 24.9k\Omega$

Calculated values

$R_{EN} = 94.9k\Omega$;

$R_{SUM} = 8.9M\Omega$;

Selected values

$R2 = R3 = R4 = R_{SUM} = 3 \times 3M\Omega$;

$R_5 = R_{EN} = 95.3k\Omega$;

$R_6 = R_{OVI} = 24.9k\Omega$

Step 12. Configuring the Input Supply for the MAX17595 (V_{IN}, V_{DRV}, N_{DRV})

The MAX17595 accepts an input voltage range of 8V to 29V. The input is stepped down to a safe and optimal voltage range for the IC to function. A bias winding (auxiliary winding) is added to the flyback transformer to power the IC during the steady state. The transformer is not magnetized in the initial period. It takes time to magnetize the transformer's primary winding as the MOSFET is not in a conduction state. The transformer magnetizes accordingly when an alternate input supply to the IC starts the switching operation. A simple RC circuit is used to power the input voltage source for the IC to start from the UVLO threshold (20V typ).

Step 12a. Calculating the Turns Ratio (N_B = Bias Winding/Primary Turns)

The MAX17595 is implemented with a 20V V_{IN} UVLO wake-up level with a 13V hysteresis to optimize the size of the bias capacitor. The IC is bootstrapped through diode D2 to sustain the operation of the circuit (refer to the startup operation of the MAX17595 mentioned in the data sheet).

The bias winding powers the IC during the steady-state operation. Assuming the diode drop is V_{D2} = V_{D4} = 0.8V and bias voltage of 12V (V_{BIAS}) is supplied to the MAX17595 for safe operation, the bias winding (N_B) is:

$$n_b = n_{SP} \times \frac{V_{BIAS} + V_{D2}}{V_{OUT} + V_{D4}}$$

Thus, n_B = 0.26

The IC requires 2mA to 7mA of current during the steady-state operation. The bias winding is configured for 20mA of current.

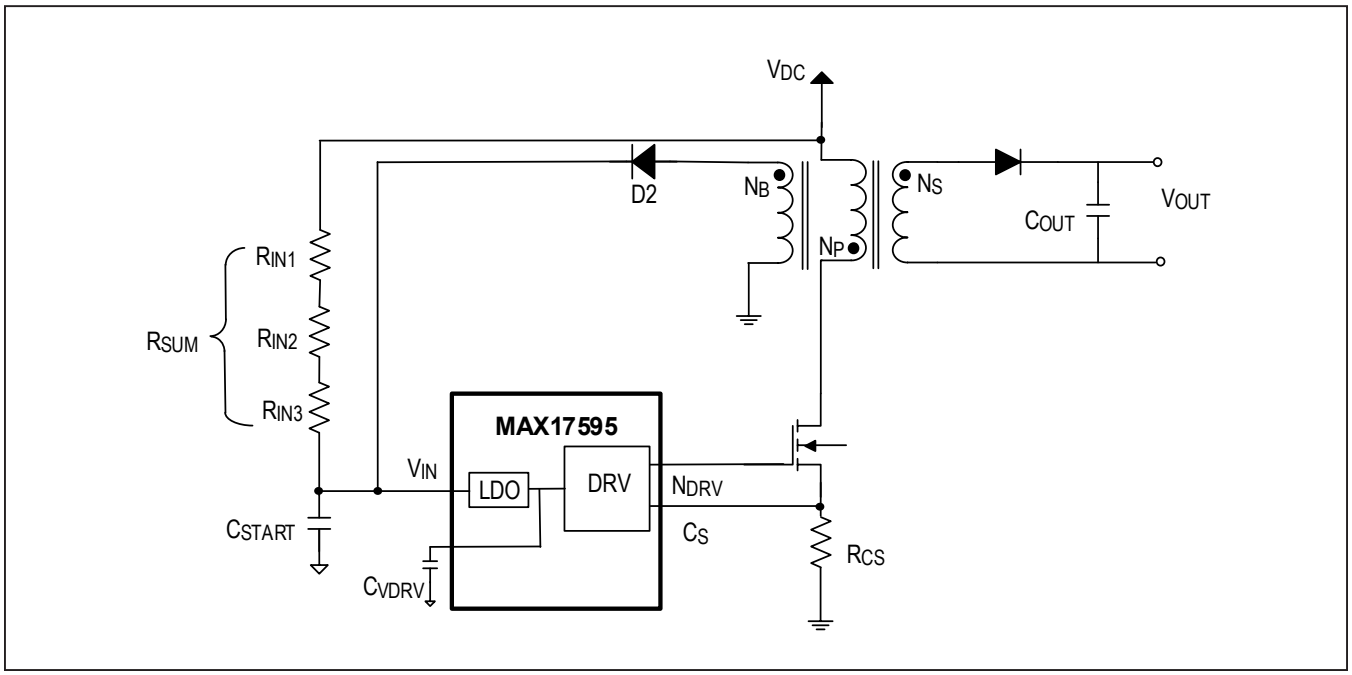

Figure 7. Input supply configuration for the ac/dc isolated design.

Step 12b. Estimating the RC Startup Circuit

The startup resistor (R_{START}) charges the startup capacitor (C_{START}) through the input DC voltage, increasing the voltage at the input pin (V_{IN}). The startup capacitor charges to a wake-up voltage. The MAX17595 draws 20µA through this capacitor and charges the drive capacitance to around a voltage of 7V typ to charge the gate capacitance of the MOSFET and start the switching operation. The startup capacitance and resistor values are:

$$C_{START} = 0.75 \times \left(\begin{array}{l} C_{VDRV} + I_{IN} \times t_{ss} \times 0.1 + \\ 0.04 \times \frac{t_{SS} \times Q_G \times f_{SW}}{10^6} \end{array} \right) \mu F$$

C_{VDRV} is the cumulative capacitance used at the drive pin (V_{DRV}) assuming 1µF, I_{IN} is the typical current consumption of the IC around 2mA, t_{SS} is the soft-start time assuming around 12ms (replace with suitable value after iterations on actual board, if required), Q_G is the total gate capacitance of the selected MOSFET. It is 10.5nC here.

$$C_{START} = 2.65\mu F$$

Select a 4.7µF capacitor, considering the DC biasing derating, as the capacitor value is crucial for the start-up operation (V_{START} = 91V).

$$C_9 = C_{START} = 4.7\,\mu F$$

$$R_{START} = \frac{(V_{START} - 10) \times 50}{1 + C_{START}} k\Omega$$

$$R_{START} = 3 \times 240\,k\Omega$$

$$R_{14} = R_{15} = R_{16} = 240k\Omega$$

R_{START} is configured as a 3 x 240kΩ resistor network so that the voltage is spread across the network. The N_{DRV} pin is generally connected with a low-value resistor in series to the gate of the MOSFET to limit the current into the gate.

Step 13. Configuring the Switching Frequency Resistor (R_{RT})

The resistor across the R_{RT} pin sets the switching frequency of the IC. Select a frequency of 125kHz for the application. The corresponding value of resistance is:

$$R_{RT} = \frac{10^{10}}{f_{SW}} \Omega$$

$$R_9 = R_{RT} = 80k\Omega$$

Step 14. Frequency Dithering for Spread-Spectrum Application for Low EMI (DITHER)

The switching frequency is dithered to reduce the EMI emissions. A current source at the DITHER/SYNC pin charges the C_{DITHER} capacitor to 50µA at 2V and discharges to 0.4V. The triangular ramp thus created must have the frequency (f_{TRI}) to 1kHz, calculated as:

$$f_{TRI} = \frac{50\mu A}{C_{DITHER} \times 3.2V}$$

The frequency of the triangular ramp is set close to 1kHz. The capacitor (C_{DITHER}) is connected from the DITHER/SYNC pin to the SGND.

$$C_{DITHER} = \frac{50\mu A}{f_{TRI} \times 3.2V}$$

$$C_2 = C_{DITHER} = 15nF$$

A resistor is connected from the R_{RT} pin to the DITHER/SYNC pin, which determines the amount of dither. Use 5% dithering as follows:

$$\%DITHER = \frac{R_{RT}}{R_{DITHER}}$$

The corresponding R_{DITHER} (R11) is 1.6MΩ.

Step 15. Estimating the Current-Sense Resistor (CS Pin)

The overcurrent protection scheme protects the circuit from overload and short circuit. A current-sense resistor is connected across the CS pin (source of the MOSFET and PGND), which sets or limits the peak current that flows through the MOSFET (I_{MOSFET}). The comparator that senses the voltage across the resistor has a trip level of ($V_{CS-PEAK}$) 300mV. The R_{CS} is:

$$R_{CS} = \frac{300mV}{I_{MOSFET}} \Omega$$

$$R_{21} = 120m\Omega$$

The device has a 65ns of leading-edge blanking time to ignore the leading-edge current spikes caused due to leakage and noise. An RC network is used to filter the noise. The corner frequency is set around 10 MHz to 20MHz.

Step 16. Programming the Soft-Start Time (SS)

The soft-start limits the inrush current. It protects the load and IC during high inrush current events. A capacitor (C_{SS}) at the soft-start pin is charged to a certain voltage during the soft-start period. This voltage is used by the error amplifier to ramp the output to its full potential at a rate determined by the soft-start period. Assume 12ms as the soft-start period. The corresponding soft-start capacitor is:

$$C_{SS} = 8.2645 \times t_{ss} nF$$

$$C_7 = C_{SS} = 100nF$$

Step 17. Decoupling the Capacitors

The DC-biasing decoupling capacitors must be placed across the V_{IN} and EN/UVLO pins of the MAX17595 to provide robust and accurate regulated voltage for controller operations. Ceramic capacitors are used because of low ESR. The capacitor across the V_{IN} pin must be rated for the same high voltage as that of the biasing capacitor. Place the capacitor of the DITHER and V_{IN} pin close to the IC (C21 = 470nF and C6 = 470nF).

Step 18. Programming the Feedback Network (R_U, R_B)

The output voltage is sampled and a fraction of it obtained through the feedback resistive divider network. The output voltage is fed to the feedback pin through an optocoupler. The IC controls the duty cycle of the MOSFET. The feedback network of the resistive divider along with the voltage reference is set using TLV431, which sets the reference voltage to 1.24V (V_{REF} = 1.24V).

The resistive divider is:

$$R_B = \frac{10 \times (30 \times C_{START} - 20 \times C_{DRV} - I_{IN} \times t_{SS})}{V_{OUT} \times C_{OUT} \times (I_{IN} + Q_G \times f_{SW})}$$

$$R_U = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_B$$

Applying the values of variables, C_{START} = 4.7µF, C_{DRV} = 1µF, I_{IN} = 2mA, t_{SS} = 12ms, V_{OUT} = 48V, C_{OUT} = 12.6 µF (DC bias), Q_G = 10.5nC, f_{SW} = 125kHz, and V_{REF} = 1.24V.

$$R_{29} = R_B = 475\Omega$$

$$R_8 = R_U = 18.2k\Omega$$

Part III. Control Loop and Compensation Design

Step 19. Programming the Optocoupler

The secondary side voltage is fed back to the primary side using an optocoupler and voltage reference network. The isolated signal is fed back to the primary side. It is used to control the primary side MOSFET and compensate for the error. The midband frequency, used to boost the gain and phase, is obtained through the R_{LED}, which controls the required amount of current to the optocoupler. The R_{LED} is:

$$R_{LED} = 400 \times CTR \times (V_{OUT} - 2.7)$$

The CTR (current transfer ratio) is the ratio of the forward current to collector current of the optocoupler and how efficiently it can translate the signal. A CTR ratio of 1 is assumed good and the optocoupler must be rated for isolation like the transformer (4kV). The RLED sets the current to the optocoupler. The selected value is:

$$R_{26} = R_{LED} = 18.12k\Omega$$

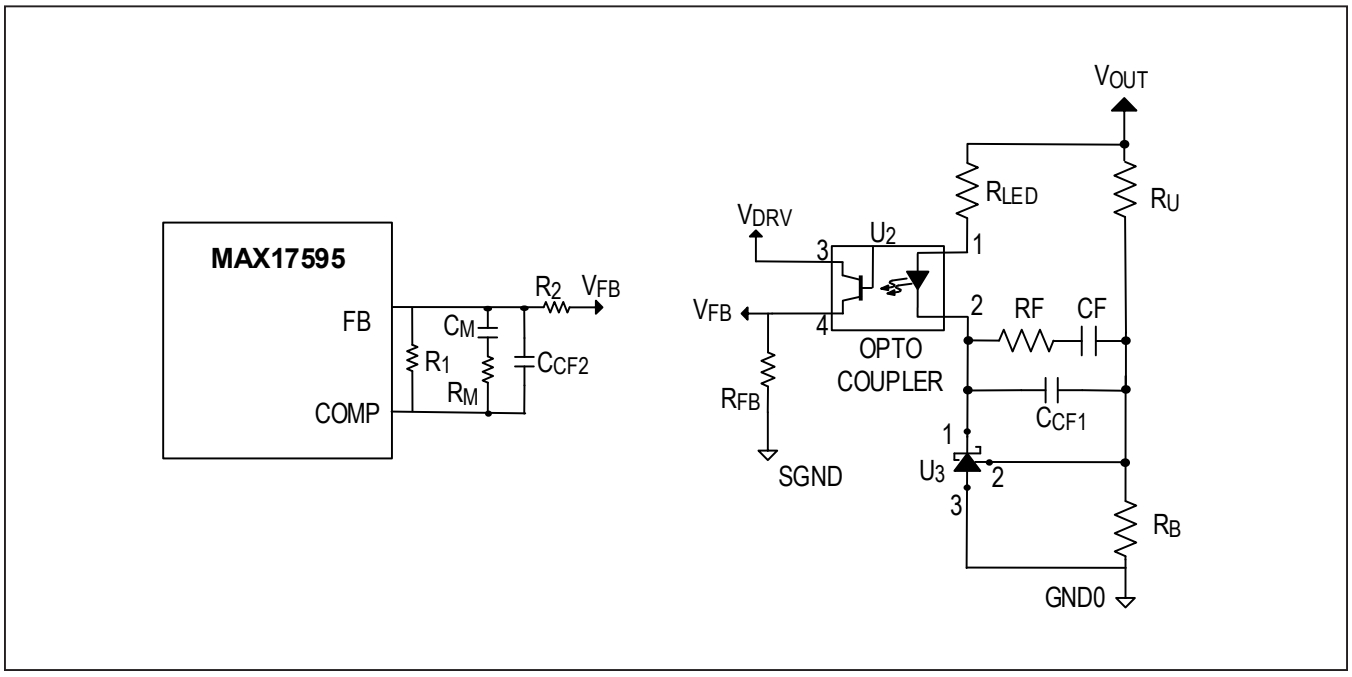

Figure 8. Optocoupler feedback for the isolated flyback designs.

Step 20. Programming the Closed Loop Feedback Network

The control loop design determines the transfer function of the error amplifier. Some margin is maintained at the crossover frequency so that the phase margin does not fall below 20° or 30°. A higher margin (60° or 75°) assumes good phase margin over all the load, line, and temperature changes. The optimum dynamic performance crossover frequency (f_C) must be 1/4th of the switching frequency. It can be close to 1/10th of the switching frequency when the optimum crossover is not concerned.

The output capacitance and load resistance contribute to a pole. The output capacitance and its corresponding ESR contributes to zero in the transfer function of the control loop. A pole is placed to suppress the effect of the zero and pole at their respective frequencies of operation. The pole frequency due to the output capacitance and load is:

$$f_P = \frac{1}{2x\,\pi x C_{OUT} x R_{LOAD}}$$

The capacitance must be able to tolerate the step response of the output (typically 50%). The ESR is selected as low as possible so that the dominant zero is not effective enough to cause damping.

$$f_P = \frac{I_{OUT}}{\pi x\, C_{OUT} x\, V_{OUT}} = 497.3Hz$$

Thus, f_P = 497.3Hz.

The plant transfer function comprising the output capacitor, load, and current sense amplifier gain is:

$$G_{PLANT} = \frac{f_p}{f_c} x \sqrt{\frac{L_{PRI} x f_{SW} x V_{OUT}}{8 * I_{OUT}}} x \frac{V_{IN}}{V_{IN} x R_{CS} + 50 x 10^{3} x L_{PRI}}$$

Applying the values and f_C = 10kHz in Step 9, the magnitude of the plant transfer function is:

$$G_{PLANT} = 4.156$$

The component values across the COMP and FB pin are R_1 = 49.9kΩ and R_2 = 22kΩ. The configuration loop gain of the setup is:

$$G_{PLANT} x CTR x \frac{R_{FB}}{R_{LED}} x \frac{R_1}{R_2} \approx 0.246$$

Refer to *Application Note AN5504 (Designing Flyback Converters Using Peak-Current-Mode Controllers)* for the three configurations in the secondary feedback implementation. Configuration 1 is used based on the value 0.246 < 0.8.

$$G_{PLANT} x CTR x \frac{R_{FB}}{R_{LED}} x \frac{R_1}{R_2} = 0.246 \le 0.8$$

$$R_F = \left(\frac{R_{LED} x R_2}{G_{PLANT} x CTR x R_{FB} x R_1} - 1 \right) x R_U\ \Omega$$

$$C_F = \left(\frac{1}{2\pi x (R_U + R_F) x f_P} \right) farad$$

$$C_F = \left(\frac{1}{\pi x f_{SW} x R_F} \right) farad$$

Applying the values, the components become:

$R_{27} = R_F$ = 64.9kΩ

$C_{17} = C_F$ = 5.6nF

$C_{18} = C_{CF1}$ = 43pF

Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/20	Initial release	—