Miniature 24W, 12V DC-DC Flyback Converter Using MAX17596

MAXREFDES1227

Introduction

The MAXREFDES1227 is a miniature 12V output isolated power supply that can deliver up to 2A load current. The design employs the MAX17596 peak-current-mode controller in discontinuous-conduction mode (DCM) flyback topology running at 125kHz. The input voltage range of MAX17596 is 4.5V to 36V; however, an extra bias winding from the transformer is used to power the controller. This allows an input operating voltage of up to 60V for this design.

The transformer provides a galvanic isolation of $1500V_{RMS}$ between the primary and the secondary. In addition, an optocoupler is used to provide secondary side feedback to the controller for voltage regulation while maintaining isolation. This document also discusses a step-by-step procedure that is used to implement this reference design. Design equations for the calculation of all the design parameters are presented. These equations show how the component values were calculated enabling users to modify this design for their applications. The key features are as follows:

- Miniature Design Optimized for Small Size
- 17V to 60V Input Range
- Isolated Output of 12V DC at 24W
- Cycle-by-Cycle Current Limit
- Resistor Programmable UVLO/OVI Threshold
- Low-Cost DCM Flyback Design
- Galvanic Isolation up to $1500V_{RMS}$
- Proven PCB Layout
- Fully Assembled and Tested

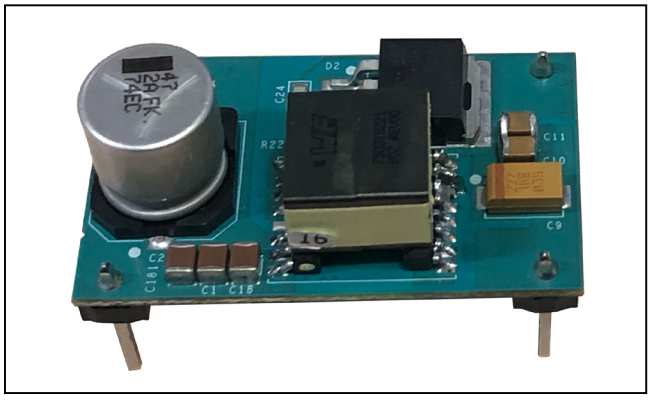

Figure 1. MAXREFDES1227 hardware – top.

Hardware Specification

A DC input DCM flyback converter using the MAX17596 is demonstrated for a 12V DC output application. The power supply delivers up to 2A at 12V. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	17V	60V
Frequency	f_{SW}	125kHz	
Maximum Efficiency	η	88.4%	
Output Voltage	V_{OUT}	12V	
Output Voltage Ripple	ΔV_{OUT}	1% of V_{OUT} max	
Output Current	I_{OUT}	0	2A
Output Power	P_{OUT}	24W	

Designed–Built–Tested

This document describes the hardware shown in Figure 1 and Figure 2. It provides a detailed systematic technical guide to designing a DC-DC DCM flyback using Maxim's MAX17596 current-mode controller. The power supply has been built and tested, details of which follow later in this document.

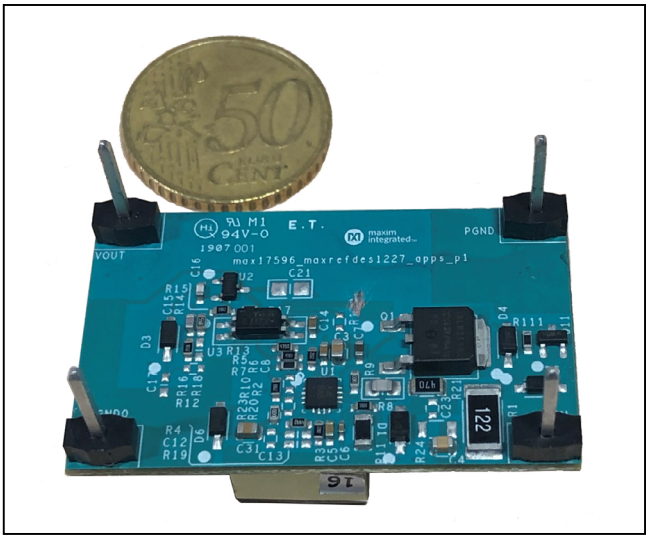

Figure 2. MAXREFDES1227 hardware – bottom.

Generic Isolated Power Supply

Figure 3 shows a generic isolated power-supply block diagram. It consists of a power stage, an isolation transformer, rectifier, secondary-side error amplifier, and opto-coupler to provide a feedback for the primary side control. Different isolated power supplies are different depending upon how the transformer is being used in them.

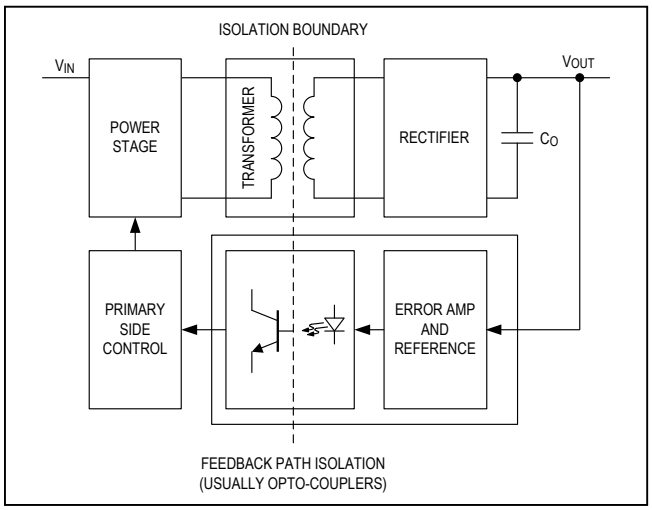

Figure 3. Generic isolated power supply.

Flyback Principle

A transformer in a flyback configuration acts differently than its usual operation of transformation of energy from primary to secondary. During a transformer's usual operation, both primary and secondary windings conduct together at the same time to make the transfer of energy possible from primary to secondary. In a flyback configuration, the primary and secondary windings do not conduct at the same time and the transformer acts more like a coupled inductor. Note that in this document we have used the following equations for the transformer turns ratio:

$$K = \frac{N_P}{N_S}$$

$$k = \frac{N_S}{N_P}$$

This means capital K represents primary turns/secondary turns and small k represents secondary turns/primary turns.

Figure 4 shows a simple flyback topology that consists of a transformer whose primary winding is connected to the drain of a switching MOSFET. The source of the MOSFET is connected to ground. The secondary winding is connected to the output capacitor through a rectifier diode. In this flyback configuration, the current flows into the primary winding during the on-time of the switching period and flows into the secondary winding during the off-time of the switching period.

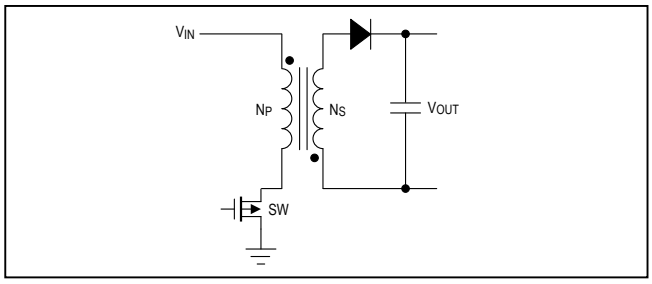

Figure 4. Simple flyback topology.

During the on-time when the primary switch is closed, a current, I_P, flows through the primary winding as shown in Figure 5.

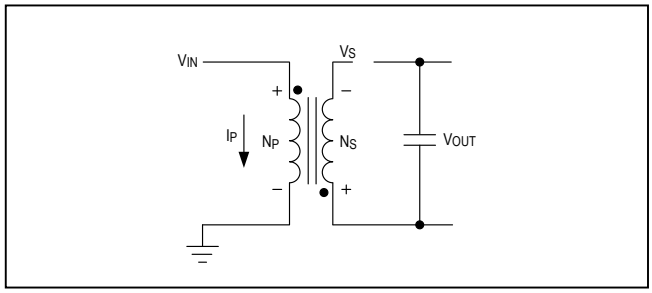

Figure 5. Flyback topology during on-time, t_{ON}.

I_P can be written as follows:

$$I_P(t) = \frac{1}{L_P}\int_0^t V_{IN}d\tau = \frac{1}{L_P}V_{IN}t$$

The peak magnitude of the primary current can be written as follows:

$$I_{P-P} = \frac{1}{L_P}\int_0^{t_{ON}} V_{IN}d\tau = \frac{1}{L_P}V_{IN}t_{ON}$$

In the secondary winding, a negative voltage is induced due to the current flowing in to the primary. The rectifier diode is reverse-biased and no current is flowing in the secondary winding. The induced voltage in the primary can be written as:

$$V_S(t) = L_S \times \frac{dI_P(t)}{dt}$$

During the off-time when the primary switch opens as shown in Figure 6, the magnetic field in the primary winding collapses and the voltage at the winding reverses, while current keeps flowing in the same direction until the field fades away.

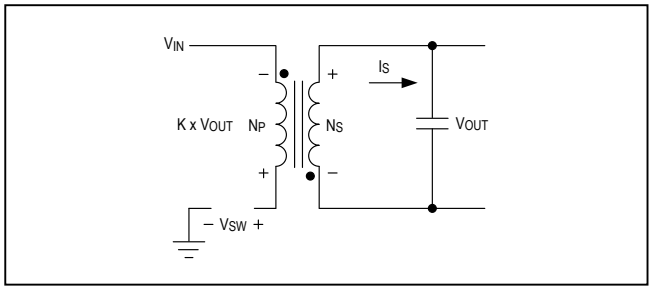

Figure 6. Flyback topology during off-time, t_{OFF}.

The secondary current, I_S, flows and the secondary and rectifier diode is forward-biased. Output voltage, V_{OUT}, is now available across the secondary coil if we ignore the forward-voltage drop of the rectifier diode. The secondary winding voltage is now flown away to primary side as K x V_{OUT}. This voltage is present across the switch until the current in the secondary winding decays to zero. Total voltage available across the switch during the off-time can be written as:

$$V_{SW} = V_{IN} + K \times V_{OUT}$$

This voltage also causes the breakdown of the magnetic flux in the primary winding (no current is flowing in the primary winding after this reset). Here we can see that, unlike a usual transformer action where current flows in both of the windings at the same time, in a flyback transformer the current flows into the primary winding during the on-time and into the secondary winding during the off-time. This is why we use the term “coupled storage inductor” for transformers used in flyback operation. It should be noted though that mechanically these transformers are like any transformer. Use in flyback operations makes transformers act differently as coupled inductors. The required duty cycle for a given input voltage and output voltage can be calculated from:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}}$$

where:

$$V_{OUT} = (V_{OUT} + V_F) \times \frac{N_P}{N_S}$$

Figure 7 shows a typical continuous-conduction mode (CCM) flyback primary and secondary winding current, and Figure 8 shows a typical DCM flyback waveform.

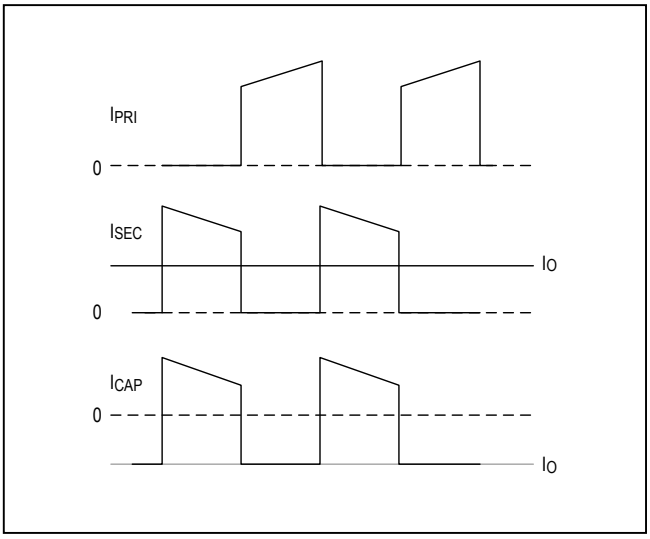

Figure 7. A typical CCM flyback primary and secondary winding current.

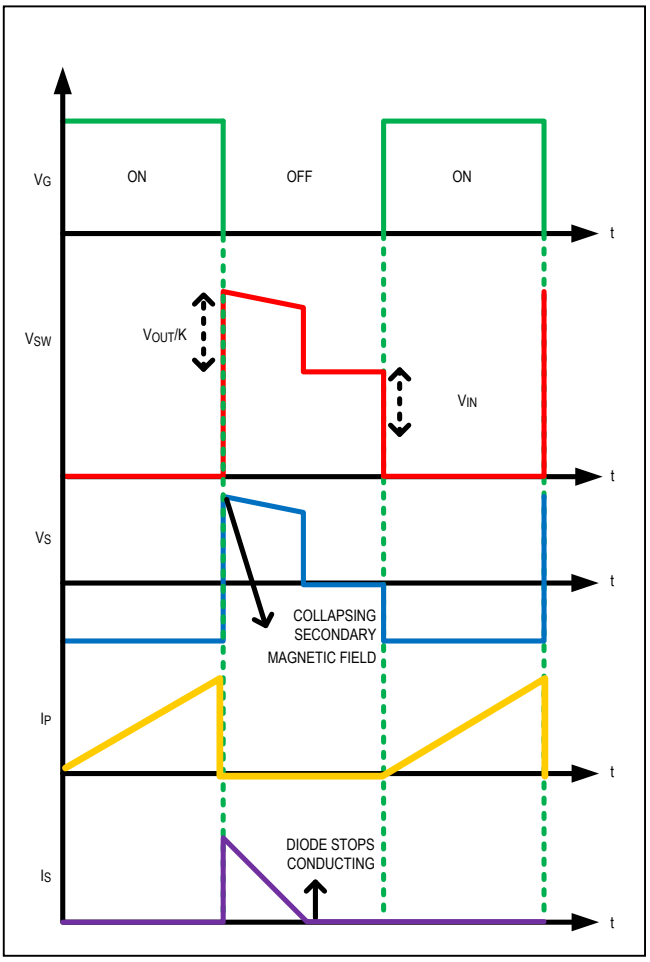

Figure 8. A typical DCM flyback topology waveform.

Design Procedure for DC-DC Flyback Using MAX17596

Now that the basic principle of the DCM flyback is understood, a practical design can be illustrated. The design parameters are obtained by using equations given in **Application Note 5504**. This document is primarily concerned with the power stage and the feedback loop design, and is intended to complement the information contained in the MAX17596 data sheet.

Flyback converters can be operated in DCM or CCM. The component choices, stress level in power devices, and controller design vary depending on the operating mode of the converter. The design discussed in this document is a DCM design, and expressions for calculating component values and ratings are presented to achieve the design goals.

Step 1: Switching Frequency

For this design, we selected a 125kHz switching frequency. The MAX17596 switching frequency is programmable between 100kHz and 1000kHz with a resistor, R_{RT}, con-

nected between RT and SGND. R_{RT} is calculated as follows:

$$R_{RT} = \frac{10^{10}}{f_{SW}}\Omega$$

$$R_{RT} = \frac{10^{10}}{125k} = 80k\Omega$$

A standard 80.6kΩ resistor is selected for R_{RT}.

Step 2: Transformer Magnetizing Inductance and Turns Ratio

In a DCM flyback converter, the energy stored in the primary inductance of the flyback transformer is delivered entirely to the output. The maximum primary-inductance value for which the converter remains in DCM at all operating conditions can be calculated as:

$$L_{PRI} \le \frac{0.4 \times (V_{INMIN} \times D_{MAX})^2}{(V_{OUT} + V_D) \times I_{OUT} \times f_{sw}}$$

where:

D_{MAX} = 0.43V

V_D = 0.76V is the forward-voltage drop of the rectifier diode of the secondary winding.

In this application, the DC input voltage varies from 17V DC to 36V DC. Substitute the values in the equation of L_{PRI} as follows:

$$L_{PRI} \le \frac{0.4 \times (17 \times 0.43)^2}{(12 + 0.76) \times 2 \times 125k} = 6.7\mu H$$

For our design, L_{PRI} is chosen as 6.7µH, L_{PRI} = 6.7µH.

The leakage inductance of the transformer should be targeted as low as possible. For this design, we achieved a 1.5% leakage inductance of 0.1µH, L_{LKG} = 0.1µH. A customized transformer 750318221 from Würth Electronik is used in this design. This transformer also fulfills the specification of turns ratio and primary/secondary currents requirement of the design that is calculated step by step in this document. The transformer has dielectric isolation specification of 1500V AC.

Step 3: Maximum Duty-Cycle Calculation with Selected L_{PRI}

Use the following equations to calculate the maximum duty cycle of the converter for the selected frequency and magnetizing inductance:

$$D_{NEW} = \frac{\sqrt{2.5 \times L_{PRI} \times V_{OUT} \times I_{OUT} \times f_{SW}}}{V_{INMIN}}$$

$$D_{NEW} = \frac{\sqrt{2.5 \times 6.7\mu \times 12 \times 2 \times 125k}}{17} = 0.416$$

Calculate the required transformer turns ratio (k) using the equation as follows:

$$k = \frac{N_s}{N_p} = \frac{(V_{OUT} + V_D) \times (1 - D_{NEW})}{D_{NEW} \times V_{INMIN}}$$

$$k = \frac{N_s}{N_p} = \frac{(12 + 0.7) \times (1 - 0.416)}{0.416 \times 17} = 1.04$$

For the present design, k is chosen as 1:1.

Step 4: Calculation of Peak/RMS Current

Primary and secondary RMS and primary peak currents calculations are needed to design the transformer in switched-mode power supplies. Also, primary peak current is used in setting the current limit. Use the following equations to calculate the primary and secondary peak and RMS currents:

$$I_{PRIPEAK} = \frac{V_{INMIN} \times D_{NEW}}{L_{PRI} \times f_{SW}} = \frac{17 \times 0.416}{6.7\mu \times 125kHz} = 8.46A$$

$$I_{PRIRMS} = I_{PRIPEAK} \times \sqrt{\frac{D_{NEW}}{3}} = 8.46 \times \sqrt{\frac{0.416}{3}} = 3.15A$$

$$I_{SECPEAK} = \frac{I_{PRIPEAK}}{k} = \frac{8.46}{1.04} = 8.06A$$

$$I_{SECRMS} = \sqrt{\frac{2 \times I_{OUT} \times I_{PRIPEAK}}{3 \times k}} = 3.28A$$

Step 5: Current-Limit Resistor Calculation

For the current-limit setting, the peak current can be calculated as follows:

$$I_{LIM} = 1.2 \times I_{PRIPEAK} = 1.2 \times 8.4 = 10A$$

The device includes a robust overcurrent protection scheme that protects the device under overload and short-circuit conditions. A current-sense resistor, connected between the source of the MOSFET and PGND, sets the peak current limit. The current-limit comparator has a voltage trip level ($V_{CS-PEAK}$) of 300mV. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{305m}{I_{MOSFET}} = \frac{305m}{10} = 30.25m\Omega$$

where I_{MOSFET} is the peak current flowing through the MOSFET. A typical 30mΩ current-sense resistor is selected, R_{CS} = 30mΩ.

Step 6: MOSFET Selection

MOSFET selection criteria includes maximum drain voltage, peak/RMS current in the primary, and the maximum allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input

voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum V_{DS} rating must be higher than the worst-case drain voltage as follows:

$$V_{DSMAX} = V_{INMAX} + \left(\frac{2.5 \times (V_{OUT} + V_D)}{k}\right)$$

$$V_{DSMAX} = 60 + \left(\frac{2.5 \times (12 + 0.7)}{1}\right) = 90.39V$$

For this application, we chose the Infineon® IRLR3110ZTRPbF 100V, 63A n-channel MOSFET as the primary MOSFET.

Step 7: Snubber Selection

An RCD snubber reduces the maximum voltage stress on the MOSFET by clamping the voltage level. However, it also dissipates power and reduces efficiency. RCD snubbers may not always be required; however, it is always a good idea to leave placeholders in the board for RCD and RC snubbers. Ideally, the external MOSFET experiences a drain-source voltage stress equal to the sum of the input voltage and reflected voltage across the primary winding during the off period of the MOSFET. In practice, parasitic inductors and capacitors in the circuit, such as leakage inductance of the flyback transformer, cause voltage overshoot and ringing in addition to the ideally expected voltage stress. Snubber circuits are used to limit the voltage overshoots to safe levels within the voltage rating of the external MOSFET. The snubber capacitor can be calculated using the following equation:

$$C_{SNUB} = \frac{2 \times L_{LK} \times I_{PRIPEAK}^2 \times k^2}{V_{OUT}^2}$$

$$C_{SNUB} = \frac{2 \times 0.1\mu \times 8.4^2 \times 1^2}{12^2} = 110nF$$

Considering the derating of the capacitor, we selected a 120nF capacitor, C_{SNUB} = 120nF.

The power that must be dissipated in the snubber resistor is calculated using the following equation:

$$P_{SNUB} = 0.833 \times L_{LKG} \times I_{PRIPEAK}^2 \times f_{SW}$$

$$P_{SNUB} = 0.833 \times 0.1\mu \times 8.4^2 \times 125k = 0.75W$$

The snubber resistor is calculated based on the below equation:

$$R_{SNUB} = \frac{6.25 \times V_{OUT}^2}{P_{SNUB} \times k^2} = \frac{6.25 \times 12^2}{0.75 \times 1^2} = 1.09k\Omega$$

A standard 1.2kΩ, 1W resistor is selected, R_{SNUB} = 1.2kΩ.

The voltage rating of the snubber diode is:

$$VD_{SNUB} = V_{INMAX} + (2.5 \times \frac{V_{OUT}}{k})$$

$$VD_{SNUB} = 60 + (2.5 \times \frac{12}{1}) = 88.6V$$

We selected the Micro Commercial Components® SMD110PL 100V, 1A diode as the snubber diode.

Step 8: Secondary Rectifier Diode Selection

The maximum operating reverse voltage rating of the secondary rectifier diode must be higher than the sum of the output voltage and the reflected input voltage. We use the following equation to calculate the secondary diode voltage rating:

$$V_{SEC,DIODE} = 1.25 \times (k \times V_{INMAX} + V_{OUT})$$

$$V_{SEC,DIODE} = 1.25 \times (1 \times 60 + 12) = 93.7V$$

The current rating of the secondary diode should be selected so that the power loss in the diode (given as the product of forward-voltage drop and the average diode current) should be low enough to ensure that the junction temperature is within limits. It is recommended to select fast-recovery diodes with a recovery time less than 50ns, or Schottky diodes with low junction capacitance.

We selected the STMicroelectronics® STPS30SM100SG 100V, 30A ultra-fast recovery diode as a secondary rectifier diode.

Step 9: Feedback Resistor (R_U, R_B) Selection

A standard 10kΩ resistor is selected, R_B = 10kΩ.

$$R_U = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_B$$

where V_{REF} is the reference set by the secondary-side controller (V_{REF} = 2.5V for the TL431AQDBZRQ1 used in this design).

$$R_U = \left(\frac{12}{2.5} - 1\right) \times 10k\Omega = 38k\Omega$$

A standard 39kΩ resistor is selected, R_U = 39kΩ.

Step 10: Soft-Start Capacitor

The soft-start period for the devices can be programmed by selecting the value of the capacitor C_{SS} connected from the SS pin to SGND. Capacitor C_{SS} can be calculated as:

$$C_{SS} = 8.264 \times t_{SS}$$

where t_{SS} is expressed in ms and the resultant value of C_{SS} is in nF.

$$C_{SS} = 8.264 \times t_{SS} = 8.264 \times 12 = 99.17nF$$

A standard 100nF is selected as the soft-start capacitor, C_{SS} = 100nF.

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Step 11: Input Capacitor Selection

For DC-DC applications, X7R ceramic capacitors are recommended due to their stability over the operating temperature range. The effective series resistance (ESR) and effective series inductance (ESL) of a ceramic capacitor are relatively low, so the ripple voltage is dominated by the capacitive component. For the flyback converter, the input capacitor supplies the current when the main switch is on. We used the following equation to calculate the input capacitor for a specified peak-to-peak input switching ripple:

$$C_{IN} = \frac{D_{NEW} \times I_{PRIPEAK}\left[1-\left(0.5 \times D_{NEW}\right)\right]^2}{2 \times f_{SW} \times V_{IN\_RIP}}$$

Step 12: Output Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of a certain percentage of the rated output current so that the output-voltage deviation is contained to 3% of the rated output voltage. The output capacitance can be calculated by using the below equation:

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output-voltage deviation, and f_C is the target closed-loop crossover frequency. In this application, we selected f_C = 5kHz.

$$I_{STEP} = 0.5 \times I_{OUT} = 0.5 \times 2 = 1A \text{ (50\% of } I_{OUT})$$

$$\Delta V_{OUT} = 0.03 \times 12 = 360mV \text{ (3\% of } V_{OUT}, \text{ typ})$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{5k} + \frac{1}{125k}\right) = 74\mu s$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}} = \frac{1 \times 74\mu}{0.360} = 205\mu F$$

Capacitor values change with temperature and applied voltage. Refer to the capacitor data sheets to select capacitors that guarantee the required output capacitance across the operating range. For design calculations, use the worst-case derated value of capacitance based on temperature range and applied voltage. In this case, the worst-case derated value of capacitors is 219µF.

For the flyback converter, the output capacitor supplies the load current when the main switch is on, and therefore the output-voltage ripple is a function of load current and duty cycle. Use the following equation to estimate the output capacitor ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times \left[I_{PRIPEAK} - \left(K \times I_{OUT}\right)\right]^2}{I_{PRIPEAK}^2 \times f_{SW} \times C_{OUT}}$$

$$\Delta V_{COUT} = \frac{2 \times \left[8.4 - \left(1 \times 2\right)\right]^2}{8.4^2 \times 125kHz \times 219\mu} = 41.2mV$$

Step 13: Loop Compensation

Optocoupler feedback is used in isolated flyback converter designs for precise control of isolated output voltage. Figure 9 shows the overall scheme of the optocoupler feedback.

Use R_{FB} = 470Ω (typ), for an optocoupler transistor current of 1mA. Select R1 = 49.9kΩ and R2 = 22kΩ (typical

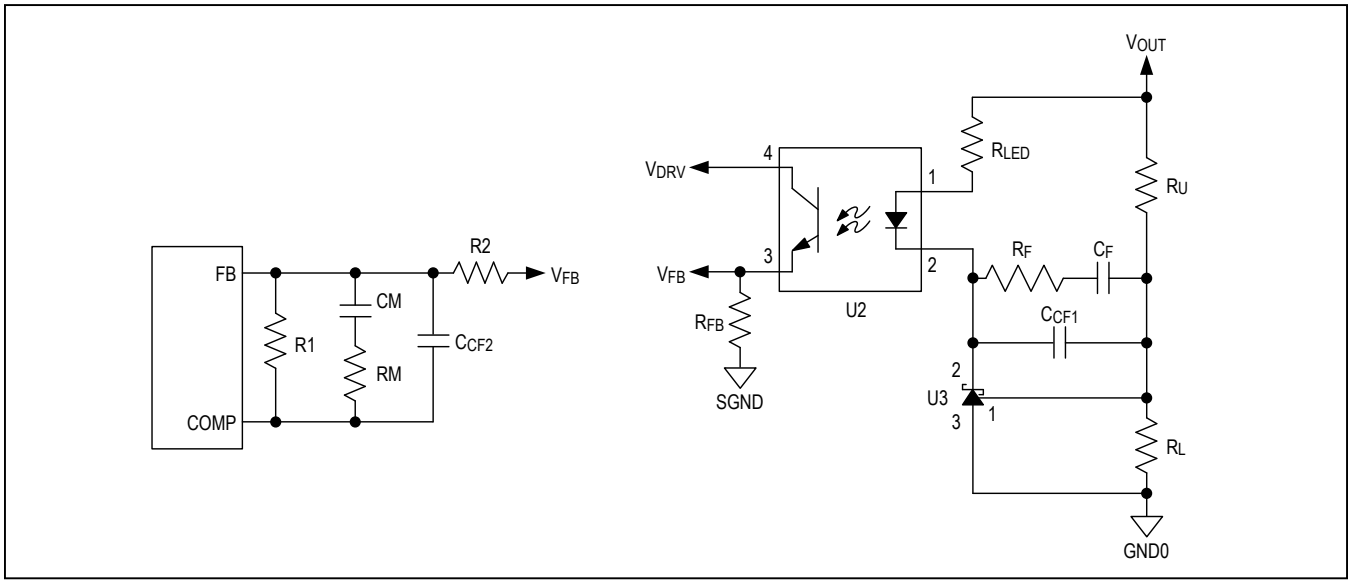

Figure 9. A typical opto-coupler-based feedback compensation.

values) to use the full range of available COMP voltage. U3 is a low-voltage adjustable shunt regulator with a 2.5V reference voltage. In this design, we selected a Texas Instruments® TL431AQDBZRQ1 2.5V shunt regulator.

Calculate R_{LED} using the below equation:

$$R_{LED} = 400 \times CTR \times (V_{OUT} - 2.7)$$

$$R_{LED} = 400 \times 1 \times (12 - 2.7) = 3.72k\Omega$$

A standard 3.65kΩ resistor is selected, R_{LED} = 3.65kΩ.

The bandwidth of typical optocouplers limits the achievable closed-loop bandwidth of opto-isolated converters. Considering this limitation, the closed-loop crossover frequency can be chosen at the nominal input voltage by selecting f_C = 5kHz. Closed-loop compensation values are designed based on the open-loop gain at the desired crossover frequency, f_C. The open-loop at f_C is calculated using the following equation.

$$f_P = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}} = \frac{2}{\pi \times 12 \times 219\mu} = 242Hz$$

$$G_{PLANT} = \frac{f_P}{f_C} \times \sqrt{\frac{L_{PRI} \times f_{SW} \times V_{OUT}}{8 \times I_{OUT}}} \times \frac{V_{IN}}{V_{IN} \times R_{CS} + 50 \times 10^3 \times L_{PRI}}$$

$$G_{PLANT} = \frac{242}{5kHz} \times \sqrt{\frac{6.7\mu \times 125k \times 12}{8 \times 2}} \times \frac{60}{60 \times 30m + 50 \times 10^3 \times 6.7\mu}$$

$$G_{PLANT} = 0.048 \times 0.792 \times 28.1 = 1.077$$

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Three controller configurations are suggested in **Application Note 5504** based on open-loop gain and the R_{LED} value. For typical designs, the current transfer ratio (CTR) of the optocoupler designs can be assumed to be unity. It is known that the comparator and gate-driver delays associated with the input voltage variations affect the opto-coupler CTR. Depending on the optocoupler selected, variations in CTR causes wide variations in bandwidth of the closed-loop system across the input-voltage operating range. It is recommended to select an optocoupler with less CTR variations across the operating range. Checking the condition as stated in **Application Note 5504**:

$$G_{PLANT} \times CTR \times \frac{R_{FB}}{R_{LED}} \times \frac{R_1}{R_2} =$$

$$1.077 \times 1 \times \frac{470}{3.65k} \times \frac{49.9k}{22k} = 0.312$$

As stated in **Application Note 5504**, as 0.339 < 0.8, configuration 1 is selected. Figure 10 shows a typical schematic of configuration 1. The R_F value can be calculated from the equation below:

$$R_F = \left[\frac{R_{LED} \times R2}{G_{PLANT} \times CTR \times R_{FB} \times R1} - 1\right] \times R_U$$

$$R_F = \left[\frac{3.65k\Omega \times 22k\Omega}{1.07 \times 1 \times 470 \times 49.9k\Omega} - 1\right] \times 39k\Omega = 83.57k\Omega$$

A typical 82.5kΩ value is selected as R_F, R_F = 82.5kΩ.

The C_F value can be calculated as follows:

$$C_F = \frac{1}{2\pi \times (R_U + R_F) \times f_P} =$$

$$\frac{1}{2\pi \times (39k\Omega + 82.5k\Omega) \times 242} = 5.416nF$$

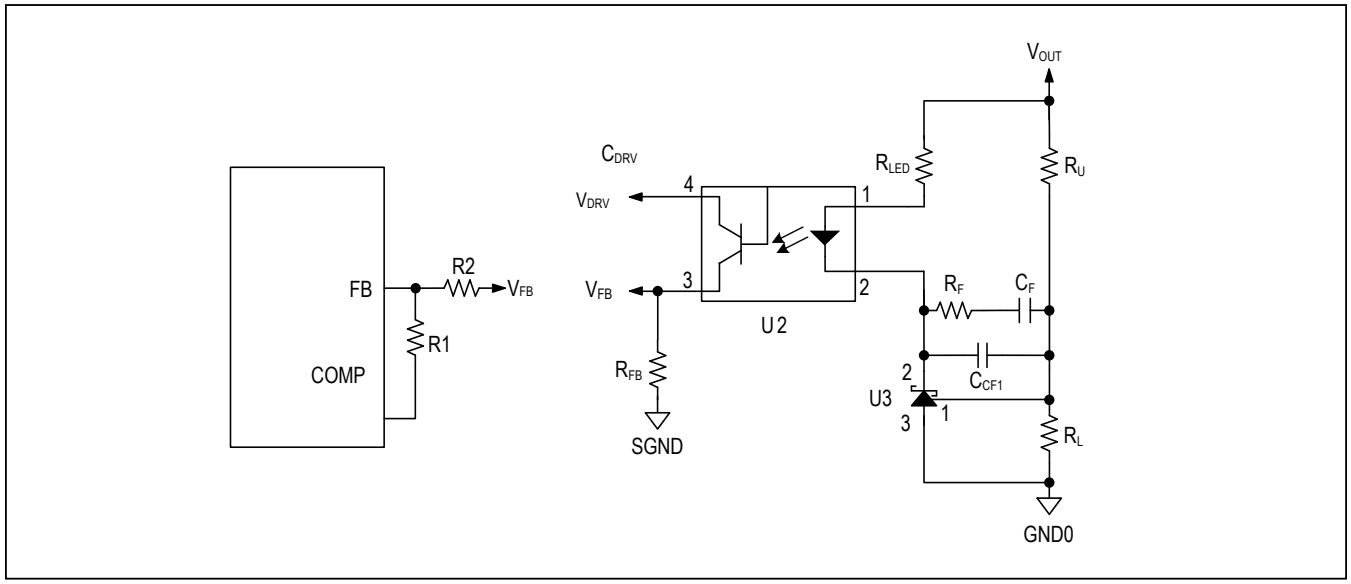

Figure 10. Opto-coupler feedback compensation configuration 1 schematic.

A standard 1.8nF capacitor is selected, C_F = 1.8nF.

The C_{CF1} value can be calculated as follows:

$$C_{CF1} = \frac{1}{\pi \times R_F \times f_{SW}}$$

$$= \frac{1}{\pi \times 82.5k\Omega \times 125kHz} = 30.88pF$$

A standard 39pF capacitor is selected, C_{CF1} = 39pF.

Step 14: EN/UVLO and OVI Setting

The device's EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable input UVLO pin. The device does not commence startup operation unless the EN/UVLO pin voltage exceeds 1.21V. The device turns off if the EN/UVLO pin voltage falls below 1.15V. A resistor-divider from the input DC bus to ground can be used to divide down and apply a fraction of the input DC voltage (V_{DC}) to the EN/UVLO pin. The values of the resistor-divider can be selected so the EN/UVLO pin voltage exceeds the 1.23V turn-on threshold at the desired input DC bus voltage. The same resistor-divider can be modified with an additional resistor (R_{OVI}) to implement input overvoltage protection in addition to the EN/UVLO functionality, as shown in Figure 11.

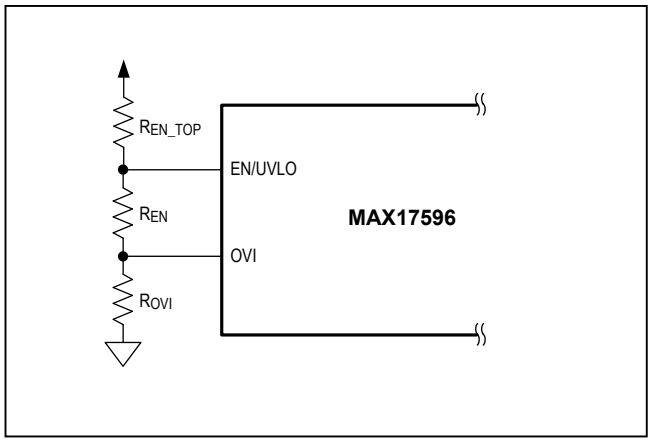

Figure 11. Programming EN/UVLO and OVI.

When voltage at the OVI pin exceeds 1.21V, the device stops switching and resumes switching operations only if voltage at the OVI pin falls below 1.15V. For given values of startup DC input voltage (V_{START}) and input overvoltage-protection voltage (V_{OVI}), the resistor values for the divider can be calculated as follows:

Select R_{OVI} = 10kΩ.

$$R_{EN} = R_{OVI} \times \left(\frac{V_{OVI}}{V_{START}} - 1 \right)$$

where V_{OVI} = maximum allowed overvoltage = 61V.

$$R_{EN} = 10k \times \left(\frac{61}{17} - 1 \right) = 25.5k\Omega$$

A standard 25.5kΩ resistor is selected, R_{EN} = 25.5kΩ.

The same resistor-divider can be modified to implement input overvoltage protection. When the voltage at the OVI pin exceeds 1.215V (typ), the device stops switching. The device resumes switching operations only if the voltage at the OVI pin falls below 1.1V (typ).

$$R_{EN\_TOP} = \left[R_{OVI} + R_{EN} \right] \times \left[\frac{V_{START}}{1.21} - 1 \right]$$

$$R_{EN\_TOP} = \left[10k + 25.5k \right] \times \left[\frac{17}{1.21} - 1 \right] = 463k\Omega$$

A standard 470kΩ resistor is selected for R_{EN_TOP}.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/19	Initial release	—

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