Boosting the Single-Output, 2.6V to 4.5V Input, 12V/833mA Output DC-DC Converter Using the MAX669

MAXREFDES1221

Introduction

This reference design boosts a single-cell battery voltage to a 10W output using the MAX669 controller in the bootstrapped mode. The bootstrap on the input allows the circuit to continue regulating for very low-input voltages.

This circuit boosts to 12V, 0.833A on the output for a 2.6V to 4.5V input. The MAX669 IC in this design is a constant-frequency, pulse-width modulating (PWM), and current-mode DC-DC controller. It can be used for a wide range of DC-DC conversion applications including step-up, SEPIC, flyback, and isolated-output configurations. Power levels of 20W or more can be controlled with conversion efficiencies of over 90%.

Benefits and Features

- Tiny 10-pin µMAX package
- Low-input voltage range
- Current-mode PWM and idle-mode operation
- 220µA quiescent current
- Logic-level shutdown
- Soft-start
- High efficiency

Hardware Specification

A bootstrapped, positive output DC-DC converter using the MAX669 is demonstrated for a 12V DC output application. The power supply delivers up to 833mA at 12V. Table 1 is an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Voltage Range	V_{IN}	2.6	3	4.5
Switching Frequency	f_{SW}		400kHz	
Maximum Efficiency	η		90%	
Duty Cycle	D	64%		86%
Output Voltage	V_{OUT}		12	
Output Voltage Ripple	ΔV_{OUT}			0.36V
Output Current	I_{OUT}	0		0.833A
Output Power	P_{OUT}			10W

Designed–Built–Tested

This reference design describes the hardware in Figure 1. It provides a detailed, systematic technical guide to design a low-voltage boost converter using the MAX669 current-mode PWM controller. The power supply was built and tested. The details follow later in this document.

Figure 1. MAXREFDES1221 hardware.

Boost Converter Principle

A boost (step-up) converter is a DC-DC power converter that steps up the voltage (while stepping down current) from its input to output. The key principle that drives the boost converter is the tendency of an inductor to resist changes in current by creating and destroying a magnetic field. The output voltage is always higher than the input voltage in a boost converter. Figure 2 shows the schematic of a boost power stage.

Figure 3 shows the current flow through the inductor in a clockwise direction. The inductor stores some energy by generating a magnetic field when the switch is on. The polarity of the left side of the inductor is positive. The diode D_1 is reverse-biased during this period. So, there is no current flow through the diode.

Figure 4 shows the current reduction as the impedance is higher when the switch is off. The previously created magnetic field is destroyed to maintain the current toward the load. Thus, the polarity is reversed (the left side of the inductor is negative). The two sources are thus in series, causing a higher voltage to charge the capacitor through the diode D_1.

The average voltage across the inductor over the entire switching cycle is zero in a steady-state operating condition. Thus, the average current through the inductor is also in a steady-state. This is an important rule governing all the inductor-based switching topologies. There is a specific discharge time (t_{OFF}) for an output voltage for a given charge time (t_{ON}), a given input voltage, and with the circuit in equilibrium. The boost circuit is as follows because the average inductor voltage in a steady-state must be zero:

$$V_{IN} \times t_{ON} = t_{OFF} \times V_L$$

and because:

$$V_{OUT} = V_{IN} + V_L$$

the following relationship is established:

$$V_{OUT} = V_{IN} \times \left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

Using the relationship for duty cycle (D):

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

the boost circuit is:

$$V_{OUT} = \frac{V_{IN}}{1 - D}$$

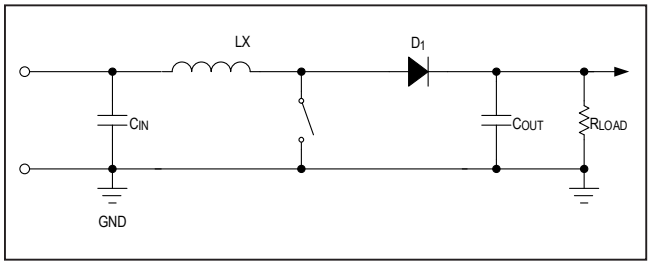

Figure 2. Boost converter topology.

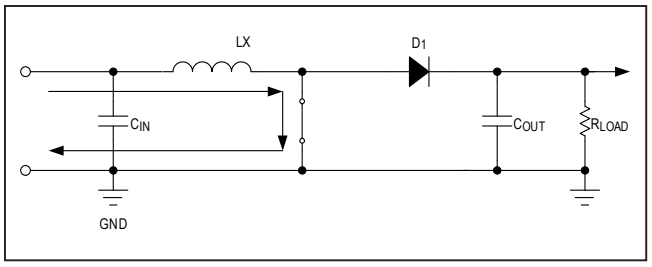

Figure 3. Switch on-period equivalent circuit.cal waveforms.

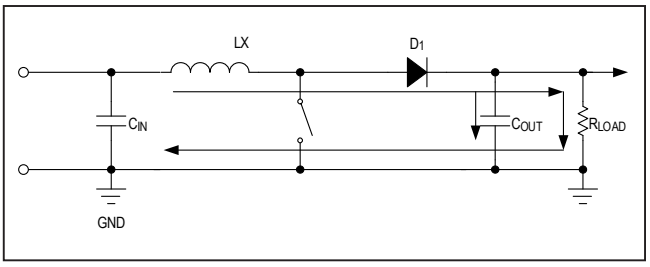

Figure 4. Switch off-period equivalent circuit.

Bootstrapped Operation

The bootstrapped operation for the MAX669 is performed for a low-input voltage range, where the IC is powered from the circuit output (V_{OUT}). This improves efficiency, particularly when the input voltage is below 2.7V. Bootstrapping is required because the MAX669 does not have undervoltage lockout. It instead drives the EXT (External MOSFET Gate Driver Output) pin with an open-loop, 50% duty-cycle start-up oscillator when the LDO is below 2.5V. It switches to closed-loop operation only when the LDO exceeds 2.5V. The output voltage soars above the regulation point if a non-bootstrapped connection is used with the MAX669 and V_{CC} (the input voltage) remains below 2.7V.

Design Procedure for the Boost Converter Using MAX669

Now that the basic principles of the boost converter and bootstrapped operation are understood, a practical design can be illustrated. The converter design process can be divided into several stages: switching frequency and output voltage, inductors, and capacitors, MOSFET and diode. This document complements the information in the MAX669 data sheet. The following abbreviations are used throughout this document.

PARAMETER	SYMBOL
Output Load	I_{OUT}
Average DC Input Current	I_{LDC}
Peak Inductor Current	I_{LPEAK}
Inductance	L
Input Capacitance	C_{IN}
Output Capacitance	C_{OUT}

The design parameters are sometimes followed by parentheses to indicate if minimum or maximum values of the parameters are intended, such as $V_{IN(MIN)}$, for example, to indicate minimum input voltage. Otherwise, the typical values are intended.

Step 1. Selecting the Switching Frequency

The MAX669 can be set to operate from 100kHz to 500kHz. The oscillator frequency is set by a resistor, R_{OSC}, connected from the FREQ to GND. The R_{OSC} must be connected whether the part is externally synchronized or not, and as an external clock was not used in this design. The following equation determined ROSC for the specified 400kHz switching frequency:

$$R_{OSC} = \frac{5 \times 10^{10}}{f_{OSC}} = \frac{5 \times 10^{10}}{400 \times 10^{3}} = 125k\Omega$$

A 124kΩ resistor was chosen for R4.

Step 2. Calculating the Output Voltage

The output voltage is set by connecting a resistor-divider (comprising resistors R_2 and R_3) to the FB pin from the corresponding output to GND. The value for R_3 is within the 10kΩ to 1MΩ range. A resistor of 100kΩ was initially chosen for R_3 and the corresponding value for R_2 was:

$$R_2 = R_3\left(\frac{V_{OUT}}{V_{REF}} - 1\right) = 1 \times 10^5\left(\frac{12}{1.25} - 1\right) = 860k\Omega$$

where V_{REF} is 1.25V. The values for R_2 and R_3 were 866kΩ and 97.6kΩ, respectively.

Step 3. Selecting the Inductor

The key parameters to select the inductor are:

- Inductance (L)
- Inductor saturation current (ISAT)
- DC resistance of inductor (DCR)

The required inductance (L) is calculated based on the ratio of the inductor's peak-to-peak ripple AC current to its DC average current. This is called the inductor ripple current ratio or LIR. An LIR of 30% was selected. The switching frequency f_{SW}, input voltage VIN, inductor current IL, and selected LIR determine the inductance value as:

$$V_{IN(MAX)} - V_T = L\frac{LIR \times I_L}{D \times T}$$

$$L = \frac{\left(V_{IN(MAX)} - V_T\right) \times D}{LIR \times I_L \times f_{SW}}$$

$$L = \frac{(4.5V - 0.05V) \times 0.64}{0.3 \times 2.47A \times (400 \times 10^3)Hz} = 9.61uH$$

where V_T is the voltage drop across the MOSFET. The maximum inductance value is obtained at the maximum input voltage and where D is the minimum duty cycle:

$$D = \frac{V_o - V_{IN(MAX)} + V_D}{V_o - V_T + V_D}$$

$$D = \frac{12V - 4.5V + 0.5V}{12V - 0.05V + 0.5V} = 0.64$$

V_D is the forward voltage drop across the Schottky output diode. The current through the inductor is calculated using the efficiency (η) and power relationship:

$$I_L = \frac{V_o \times I_o}{V_{IN} \times \eta} = \frac{12V \times 0.833A}{4.5V \times 0.9} = 2.47A$$

An inductance value of 10µH with a tolerance of ±20%, maximum DC resistance of 15mΩ, and saturation current of 11.32A was used in this reference design.

Step 4. Calculating the Peak Current and Current-Sense Resistor

The current-sense resistor, R_{CS}, connected between the source of the MOSFET Q1 and PGND is used to set the peak current limit as:

$$I_{LPEAK} = I_{LDC} + \frac{I_{LPP}}{2}$$

where I_{LDC} is the average DC input current and I_{LPP} is the inductor peak-to-peak ripple current. The I_{LDC} and I_{LPP} are determined as:

$$I_{LDC} = \frac{I_{OUT} \times (V_{OUT} + V_D)}{V_{IN(MIN)} - V_T}$$

$$= \frac{0.833A \times (12V + 0.5V)}{2.6V - 0.05V} = 4.08A$$

$$I_{LPP} = \frac{(V_{IN(MIN)} - V_T) \times (V_{OUT} + V_D - V_{IN(MIN)})}{L \times f_{SW} \times (V_{OUT} + V_D)}$$

$$= \frac{(2.6V - 0.05V) \times (12V + 0.5V - 2.6V)}{10 \times 10^{-6} L \times 400 \times 10^{3} Hz \times (12V + 0.5V)} = 0.50A$$

$$I_{LPEAK} = 4.08A + \frac{0.50A}{2} = 4.34A$$

Once the peak inductor current is selected, the current-sense resistor is:

$$R_{CS} = \frac{85mV}{I_{LPEAK}} = 19.59m\Omega$$

A current sense resistor of 15mΩ was chosen with a tolerance of ±1%

Step 5. Selecting the Input Capacitor

The input filter capacitor is used to reduce the peak currents drawn from the power sources, and further reduce the noise and voltage ripples caused by the circuit's switching. The minimum required input ceramic capacitor can be calculated using the capacitor's voltage-current relation:

$$\Delta V = \frac{1}{C_{IN}} \int Idt$$

Figure 5 shows the input capacitor current waveform. The area under the current waveform denotes the charge enclosed. So, geometrical interpretations are used to deduce the following:

$$\Delta V = \frac{1}{C_{IN}} \times \left(\frac{1}{2} \times \frac{t_{ON}}{2} \times \frac{\Delta I}{2} + \frac{1}{2} \times \frac{t_{OFF}}{2} \times \frac{\Delta I}{2} \right)$$

$$C_{IN(MIN)} = \frac{LIR \times I_{L(MAX)}}{8 \times \Delta V_{IN(MIN)} \times f_{SW}}$$

$$C_{IN(MIN)} = \frac{0.3 \times 4.34A}{8 \times (2.6V \times 0.02) \times 400 \times 10^{3} Hz} = 7.82\mu F$$

where ΔV_{IN} is the ripple voltage allowed on the input DC bus. Here, ΔV_{IN} = 2% of V_{IN}. Two ceramic capacitors, each with a value of 10µF, were chosen and placed in parallel because of the DC bias and to reduce the effects of the ESR.

Step 6. Selecting the Output Capacitor

The minimum output filter capacitance is determined as:

$$C_{OUT(MIN)} = \frac{7.5V \times \frac{L}{L_{IDEAL}}}{2\pi R_{CS} \times V_{IN(MIN)} \times f_{SW}}$$

$$= \frac{7.5V \times \frac{10\mu H}{9\mu H}}{2\pi \times 15 \times 10^{-3} \Omega \times 2.6V \times 400 \times 10^{3}} = 85\mu F$$

The optimal value for stability is based on the MAX668/669's internally-set slope compensation. The inductance value that provides this stability is determined using the following L_{IDEAL} relationship:

$$L_{IDEAL} = \frac{V_{OUT}}{4 \times I_{OUT} \times f_{SW}}$$

$$= \frac{12V}{4 \times 0.833A \times 400 \times 10^{3} Hz} = 9\mu H$$

The output filter capacitance must also be increased by the same proportion that L has to L_{IDEAL} as the inductance value used in this design is greater than the L_{IDEAL} value.

The calculated $C_{OUT(MIN)}$, although sufficient for stability, is not adequate for low-output voltage ripple. A capacitance value two or three times larger than the $C_{OUT(MIN)}$ is needed as the output ripple in the boost DC-DC designs is dominated by the capacitance equivalent resistance (ESR). Therefore, four ceramic capacitors, each with a value of 47µF, were chosen in this design with ±20% tolerance and an effective ESR of 0.844mΩ.

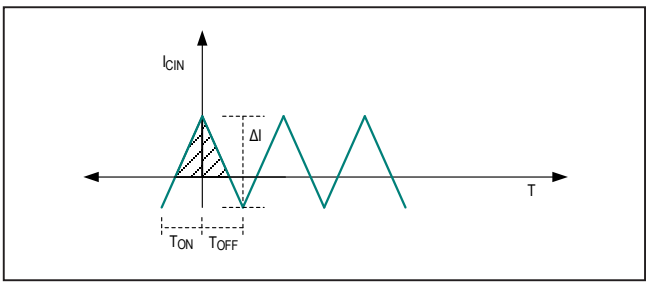

Figure 5. Input capacitor current waveform.

Step 7. Selecting the Compensation and Bypass Capacitor

The output ripple voltage due to C_{OUT} ESR affects the loop stability by introducing a left half-plane zero. A small capacitor connected from the FB to GND forms a pole with the feedback resistance that cancels the ESR zero. The optimum compensation value is:

$$C_{FB} = C_{OUT} \times \frac{ESR_{C_{OUT}}}{(R_2 \times R_3)/(R_2 + R_3)}$$

$$C_{FB} = 170\mu F \times \frac{0.844m\Omega}{(866 \times 100) \times 10^3 / 866 + 100) \times 10^3} = 1.6pF$$

where R_2 and R_3 are the feedback resistors. Three ceramic bypass capacitors are required for the MAX668/669 in addition to C_{IN} and C_{OUT}. The bypass capacitor from the REF to GND was chosen as 0.47µF, from LDO to GND as 2.2µF, and from V_{CC} to GND as 0.22µF.

Step 8. Selecting the Output Diode

Ensure the reverse-breakdown voltage exceeds the V_{OUT} when choosing a diode. The MAX668/MAX669's high-switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. Also, ensure the diode's average current rating is adequate using the diode manufacturer's data. The VS-MBRS130L-M3 with 30V reverse voltage and 1A forward current was chosen as the output diode for this design based on the specifications.

Step 9. Selecting the nFET

The MAX668/669 can drive a wide variety of n-channel power MOSFETs (nFETs). The key parameters when selecting an nFET include:

1) Total gate charge - Q_{GATE}
2) On-resistance - $R_{DS(ON)}$
3) Output capacitance - C_{OSS}
4) Maximum drain-to-source voltage - $V_{DS(MAX)}$
5) Power dissipation rating and package thermal resistance

The n-Channel MOSFET FDD86102LZ with a drain-to-source voltage of 100V, drain current of 35A, and on-resistance of 22.5mΩ is chosen for this design.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/20	Initial release	—