Dual-Phase Buck Converter with Inductor DCR Current Sensing Using the MAX17558

MAXREFDES1202

Introduction

The MAXREFDES1202 is a dual-phase, buck converter reference design developed using the MAX17558, MAX15019A, and MAX17552. This reference design is rated to operate over a wide input voltage range from 15V to 55V. The design can deliver an output power of 360W at 12V.

Main features include the following:

- Very High Efficiency > 95% at Full Load
- Very Low Line Regulation < 0.1% and Very Low Load Regulation < 0.25%
- Inductor DCR Current Sensing
- Output-Voltage Ripple < 0.5% at V_{IN} (nom)
- Overshoot < 3% for 50% Step Load

Hardware Specification

A single-output, dual-phase buck converter is demonstrated for a 15V to 55V input voltage range application. The output is 12V, delivering 30A of current at full load.

The MAX17558 is used for controlling the converter. This IC is a dual-output, synchronous step-down controller using a constant-frequency, peak-current-mode architecture. It has wide input supply range of 4.5V to 60V. The device also provides the ability to run two controllers 180° out of phase to reduce power loss and noise due to the input-capacitor ESR.

The gate pulses from the MAX17558 are input to the MAX15019A gate driver, which is used for driving the MOSFETs. The MAX15019A is a high-frequency, 125V half-bridge, n-channel MOSFET driver that drives high and low-side MOSFETs. This IC supports supply voltages from 8V to 12.6V V_{DD}, thus making it suitable for driving MOSFETs with higher gate threshold voltage.

The power supply for the gate driver is derived from the MAX17552 low-cost, high-voltage buck controller IC.

Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Voltage	V_{IN}	15	48	55
Output Voltage	V_O		12V	
Load Current	I_O		30A	
Frequency	f_{SW}		100kHz	
Efficiency at Full Load	η		>90%	
Voltage Overshoot	ΔV_{O_OS}		5%	

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed, systematic technical guide for designing a dual-phase buck converter using the MAX17558 current-mode controller. This power supply has been built and tested, details of which follow later in this document.

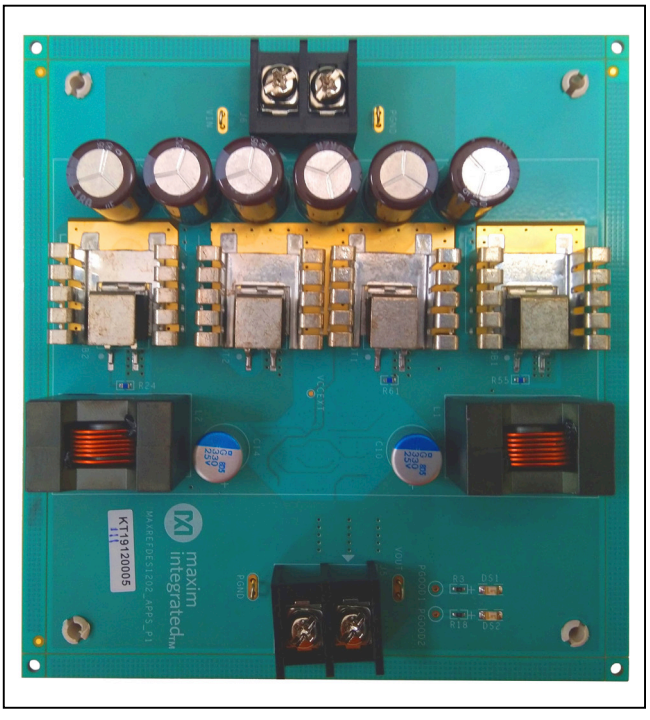

Figure 1. MAXREFDES1202 hardware.

Quick Start

Required Equipment

- DC Power Supply
- DC Electronic Load
- Multimeter
- Oscilloscope

Procedure

This reference design is fully assembled and tested. Follow these steps to verify board operation:

1) Connect a 60V DC power supply to the input.
2) Keep the input voltage at 48V and turn on.
3) Observe the output voltage using a multimeter. It should show 12V.
4) Connect a DC electronic load at the output and load in steps up to 30A. Observe the output-voltage regulation and output ripple.

Operation of a Dual-Phase Buck Converter

Figure 2 shows the electrical block diagram of a dual-phase buck converter. The two phases share a common input and load. Current delivered to the load is shared equally by the inductors and switches. Each phase is operated with 180° phase difference between the PWM gate signals for improved ripple performance.

Compared to single-phase buck regulators, a dual-phase buck converter offers several advantages as follows:

1) Load Sharing
2) Input Ripple Reduction
3) Output Ripple Reduction

As seen in Figure 2, the two phases are operated at a 180° phase shift. G_1 and G_2 are the gate signals applied to the top switches of their respective phases. I_{L1} and I_{L2} are the inductor currents, I_{QT1} and I_{QT2} are the top switch currents, and I_{CO} is the output capacitor current.

Assuming that the current drawn from the input supply is DC, the AC of the switch currents I_{QT1} and I_{QT2} is supplied by the input capacitor. The phase shift of the two switch currents effectively reduces the peak of the input current by half, while the frequency is doubled.

Similarly, the inductor currents I_{L1} and I_{L2} supply the load. A 180° phase shift between the two phases causes a reduced ripple current (I_{CO}) in the output capacitor.

Design and Power Loss in Critical Components

Inductor

The required inductance per phase is calculated based on the inductor ripple current ratio (LIR). This is defined as the ratio of the peak-to-peak inductor current (ΔI_L) to the average current (I_O). For a switching frequency:

$$f_{SW} = \frac{1}{T_S} Hz$$

and operating at a minimum duty cycle:

$$D = \frac{V_O}{V_{IN\,MAX}}$$

and

$$LIR = \frac{\Delta I_L}{I_O}$$

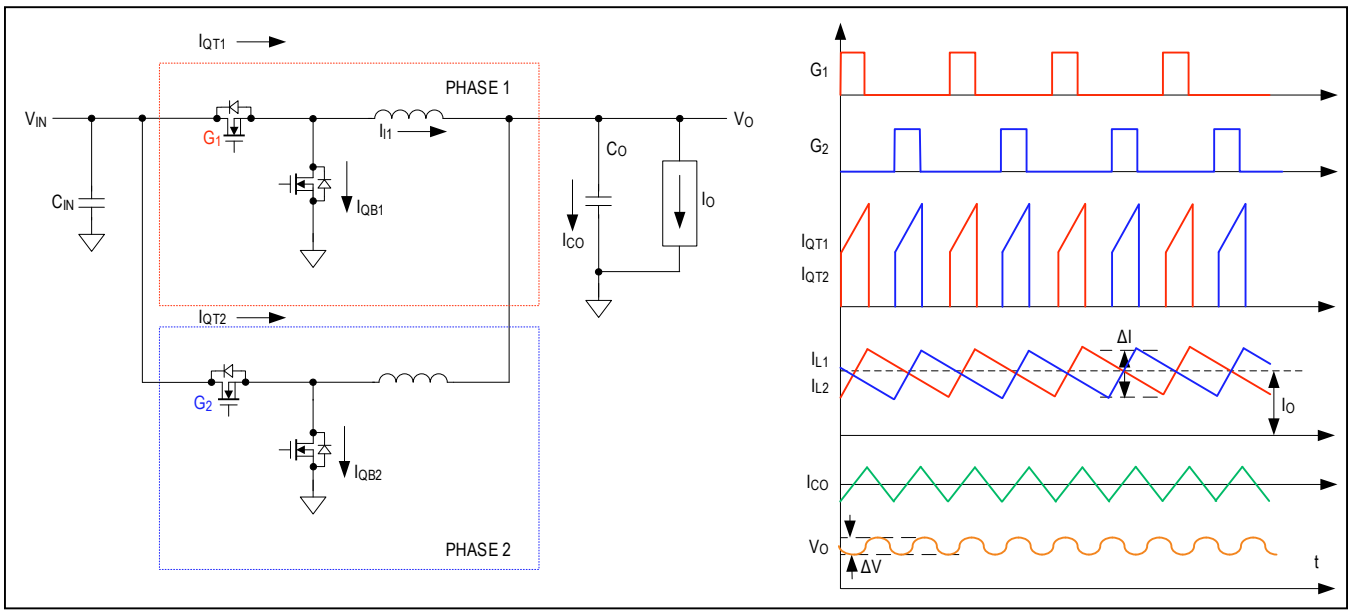

Figure 2. Power stage and steady-state waveforms in a dual-phase buck converter.

the inductance required per phase is calculated by applying volt-second balance on the inductor voltage as follows:

$$L\frac{\Delta I_L}{DT_S} = (V_{INMAX} - V_O)$$

With LIR at 0.4 and the load current at 15A (per phase current), the value of inductance is calculated. Based on the calculated specifications for the inductors, the Coilcraft® VER2923-153KL was selected.

$$L_1 = L_2 = 15\mu H$$

The losses in the inductor have two components: copper loss and core loss. The core loss is obtained from the manufacturer website. The copper loss is calculated as follows:

$$\text{Inductor copper loss} = I_{L-RMS}^2 \times R_{CS}$$

where:

$$I_{L-RMS}^2 = I_O^2 + \frac{\Delta I_L^2}{12}$$

R_{CS} is the DC resistance (DCR) of the inductor. DCR is used for current sensing in this reference design.

$$R_{CS} = 2.6m\Omega$$

Table 2 gives a summary of the calculated values for power loss in each inductor.

Table 2. Power Loss at Nominal Operating Voltage

PARAMETER	SYMBOL	VALUE	UNITS
Inductor Ripple Current Ratio	LIR	0.4	—
Peak-to-Peak Inductor Ripple	ΔI_L	6.0	A
Duty Cycle at VG_{NOM}	D	0.25	—
Inductor RMS Current at Full Load	I_{L-RMS}	15.10	A
Inductor Cu Loss per Phase	P_{IND-CU}	0.59	W
Inductor Core and AC Losses (approx.) per Phase	P_{IND-AC}	1	W

Current Sensing

An inductor DCR is used for current sensing in this design. This effectively reduces the losses associated with two current shunt resistors, leading to improved efficiency. The voltage across the inductor is conditioned to obtain the current signal.

Figure 3 shows the DCR current-sensing circuit. An RC low-pass filter is connected across the inductor, which has a DC resistance of R_{CS}.

The equations relating the current through the inductor and voltage developed across the inductor can be written in the Laplace domain as follows:

$$V_L(s) = (R_{CS} + Ls)I_L(s)$$

$$V_{CS}(s) = \frac{1}{R_C C_C s + 1} V_L(s)$$

having:

$$\frac{L}{R_{CS}} = R_C C_C$$

The sensed voltage (V_{CS}) is a simple gain multiplied by the inductor current (I_L), $V_{CS} = R_{CS}I_L(s)$, and the values are R_C = 17.4kΩ and C_C = 330nF.

Table 3 gives the values of current-sense signal (V_{CS}) for the full load current at a nominal input voltage of 48V.

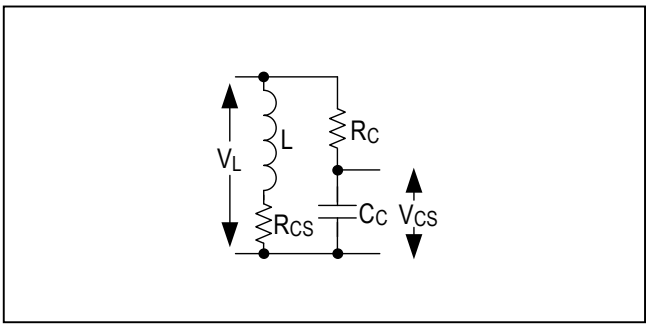

Figure 3. DCR current-sensing circuit.

Table 3. Current-Sense Voltage and Current Levels at Nominal Operating Conditions

PARAMETER	SYMBOL	VALUE	UNITS
DCR Resistance	R_{CS}	2.6	mΩ
Peak Inductor Current	I_P	18	A
Measured Sense Signal	V_{CS}	46.8	mV
Current-Sense Limit	V_{LIM}	75	mV
Current-Sense Amplifier Gain	G_{CS}	13.3	—

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MOSFETs

The current and voltage waveforms in the synchronous switches during on and off period are shown in Figure 4a for one phase. The on-state losses are due to a resistive drop in the MOSFETs.

The RMS current and the conduction power loss ($P_{T\text{-}CONDN}$) in the top device of a phase are given by the following equations:

$$I_{QT1-RMS}^2 = D\left(I_{L1}^2 + \frac{\Delta I^2}{12}\right)$$

$$P_{T-CONDN} = I_{QT1-RMS}^2 \times R_{RDS-ON}$$

Figure 4b shows the turn-on and turn-off transients in the MOSFET. I_D is the drain current and V_{DS} is the drain-to-source voltage of the MOSFET. The switching loss ($P_{T\text{-}SW}$) during turn-on and turn-off transients and the gate charging loss ($P_{T\text{-}GATE}$) are calculated as follows:

$$P_{T-SW} = f_{SW} V_{IN} I_{L1} \Delta t$$
$$P_{T-GATE} = Q_G V_{DRIVE} f_{SW}$$

The total power losses (P_T) in the top MOSFET per phase are calculated as follows:

$$P_T = P_{T-CONDN} + P_{T-SW} + P_{T-GATE}$$

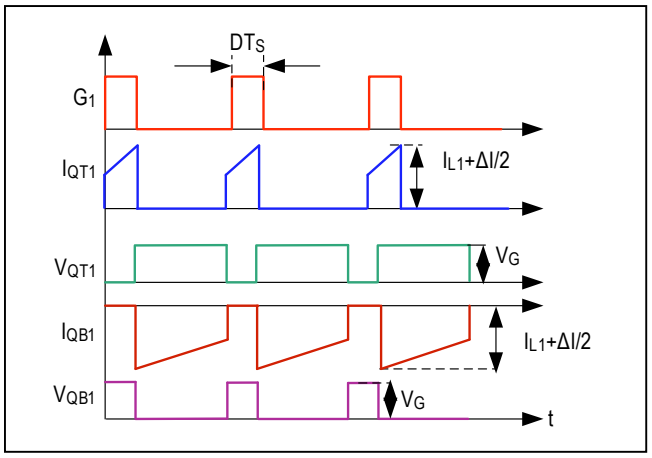

Figure 4a. Switching waveforms across the MOSFET.

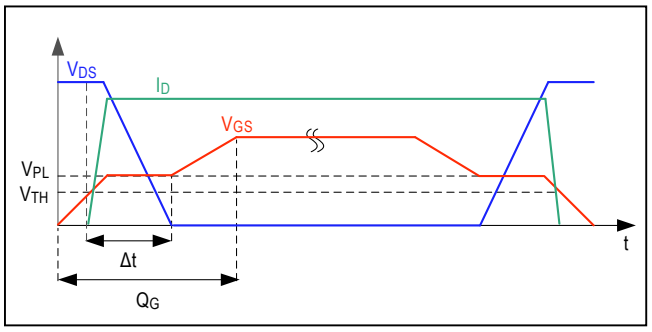

Figure 4b. Turn-on and turn-off transients.

Refer to the BOM in the **Design Resources** tab for the components chosen.

Table 4. Power Loss in Top MOSFET at Nominal Operating Conditions

PARAMETER	SYMBOL	VALUE	UNITS
Drain-to-Source Resistance	$R_{DS\text{-}ON}$	2.0	mΩ
RMS Current of Top MOSFET	$I_{QT1\text{-}RMS}$	7.55	A
Conduction Loss	$P_{T\text{-}CONDN}$	0.148	W
Turn-On Time	Δt	26	ns
Switching Loss	P_{T_SW}	1.8	W
Gate Loss	Q_G	168	nC
Gate Drive Loss	P_{T_GATE}	0.168	W

The RMS current $I_{QB1\text{-}RMS}$ and on-state conduction losses ($P_{B\text{-}CONDN}$) in the bottom device are given by the following equations:

$$I_{QB1-RMS}^2 = (1-D)\left(I_{L1}^2 + \frac{\Delta I^2}{12}\right)$$

$$P_{B-CONDN} = I_{QB1-RMS}^2 \times R_{RDS-ON}$$

During dead times (when DH is falling and DL is rising or when DL is falling and DH is rising), the body diode of the lower MOSFET conducts to maintain current through the inductor. This can be termed as “dead-time loss” ($P_{B\text{-}DT}$). Also, when the top MOSFET is turning on, the body diode of the lower MOSFET recovers to the blocking state, leading to reverse-recovery losses (P_{RR}) in the device.

$$P_{B-DT} = V_F\left[(I_O - \frac{\Delta I}{2})T_D + (I_O + \frac{\Delta I}{2})T_D\right] f_{SW}$$
$$P_{RR} = Q_{RR} V_{IN} f_{SW}$$

Table 5 shows the summary of losses in the bottom MOSFET.

Table 5. Power Loss in the Bottom MOSFET at Nominal Operating Conditions

PARAMETER	SYMBOL	VALUE	UNITS
Drain-to-Source Resistance	$R_{DS\text{-}ON}$	2.0	mΩ
RMS Current of Top MOSFET	$I_{QB1\text{-}RMS}$	13.1	A
Conduction Loss	$P_{B\text{-}CONDN}$	0.342	W
Dead Time	Δt_D	40	ns
MOSFET Diode Drop	V_F	0.9	V
Dead-Time Loss	$P_{B\text{-}DT}$	0.054	W
Gate Drive Loss	P_{B_GATE}	0.168	W
Reverse-Recovery Charge	Q_{RR}	287	nC
Reverse-Recovery Loss	P_{RR}	1.3776	W

Output Capacitor

Figure 5 shows the current in the two inductors and in the output capacitor when operating in full load at a nominal input voltage. The capacitor sees the ripple current at twice the switching frequency of the inductor current.

The ratio of the peak-to-peak capacitor ripple current to the inductor ripple current is around 0.75 at duty cycle of 0.25. The RMS current through the output capacitor is calculated as follows:

$$I_{CO\_RMS} = \frac{\Delta I_C}{2\sqrt{3}} ; \Delta I_C = 0.75 \Delta I_L$$

The output capacitance (C_{OUT}) depends on the desired steady-state voltage ripple and voltage overshoot specification. The steady-state ripple (ΔV_{O_SS}) has 2 components: one due to drop in actual capacitance (ΔV_{O_Q}) and another due to drop in ESR of the capacitor (ΔV_{O_ESR}).

$$\Delta V_{O\_SS} = \Delta V_{O\_ESR} + \Delta V_{O\_Q}$$

For ceramic capacitors, ΔV_{O_Q} predominates. For electrolytic capacitors, the ΔV_{O_ESR} component predominates.

For a steady-state ripple of ΔV_{O_SS}, the desired output capacitance is calculated from the following equations:

$$\Delta V_{O\_Q} = \frac{\Delta I_C}{8 f_{SW} C_{OUT}} ; \Delta V_{O\_ESR} = \Delta I_C \times ESR$$

For achieving good transient performance, the required output capacitance is calculated as:

$$C_{OUT} = \frac{\Delta I_O \tau}{\Delta V_{O\_OS}} ; f_C = \frac{f_{SW}}{10} ; \tau = \frac{1}{3 f_C}$$

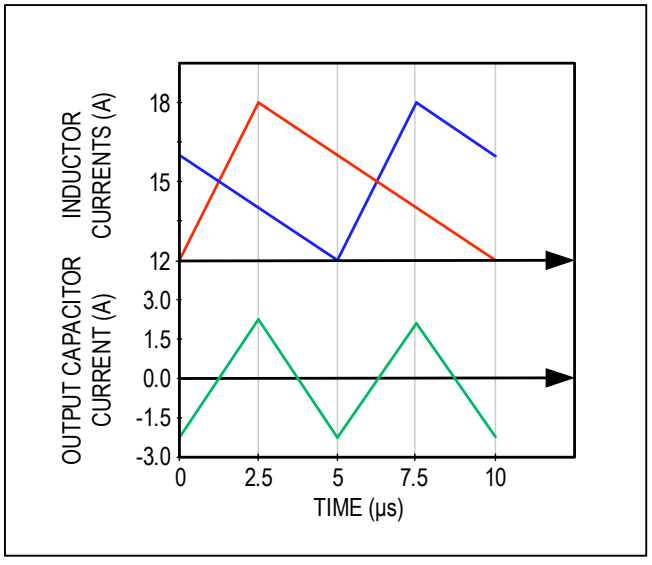

Figure 5. Current through the inductors and output capacitor.

where ΔI_O is the total load change, f_C is the unity gain bandwidth (or crossover frequency), and ΔV_{O_OS} is the transient overshoot specification.

A combination of electrolytic and ceramic capacitors has been used for optimal performance in this design. Table 6 shows the summary of current and loss in the output capacitor.

Table 6. Current and Power Loss in the Output Capacitor

PARAMETER	SYMBOL	VALUE	UNITS
Peak-to-Peak Inductor Ripple	ΔI_L	6.0	A
Peak-to-Peak Capacitor Ripple Current	ΔI_C	4.5	A
Capacitor RMS Current	I_{CO_RMS}	1.3	A
Total Output Capacitance	C_{OUT}	833	µF
Effective Series Resistance	ESR	14	mΩ
Power Loss	P_{CO}	2.73	mW

Input Capacitor

The input filter capacitor reduces the peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

Figure 6 illustrates the current flowing through the switch and input capacitor during rated operating voltage and current. For a DC current drawn from the input (I_{IN} = DI_O), the RMS current flowing through the input capacitor for a single-phase buck converter is given as:

$$I_{CIN-RMS}^2 = D\left[(1-D)I_O^2 + \frac{\Delta I^2}{4}\right]$$

The RMS of the current in input capacitor for a dual-phase buck converter under nominal operating conditions (D < 0.5) is given as:

$$I_{CIN-RMS}^2 = D\left[(1-2D)I_O^2 + \frac{\Delta I^2}{8}\right]$$

Table 7. RMS Current in the Input Capacitor for Single- and Dual-Phase Buck Converters

PARAMETER	SYMBOL	VALUE	UNITS
Input Capacitance RMS Current for Single-Phase Buck Converter	$I_{CIN-RMS-1PH}$	13.33	A
Input Capacitance RMS Current for Dual-Phase Buck Converter	$I_{CIN-RMS-2PH}$	10.8	A

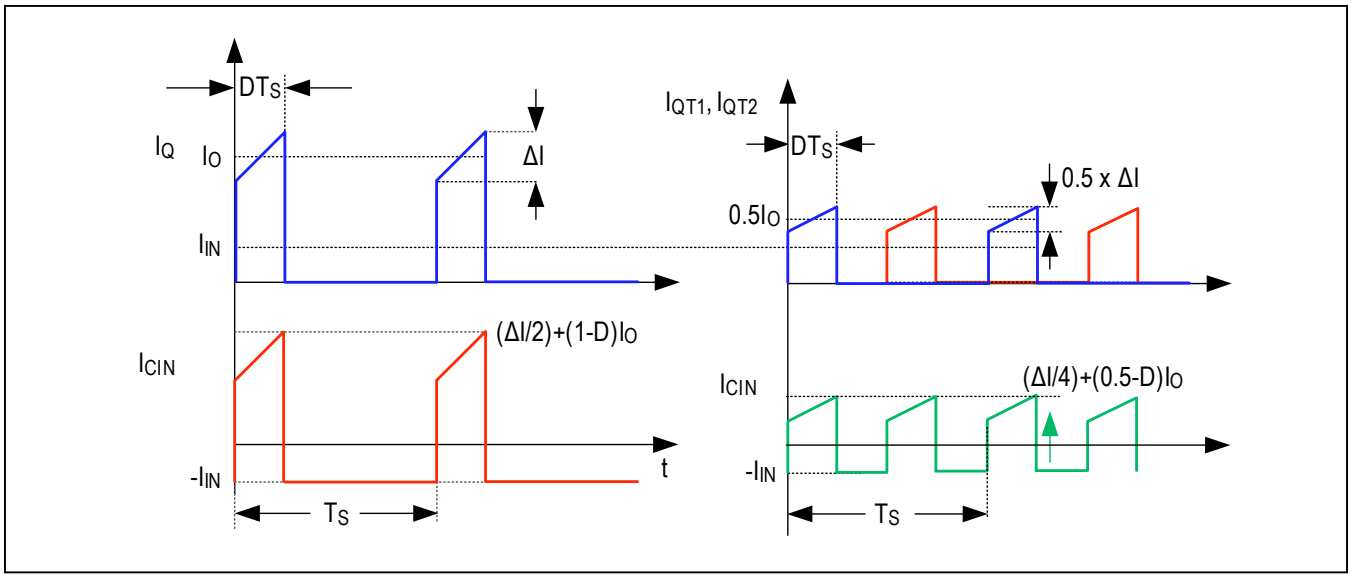

Figure 6. Comparison of ripple currents flowing through the input capacitor in a single- and dual-phase buck converter for D < 0.5.

Compensation

Figure 7 shows the control block diagram of a dual-phase buck converter. The output-voltage error amplifier of both phases operates in parallel to derive a single control signal (V_C). Here, G_{CS} is the current-sense amplifier gain, G_M is the internal transconductance error amplifier gain, and G_{FB} is the output-voltage feedback divider gain (0.8/output voltage).

The plant transfer function consists of the pole f_{P1} formed by the load and output capacitor:

$$f_{P1} = \frac{1}{2 \times \pi \times C_O \times R_{LOAD}}$$

An additional zero (f_{Z1}) is introduced by the output capacitor ESR:

$$f_{Z1} = \frac{1}{2 \times \pi \times C_O \times R_{ESR}}$$

The voltage error amplifier transfer function introduces one zero and two poles.

The crossover frequency is kept at 1/10th of the switching frequency f_{SW}, and R_Z is calculated from the following:

$$R_Z = \frac{2 \times \pi \times f_{CO} \times C_O \times G_{CS} \times R_{CS}}{G_M \times G_{FB}} = 3.3k\Omega \; ; \; f_{CO} = \frac{f_{SW}}{10}$$

C_Z is calculated by placing the compensator zero near the system pole f_{P1}:

$$C_Z = \frac{1}{2 \times \pi \times f_{P1} \times R_Z} = 0.1\mu F$$

C_P is calculated by placing the compensator pole near f_{Z1}, or half of the switching frequency, whichever is the minimum:

$$C_P = \frac{1}{2 \times \pi \times f_{P\_EA} \times R_Z} = 1nF; \; f_{P\_EA} = \min(f_{Z1}, \frac{f_{SW}}{2})$$

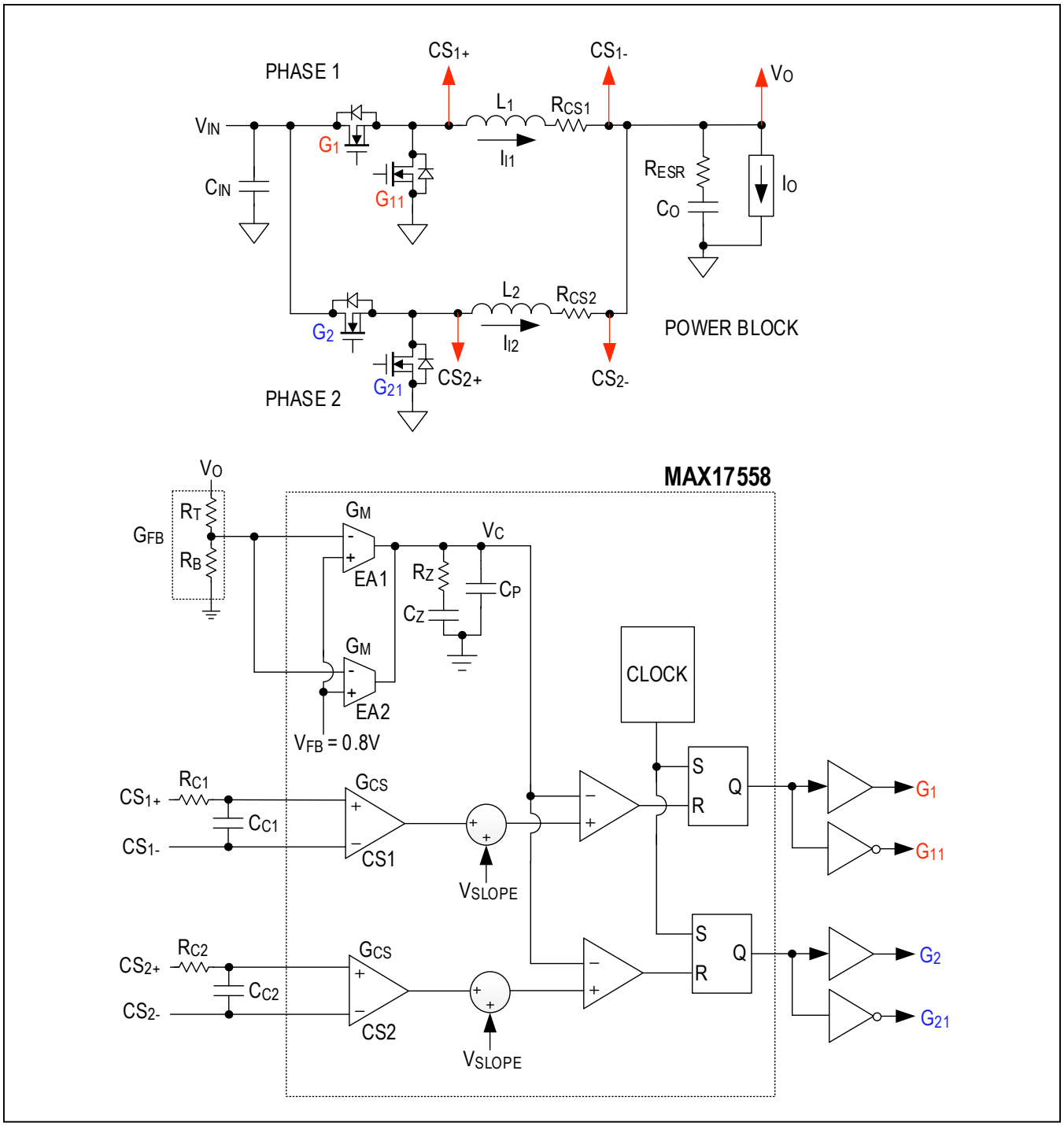

Figure 7. Block diagram of a dual-phase buck converter with current-mode control.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/20	Initial release	—