Ultra-Miniature 4.5V to 36V Input and 3.3V, 2A, High-Efficiency, Synchronous Step-Down DC-DC Converter

MAXREFDES1198

Introduction

The MAX17632 family of parts (MAX17632A, MAX17632B, and MAX17632C) includes high-efficiency, high-voltage, synchronous step-down DC-DC converters with integrated MOSFETs operating over an input-voltage range of 4.5V to 36V. These parts can deliver current up to 2A. The MAX17632A and MAX17632B are fixed 3.3V and fixed 5V output parts, respectively. The MAX17632C is an adjustable output voltage (0.9V to 90% of V_{IN}) part. Built-in compensation across the output-voltage range eliminates the need for external compensation components.

The MAX17632 features peak-current-mode control architecture. The device can be operated in forced pulse width modulation (PWM), pulse-frequency modulation (PFM), or discontinuous-conduction mode (DCM) to enable high efficiency under full-load and light-load conditions. Key features of this design include the following:

- Wide 4.5V to 36V Input
- 3.3V Output
- Up to 2A Output Current
- Fully Assembled and Tested
- Proven PCB Layout

Hardware Specification

This design is a single-output, synchronous buck, step-down DC-DC converter for small size and low output voltage. Table 1 provides an overview of the design specification.

Hardware Needed for Quick Setup

- 4.5V to 36V, 10A DC input power supply
- MAXREFDES1198 board
- Load capable of sinking 5A
- Digital voltmeter (DVM)

Designed–Built–Tested

This document provides a detailed systematic technical guide for the design of a buck converter using the MAX17632 for smaller size. Refer to the MAX17632 IC data sheet and MAX175632A EV kit data sheet for device operation details. The converter design has been built and tested, details of which follow later in this document.

MAXREFDES1198 hardware.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	4.5V	36V
Frequency	f_{SW}	400kHz	
Maximum Efficiency	η	91%	
Output Voltage	V_{OUT}	3.3V	
Output Voltage Ripple	ΔV_{OUT}	33mV	
Output Current	I_{OUT}	0	2A
Output Power	P_{OUT}	6.6W	

Operation of a Buck Converter

The buck power converter is a DC-DC converter whose output voltage is less than the input voltage. This is a non-isolated topology, which means the input and output share a common ground. Figure 2 shows the basic circuit of the synchronous buck power converter. The difference between synchronous buck and traditional buck is that in a synchronous buck, a transistor NL is placed in parallel to the diode to reduce the voltage drop and, therefore, to increase the efficiency.

A buck power converter has the following components:

- Input capacitor (C_{IN}) and output capacitor (C_{OUT})
- A switch, in this case a transistor NH
- An energy storage element, inductor (L)
- Transistor NL and diode D1 to conduct during the off-state of the switch

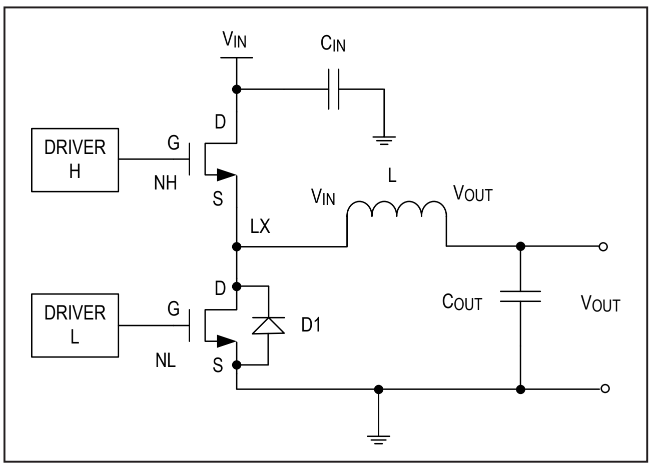

Figure 2. Synchronous buck converter.

Figure 3 shows the basic operation of the buck power converter. During the on-state (t_{ON}) of the transistor NH, the voltage at the node LX is equal to V_{IN} and then the current across the inductor rises linearly at a rate of (V_{IN} - V_{OUT})/L. When the transistor NH is off (t_{OFF}), the voltage at the LX node is 0V and the current in the inductor falls linearly. It is the property of the inductor to maintain the flow of the current, so this reverses the polarity of the inductor during the NH off-state. The current through the inductor never falls to zero. This is called Continuous Conduction Mode (CCM). The ripple current ΔI is an important parameter that is approximately 20 percent to 50 percent of I_L (load current).

Design Procedure

Now that the theory behind the synchronous buck is explained, a practical design technique can now be illustrated. The design procedure involves the following stages: output voltage selection, inductor and capacitor selection, and setup of the switching frequency. This document is intended to complement the information contained in the MAX17632 IC data sheet.

SYMBOL	FUNCTION
V_{IN}	Input voltage
V_{FB}	Feedback threshold voltage
V_{OUT}	Output voltage
ΔV_{OUT}	Output ripple voltage
I_{OUT}	Output current
η	Target minimum efficiency
P_{IN}	Input power
f_{SW}	Switching frequency
D	Duty cycle

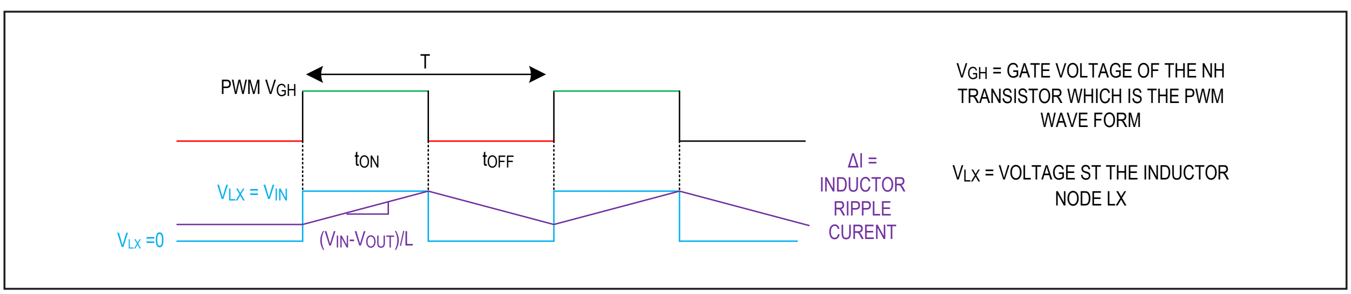

Figure 3. Basic timing wave form showing the PWM voltage and the voltage and current at the LX node.

The following design parameters are used throughout:

Step 1: Setting the Output Voltage

The MAX17632's output voltage can be adjusted between 0.9V and 0.9 × V_{IN}. The output using the R3 and R4 resistors connected to the FB pin is calculated as follows:

$$R3 = \left(\frac{216}{f_C \times C_{OUT}}\right)$$

$$R4 = \left(\frac{R3 \times 0.9}{(V_{OUT} - 0.9)}\right)$$

In this design since the output voltage is 3.3 volts we are considering R3 = 0Ω and R4 = open circuit. Refer to Typical applications circuits in MAX17632 data sheet.

Step 2: Setting the Switching Frequency

The MAX17632 can operate between 400kHz and 2.2MHz. The RT pin is used to set the regulator's switching frequency. The RT pin is left unconnected, which defaults to 400kHz. This is calculated using the following formula:

$$R_{RT} = \frac{21000}{f_{SW}} - 1.7$$

where R_{RT} is in kΩ and f_{SW} is in kHz. The switching frequency f_{SW} = 400kHz is chosen here

Step 3: Selecting the Output Inductor

The LX pin is connected to the switching node of the inductor. The value of the inductor is calculated as follows:

$$L = \frac{V_{OUT}}{1.25 \times f_{SW}}$$

where V_{OUT} = 3.3V, f_{SW} = 400kHz, and L = 6.8µH are chosen for this design.

Step 4: Selecting the Output and Soft-Start Capacitor

The soft-start feature ramps up the output voltage slowly, reducing input inrush current during startup. A capacitor connected from SS to SGND determines the soft-start. This soft capacitor depends upon the output capacitor. The output capacitance can be calculated as follows:

$$C_{OUT} = \left(\frac{1}{2} \times \left(\frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}\right)\right)$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C}\right)$$

where I_{STEP} is the load current step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, f_C is the target closed-loop crossover frequency, and f_{SW} is the switching frequency. Choose f_C to be 1/10 of f_{SW} because in this design the switching frequency is less than 800kHz (refer to the MAX17632 data sheet for more information).

Substitute the following values in the above equations:

I_{STEP} = 1A

ΔV_{OUT} = 0.33V

f_C = (400k/10)

f_{SW} = 400kHz

$t_{RESPONSE}$ = 8.3µs

C_{OUT} = 42µF

Hence, two 22µF capacitors are selected in parallel for the nominal value.

The soft-start capacitance (CSS) is calculated as follows:

C_{SS} ≥ 28 x 10-6 × C_{OUT} × V_{OUT}

C_{OUT} is the selected output capacitance:

C_{SS} ≥ 28 x 10-6 × 44 × 10-6 × 4

C_{SS} ≥ 28 x 10-6 × 44 × 10-6 × 4

where C_{SS} ≥ 4.066nF. C_{SS} = 5600pF is considered the nominal value.

Step 5: Setting the Undervoltage Lockout (UVLO)

UVLO is a technique used to shut down the power to the IC when the input voltage is less than operational value. R1 and R2 are used to set the UVLO of the converter. In this design the pin is connected to V_{IN} pins for always-on operation

Step 6: Compensation

The MAX17632 is internally compensated.

Step 7: Input Capacitor Selector

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

Substituting the values:

$I_{OUT(MAX)}$ = 2A

V_{IN} = 24V

V_{OUT} = 3.3V

I_{RMS} = 0.688A

Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

Substituting the values:

$$I_{OUT(MAX)} = 2A$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

$$D = \frac{3.3}{24} = 0.1375$$

$$\eta = 91\%$$

$$f_{SW} = 400kHz$$

$$\Delta V_{IN} = 45mV$$

where the input capacitor = 2.2μF. As suggested in the data sheet page 19 input capacitor selection an electrolytic capacitor of 47μF is added in parallel.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/18	Initial release	—