Five-Output, No-Opto Flyback DC-DC Converter Using the MAX17690

MAXREFDES1194

Introduction

The MAXREFDES1194 is a no-opto flyback DC-DC power supply that delivers five outputs from a 6V to 60V supply voltage. It is designed for equipment that needs multichannel, isolated power supplies with a wide input voltage range.

The MAXREFDES1194 employs the no-opto flyback control technique of the MAX17690. This document explains how the MAX17690 peak current-mode PWM converter can be used to generate five isolated outputs from a 6V to 60V input voltage. An overview of the design specification is shown in Table 1.

Due to its simplicity and low cost, the flyback converter is the preferred choice for low-to-medium isolated DC-DC power-conversion applications. However, the use of an optocoupler or an auxiliary winding on the flyback transformer for voltage feedback across the isolation barrier increases the number of components and design complexity. The MAX17690 eliminates the need for an optocoupler or auxiliary transformer winding and achieves ±5% output voltage regulation over line, load, and temperature variations.

The MAX17690 implements an innovative algorithm to accurately determine the output voltage by sensing the reflected voltage across the primary winding during the flyback time interval. By sampling and regulating this reflected voltage when the secondary current is close to zero, the effects of secondary-side DC losses in the transformer winding, the PCB tracks, and the rectifying diode on output voltage regulation can be minimized. The MAX17690 also compensates for the negative temperature coefficient of the rectifying diode.

Other features include the following:

- 4.5V to 60V Input Voltage Range
- Programmable Switching Frequency from 50kHz to 250kHz
- Programmable Input Enable/UVLO Feature
- Programmable Input Overvoltage Protection
- Adjustable Soft-Start
- 2A/4A Peak Source/Sink Gate Drive Capability
- Hiccup Mode Short-Circuit Protection
- Fast Cycle-by-Cycle Peak Current Limit
- Thermal Shutdown Protection
- Space-Saving, 16-Pin, 3mm x 3mm TQFN Package
- -40°C to +125°C Operating Temperature Range

Hardware Specification

An isolated no-opto flyback DC-DC converter using the MAX17690 is demonstrated for a five-output application. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Voltage	V_{IN}	6V	24V	60V
Frequency	f_{SW}	200kHz		
Maximum Efficiency	η_{MAX}	65.28%		
Duty Cycle	d	0.04	0.25	0.65
Output Voltage 1	V_{OUT1}	3V	3.3V	3.6V
Output Current 1	I_{OUT1}	0mA	—	50mA
Output Voltage 2	V_{OUT2}	10V	11V	12V
Output Current 2	I_{OUT2}	20mA	—	50mA
Output Voltage 3	V_{OUT3}	9V	10V	11V
Output Current 3	I_{OUT3}	0.2mA	—	0.3mA
Output Voltage 4	V_{OUT4}	10V	11V	12V
Output Current 4	I_{OUT4}	28mA	—	33mA
Output Voltage 5	V_{OUT5}	9V	10V	11V
Output Current 5	I_{OUT5}	0.2mA	—	0.3mA

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing an isolated no-opto flyback DC-DC converter using the MAX17690 controller. The power supply has been built and tested.

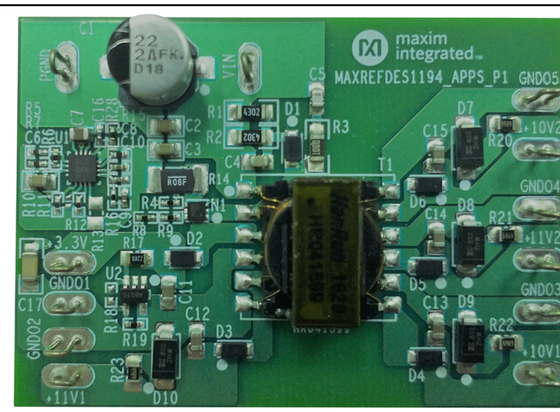

Figure 1. MAXREFDES1194 hardware.

The Isolated No-Opto Flyback Converter

One of the drawbacks encountered in most isolated DC-DC converter topologies is that information relating to the output voltage on the isolated secondary side of the transformer must be communicated back to the primary side to maintain output voltage regulation. In a regular isolated flyback converter, this is normally achieved using an optocoupler feedback circuit or an additional auxiliary winding on the flyback transformer. Optocoupler feedback circuits reduce overall power-supply efficiency, and the extra components increase the cost and physical size of the power supply. In addition, optocoupler feedback circuits are difficult to design reliably due to their limited bandwidth, nonlinearity, high current transfer ratio (CTR) variation, and aging effects. Feedback circuits employing auxiliary transformer windings also exhibit deficiencies. Using an extra winding adds to the flyback transformer's complexity, physical size, and cost, while load regulation and dynamic response are often poor.

The MAX17690 is a peak current-mode controller designed specifically to eliminate the need for optocoupler or auxiliary transformer winding feedback in the traditional isolated flyback topology, thereby reducing size, cost, and design complexity. It derives information about the isolated output voltage by examining the voltage on the primary-side winding of the flyback transformer.

Other than this uniquely innovative method for regulating the output voltage, the no-opto isolated flyback converter using the MAX17690 follows the same general design process as a traditional flyback converter. To understand the operation and benefits of the no-opto flyback converter, it is useful to review the schematic and typical waveforms of the traditional flyback converter (using the MAX17595) shown in Figure 2.

The simplified schematic in Figure 2 illustrates how information about the output voltage is obtained across the isolation barrier in traditional isolated flyback converters. The optocoupler feedback mechanism requires at least 10 components, including an optocoupler and a shunt regulator, in addition to a primary-side bias voltage (V_{BIAS}) to drive the phototransistor. The error voltage FB2 connects to the FB pin of the flyback controller.

The transformer feedback method requires an additional winding on the primary side of the flyback transformer, a diode, a capacitor, and two resistors to generate a voltage proportional to the output voltage. This voltage is compared to an internal reference in a traditional flyback controller to generate the error voltage.

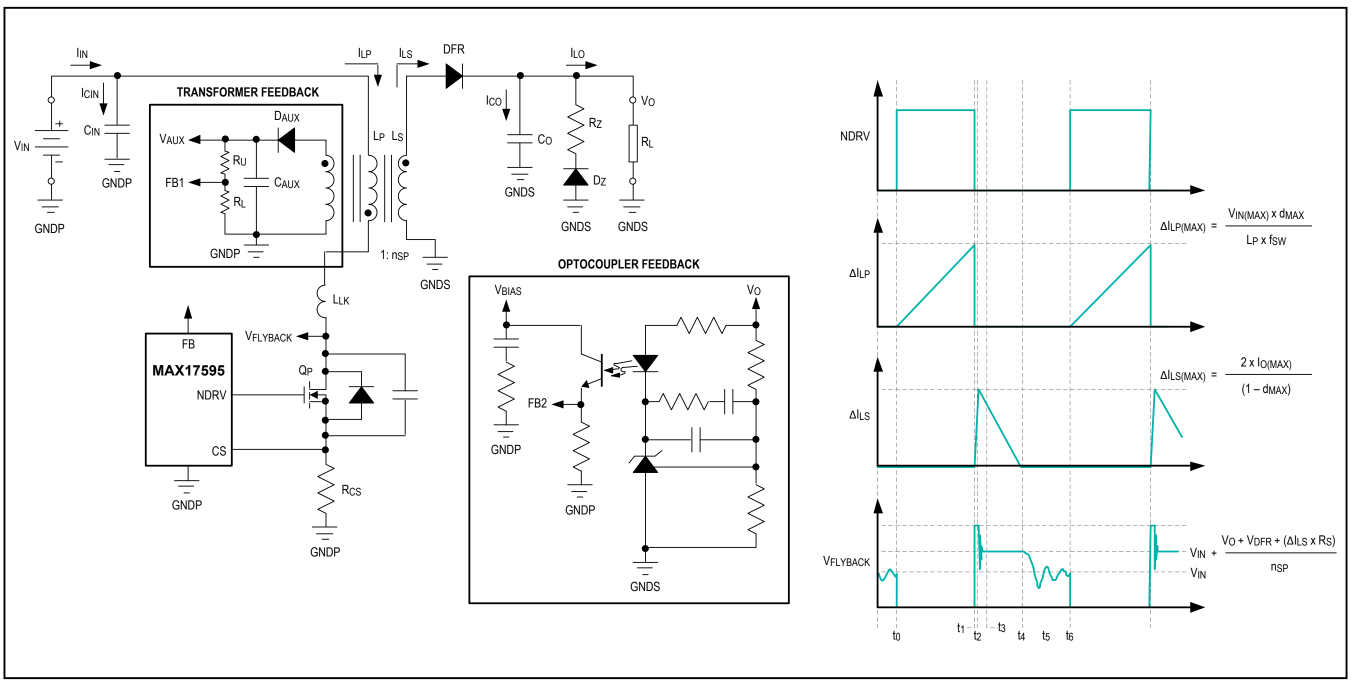

Figure 2. Isolated flyback converter topology with typical waveforms.

By including additional innovative features internally in the MAX17690 no-opto flyback controller, Maxim has enabled power-supply designers to eliminate the additional components, board area, complexity, and cost associated with both the optocoupler and transformer feedback methods. Figure 3 illustrates a simplified schematic and typical waveforms for an isolated no-opto flyback DC-DC converter using the MAX17690.

By comparing Figure 3 with Figure 2, it is evident that there is no difference in the voltage and current waveforms in the traditional and no-opto flyback topologies. The difference is in the control method used to maintain V_O at its target value over the required load, line, and temperature range. The MAX17690 achieves this with minimum components by forcing the voltage $V_{FLYBACK}$ during the conduction period of DFR to be precisely the voltage required to maintain a constant V_O. When Q_P turns off, DFR conducts and the drain voltage of Q_P rises to a voltage $V_{FLYBACK}$ above V_{IN}. After initial ringing due to transformer leakage inductance, and the junction capacitance of DFR and output capacitance of Q_P, the voltage $V_{FLYBACK}$ is given by:

$$V_{FLYBACK} = V_{IN} + \frac{\left(V_O + V_{DFR}(T) + I_{LS}(t) \times R_S(T)\right)}{n_{SP}}$$

where:

$V_{FLYBACK}$ is the Q_P drain voltage relative to primary ground.

$V_{DFR}(T)$ is the forward voltage drop of DFR, which has a negative temperature coefficient.

$I_{LS}(t)$ is the instantaneous secondary transformer current

$R_S(T)$ is the total DC resistance of the secondary circuit, which has a positive temperature coefficient.

n_{SP} is the secondary to primary turns ratio of the flyback transformer.

The voltage of interest is ($V_{FLYBACK}$ - V_{IN}), since this is a measure of V_O. An internal voltage to current amplifier generates a current proportional to ($V_{FLYBACK}$ - V_{IN}). This current then flows through R_{SET} to generate a ground referenced voltage (V_{SET}) proportional to ($V_{FLYBACK}$ - V_{IN}). This requires that:

$$\frac{V_{FLYBACK} - V_{IN}}{R_{FB}} = \frac{V_{SET}}{R_{SET}}$$

Combining this equation with the previous equation for $V_{FLYBACK}$, we have:

$$V_O = V_{SET} \times \left(\frac{R_{FB}}{R_{SET}}\right) \times n_{SP} - V_{DFR}(T) - I_{LS}(t) \times R_S(T)$$

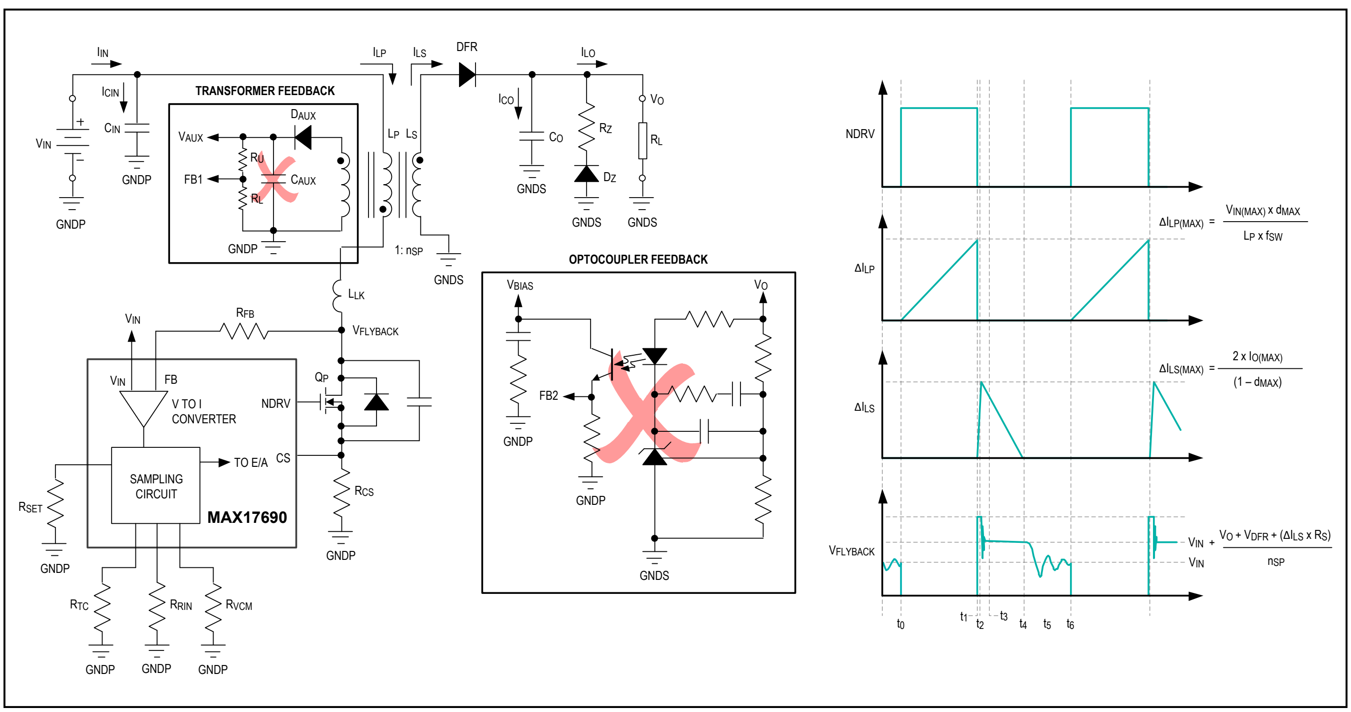

Figure 3. Isolated no-opto flyback converter topology with typical waveforms.

Temperature Compensation

We need to consider the effect of the temperature dependence of V_{DFR} and the time dependence of I_{LS} on the control system. If $V_{FLYBACK}$ is sampled at a time when I_{LS} is very close to zero, then the term $I_{LS}(t) \times R_S(T)$ is negligible and can be assumed to be zero in the previous expression. This is the case when the flyback converter is operating in, or close to, discontinuous conduction mode. It is very important to sample the $V_{FLYBACK}$ voltage before the secondary current reaches zero, since there is a very large oscillation on $V_{FLYBACK}$ due to the resonance between the primary magnetizing inductance of the flyback transformer and the output capacitance of Q_P as soon as the current reaches zero in the secondary, as shown in Figure 2 and Figure 3. The time at which $V_{FLYBACK}$ is sampled is set by resistor R_{VCM}.

The V_{DFR} term has a significant negative temperature coefficient that must be compensated to ensure acceptable output voltage regulation over the required temperature range. This is achieved by internally connecting a positive temperature coefficient current source to the V_{SET} pin. The current is set by resistor R_{TC} connected to ground. The simplest way to understand the temperature compensation mechanism is to think about what needs to happen in the control system when temperature increases. In an uncompensated system, as the temperature increases, V_{DFR} decreases due to its negative temperature coefficient. Since V_{DFR} decreases, V_O increases by the same amount, therefore $V_{FLYBACK}$ remains unchanged. Since V_{SET} is proportional to $V_{FLYBACK}$, V_{SET} also remains unchanged. Since there is no change in V_{SET}, there is no change in duty cycle demand to bring V_O back down to its target value.

What needs to happen in the temperature compensated case is, when V_O increases due to the negative temperature coefficient of V_{DFR}, V_{SET} needs to increase by an amount just sufficient to bring V_O back to its target value. This is achieved by designing V_{SET} with a positive temperature coefficient. This is expressed mathematically as:

$$\frac{\delta V_{DFR}}{\delta T} \times \frac{1}{n_{SP}} + \frac{\delta V_{TC}}{\delta T} \times \frac{R_{FB}}{R_{TC}} = 0$$

where:

$\delta V_{DFR}/\delta T$ is the diode's forward temperature coefficient

$\delta V_{TC}/\delta T = 1.85mV/°C$

$V_{TC} = 0.55V$ is the voltage at the TC pin at +25°C.

Rearranging the above expression gives:

$$R_{TC} = -R_{FB} \times n_{SP} \times \frac{\delta T}{\delta V_{DFR}} \times \frac{\delta V_{TC}}{\delta T}$$

The effect of adding the positive temperature coefficient current (TC) to the current in R_{FB} is equivalent to adding a positive temperature coefficient voltage in series with V_{DFR} on the secondary side of value:

$$\frac{V_{TC}}{R_{TC}} \times R_{FB} \times n_{SP}$$

Substituting from the previous expression, this becomes:

$$-V_{TC} \times \frac{\delta V_{DFR}}{\delta T} \times \frac{\delta T}{\delta V_{TC}}$$

We can now substitute this expression into the expression for V_O as follows:

$$V_O = V_{SET} \times \left(\frac{R_{FB}}{R_{SET}}\right) \times n_{SP} - V_{DFR} - V_{TC} \times \frac{\delta V_{DFR}}{\delta T} \times \frac{\delta T}{\delta V_{TC}}$$

and finally solve for R_{FB}:

$$R_{FB} = \frac{R_{SET}}{n_{SP} \times V_{SET}} \times \left\{V_O + V_{DFR} + V_{TC} \times \frac{\delta V_{DFR}}{\delta T} \times \frac{\delta T}{\delta V_{TC}}\right\}$$

Values for R_{SET}, V_{SET}, and $\delta V_{TC}/\delta T$ can be obtained from the MAX17690 data sheet as follows:

$R_{SET} = 10k\Omega$

$V_{SET} = 1V$

$\delta V_{TC}/\delta T = 1.85mV/°C$

Values for V_{DFR} and $\delta V_{DFR}/\delta T$ can be obtained from the output diode data sheet, and n_{SP} is calculated when the flyback transformer is designed.

The value of R_{TC} can then be calculated using the expression from earlier, restated below:

$$R_{TC} = -R_{FB} \times n_{SP} \times \frac{\delta T}{\delta V_{DFR}} \times \frac{\delta V_{TC}}{\delta T}$$

The calculated resistor values for R_{FB} and RT_C should always be verified experimentally and adjusted, if necessary, to achieve optimum performance over the required temperature range. Note that the reference design described in this document has only been verified at room temperature.

Finally, the internal temperature compensation circuitry requires a current proportional to V_{IN}. R_{RIN} should be chosen as approximately:

$$R_{RIN} = 0.6 \times R_{FB}$$

Setting the $V_{FLYBACK}$ Sampling Instant

The MAX17690 generates an internal voltage proportional to the on-time, volt-second product. This enables the device to determine the correct sampling instant for $V_{FLYBACK}$ during the Q_P off-time. The R_{VCM} resistor is used to scale this internal voltage to an acceptable internal voltage limit in the device. Selection of this resistor is described in detail in the MAX17690 data sheet.

Design Procedure for the No-Opto Flyback Converter MAX17690

Now that the principle difference between a traditional isolated flyback converter using optocoupler or auxiliary transformer winding feedback and the isolated no-opto flyback converter using the MAX17690 is understood, a practical design example can be illustrated. The converter design process can be divided into three parts: the power stage design, the setup of the MAX17690 no-opto flyback controller, and closing the control loop. This document is intended to complement the information contained in the MAX17690 data sheet.

The following design parameters are used throughout this document:

SYMBOL	FUNCTION
V_{IN}	Input voltage
V_{UVLO}	Undervoltage turn-on threshold
V_{OVI}	Overvoltage turn-off threshold
t_{SS}	Soft-start time
V_O	Output voltage
$\Delta V_{O(SS)}$	Steady-state output ripple voltage
I_O	Output current
$I_{O(CL)}$	Maximum current-limit threshold
P_O	Nominal output power
$\eta_{(MAX)}$	Target efficiency at maximum load
$\eta_{(MIN)}$	Target efficiency at minimum load
P_{IN}	Input power
f_{SW}	Switching frequency
d	Duty cycle
n_{SP}	Secondary-primary turns ratio

These symbols are sometimes followed by parentheses to indicate whether minimum or maximum values of the parameters are intended, for example, the symbol $V_{IN(MIN)}$ is the minimum input voltage. In addition, throughout the design procedure, reference is made to the schematic.

Step 1: Choose a Maximum Duty Cycle

The maximum duty cycle (d_{MAX}) occurs at maximum output power ($P_{O(MAX)}$) and minimum input voltage ($V_{IN(MIN)}$) The MAX17690 no-opto flyback controller uses peak current-mode control. Switching power converters using peak current-mode control exhibit subharmonic oscillations at duty cycles greater than 50% unless slope compensation is added to the sensed primary MOSFET current. Slope compensation is added internally in the MAX17690 to allow stable operation up to duty cycles of 66%, as specified in the data sheet. Choosing the maximum allowable duty cycle ensures the highest energy density for the power converter. For the current design, we have chosen:

$$d_{MAX} = 0.65$$

Step 2: Calculate the Minimum Duty Cycle

The MAX17690 derives the current (ΔI_{LP}) in the primary magnetizing inductance by measuring the voltage (ΔV_{RCS}) across the current-sense resistor (R_{CS}) during the on-time of the MOSFET. So:

$$\Delta I_{LP} = \frac{\Delta V_{RCS}}{R_{CS}}$$

ΔI_{LP} is a maximum at d_{MAX} and $V_{IN(MIN)}$ and is a minimum at d_{MIN} and $V_{IN(MAX)}$ so:

$$\frac{V_{IN(MIN)}}{L_P} = \frac{\Delta V_{RCS(MAX)} \times f_{SW}}{R_{CS} \times d_{MAX}}$$

and

$$\frac{V_{IN(MAX)}}{L_P} = \left(\frac{\eta_{MAX}}{\eta_{MIN}} \times \frac{\Delta V_{RCS(MIN)}}{R_{CS}} \right) \times \frac{f_{SW}}{d_{MIN}}$$

Solving the two equations above, we have:

$$d_{MIN} = d_{MAX} \times \frac{\eta_{MAX}}{\eta_{MIN}} \times \frac{V_{IN(MIN)}}{V_{IN(MAX)}} \times \frac{\Delta V_{RCS(MIN)}}{\Delta V_{RCS(MAX)}}$$

where $\Delta V_{RCS(MIN)}$ and $\Delta V_{RCS(MAX)}$ correspond to the minimum current-limit threshold (20mV) and the maximum current-limit threshold (100mV) of the MAX17690, respectively. So, for $V_{IN(MIN)}$ = 6V, $V_{IN(MAX)}$ = 60V, and d_{MAX} = 0.65, we have:

$$d_{MIN} \approx 0.04$$

Step 3: Calculate the Maximum Allowable Switching Frequency

The isolated no-opto flyback topology requires the primary side MOSFET to constantly maintain switching, otherwise there is no way to sense the reflected secondary-side voltage at the drain of the primary-side MOSFET. The MAX17690 achieves this by having a critical minimum on-time ($t_{ON(CRIT)}$) for which it drives the MOSFET. At a given switching frequency, $t_{ON(MIN)}$ corresponds to d_{MIN}. From the data sheet, $t_{ON(CRIT)}$ for the MOSFET drive output NDRV is 235ns. We can therefore calculate the maximum switching frequency ($f_{SW(MAX)}$) as follows:

$$f_{SW(MAX)} = \frac{d_{MIN}}{t_{ON(CRIT)}} \approx 170{,}200\text{Hz}$$

Since d_{MIN} is fixed by $\Delta V_{RCS(MIN)}$, $\Delta V_{RCS(MAX)}$, d_{MAX}, $V_{IN(MIN)}$, and $V_{IN(MAX)}$, we can choose a $t_{ON(MIN)}$, which is arbitrarily larger than $t_{ON(CRIT)}$ to allow a reasonable design margin. So, if we choose $t_{ON(MIN)}$ = 400ns, we obtain a new switching frequency as follows:

$$f_{SW} = \frac{d_{MIN}}{t_{ON(MIN)}} \approx 100{,}000\text{Hz}$$

Note that the MAX17690 should always be operated in the switching frequency range from 50kHz to 250kHz and $t_{ON(MIN)}$ must be chosen accordingly to ensure that this constraint is met.

Step 4: Calculate Primary Magnetizing Inductance

Maximum input power ($P_{IN(MAX)}$) is given by:

$$P_{IN(MAX)} = \frac{P_{O(MAX)}}{\eta_{MAX}} = \frac{V_O \times I_{O(CL)}}{\eta_{MAX}}$$

For the discontinuous flyback converter, all of the energy stored in the primary magnetizing inductance (L_P) during the MOSFET on-time is transferred to the output during the MOSFET off-time (i.e., the full power transfer occurs during one switching cycle). Therefore, because E = P x t, we have:

$$E_{IN(MAX)} = P_{IN(MAX)} \times \tau_{SW} = \frac{V_O \times I_{O(CL)}}{\eta_{MAX} \times f_{SW}}$$

The maximum input energy must be stored in L_P during the on-time of the MOSFET, so:

$$E_{IN(MAX)} = \frac{1}{2} \times L_P \times \Delta I_{LP(MAX)}{}^2$$

We also know that the peak current in L_P ($\Delta I_{LP(MAX)}$) occurs at input voltage $V_{IN(MIN)}$ and MOSFET on-time $t_{ON(MAX)}$. So:

$$V_{IN(MIN)} = L_P \times \frac{\Delta I_{LP(MAX)}}{t_{ON(MAX)}}$$

Rearranging this equation and squaring, we have:

$$\Delta I_{LP(MAX)}{}^2 = \frac{V_{IN(MIN)}{}^2 \times t_{ON(MAX)}{}^2}{L_P{}^2}$$

and substituting:

$$E_{IN(MAX)} = \frac{V_{IN(MIN)}{}^2 \times t_{ON(MAX)}{}^2}{2 \times L_P}$$

we now have:

$$\frac{V_{IN(MIN)}{}^2 \times t_{ON(MAX)}{}^2}{2 \times L_P} = \frac{V_O \times I_{O(CL)}}{\eta_{MAX} \times f_{SW}}$$

Finally, by rearranging, we have an expression for L_P:

$$L_P = \frac{\eta_{MAX} \times V_{IN(MIN)}{}^2 \times d_{MAX}{}^2}{2 \times V_O \times I_{O(CL)} \times f_{SW}}$$

If we estimate the power converter efficiency η_{MAX} = 0.65, then with $V_{IN(MIN)}$ = 6V, d_{MAX} = 0.65, V_{O1} = 3.3V, $I_{O1(CL)}$ = 60mA, V_{O2} = 11V, $I_{O2(CL)}$ = 60mA, V_{O3} = 10V, $I_{O3(CL)}$ = 1mA, V_{O4} = 11V, $I_{O4(CL)}$ = 40mA, V_{O5} = 10V, $I_{O5(CL)}$ = 1mA, and f_{SW} = 100kHz, we have:

$$L_{P(MAX)} \approx 49\mu\text{H}$$

This primary inductance represents the maximum primary inductance since it sets the current-limit threshold. Choosing a larger inductance will set the current-limit threshold at a lower value which would be undesirable. Assuming a ±10% tolerance for the primary inductance gives:

$$L_P \approx 40\mu\text{H} \pm 10\%$$

Step 5: Calculate the Secondary to Primary Turns Ratio for the Flyback Transformer

Assume we are operating at the border between discontinuous and continuous conduction modes at $V_{IN(MIN)}$ and $P_{O(MAX)}$. Under this condition, the primary-side MOSFET is conducting for (d_{MAX} x τ_{SW}) and the secondary-side synchronous rectifier (or diode) is conducting for (1 - d_{MAX}) x τ_{SW}. Ideally, the primary volt-seconds per turn must balance with the secondary volt-seconds per turn. However, in practice, the primary to secondary coupling of the transformer is not perfect (giving rise to uncoupled leakage inductance) and both windings have series resistance. Effectively, this means that to obtain the required volt-seconds per turn on the secondary winding we need more volt-seconds per turn on the primary winding. We introduce a transformer efficiency factor (η_T) so that:

$$\frac{V_{IN(MIN)} \times d_{MAX} \times \tau_{SW}}{\eta_T \times N_P} = \frac{(V_O + V_F) \times (1 - d_{MAX}) \times \tau_{SW}}{N_S}$$

and

$$n_{SP} = \frac{N_S}{N_P} = \frac{\eta_T \times (V_O + V_F) \times (1 - d_{MAX})}{V_{IN(MIN)} \times d_{MAX}}$$

Assuming η_T = 0.9 and V_F = 0.5V (for a synchronous rectifier), then with V_{O1} = 3.3V, V_{O2} = 11V, V_{O3} = 10V, V_{O4} = 11V, V_{O5} = 10V, d_{MAX} = 0.65, and $V_{IN(MIN)}$ = 6V, we have:

$$n_{S1P} \approx 0.31$$

$$n_{S2P} \approx 0.93$$

$$n_{S3P} \approx 0.85$$

$$n_{S4P} \approx 0.93$$

$$n_{S5P} \approx 0.85$$

Typical values of η_T range from 0.65 for an inefficient transformer design to 0.95 for a very efficient transformer design.

Step 6: Calculate Peak and RMS Currents in the Primary Winding of the Flyback Transformer

The peak primary winding current occurs at $V_{IN(MIN)}$ and d_{MAX} according to the following equation:

$$\Delta I_{LP(MAX)} = \frac{V_{IN(MIN)} \times d_{MAX}}{L_P \times f_{SW}} \approx 0.975A$$

The RMS primary winding current can be calculated from $\Delta I_{LP(MAX)}$ and d_{MAX} as follows:

$$I_{LP(RMS)} = \Delta I_{LP(MAX)} \times \sqrt{\frac{d_{MAX}}{3}} \approx 0.454A$$

Step 7: Calculate Peak and RMS Currents in the Secondary Winding of the Flyback Transformer

Again, assuming we are operating at the border between discontinuous and continuous conduction modes at $V_{IN(MIN)}$ and $P_{O(MAX)}$, the peak secondary winding current is related to $I_{O(MAX)}$ and d_{MAX} as follows:

$$\Delta I_{LS1(MAX)} = \frac{2 \times I_{O1(MAX)}}{(1 - d_{MAX})} \approx 286mA$$

$$\Delta I_{LS2(MAX)} = \frac{2 \times I_{O2(MAX)}}{(1 - d_{MAX})} \approx 286mA$$

$$\Delta I_{LS3(MAX)} = \frac{2 \times I_{O3(MAX)}}{(1 - d_{MAX})} \approx 1.72mA$$

$$\Delta I_{LS4(MAX)} = \frac{2 \times I_{O4(MAX)}}{(1 - d_{MAX})} \approx 189mA$$

$$\Delta I_{LS5(MAX)} = \frac{2 \times I_{O5(MAX)}}{(1 - d_{MAX})} \approx 1.72mA$$

The RMS secondary winding current can be calculated from $\Delta I_{LS(MAX)}$ and d_{MAX} as follows:

$$I_{S1(RMS)} = \Delta I_{LS1(MAX)} \times \sqrt{\frac{(1 - d_{MAX})}{3}} \approx 98mA$$

$$I_{S2(RMS)} = \Delta I_{LS2(MAX)} \times \sqrt{\frac{(1 - d_{MAX})}{3}} \approx 98mA$$

$$I_{S3(RMS)} = \Delta I_{LS3(MAX)} \times \sqrt{\frac{(1 - d_{MAX})}{3}} \approx 0.59mA$$

$$I_{S4(RMS)} = \Delta I_{LS4(MAX)} \times \sqrt{\frac{(1 - d_{MAX})}{3}} \approx 65mA$$

$$I_{S5(RMS)} = \Delta I_{LS5(MAX)} \times \sqrt{\frac{(1 - d_{MAX})}{3}} \approx 0.59mA$$

Step 8: Calculate Design Parameters for a Secondary Diode

In a flyback converter, because the secondary diode is reverse biased when the primary MOSFET is conducting, the voltage stress on the diode is the sum of the output voltage and the reflected primary voltage. Choosing the diode with enough margin for the reverse blocking voltage, as indicated in the following equation, should preclude the use of a snubber.

$$V_{SEC,DIODE1} = 1.5 \text{ x } (n_{S1P} \text{ x } V_{IN(MAX)} + V_{O1}) \approx 33V$$
$$V_{SEC,DIODE2} = 1.5 \text{ x } (n_{S2P} \text{ x } V_{IN(MAX)} + V_{O2}) \approx 100V$$
$$V_{SEC,DIODE3} = 1.5 \text{ x } (n_{S3P} \text{ x } V_{IN(MAX)} + V_{O3}) \approx 92V$$
$$V_{SEC,DIODE4} = 1.5 \text{ x } (n_{S4P} \text{ x } V_{IN(MAX)} + V_{O4}) \approx 100V$$
$$V_{SEC,DIODE5} = 1.5 \text{ x } (n_{S5P} \text{ x } V_{IN(MAX)} + V_{O5}) \approx 92V$$

Select a diode with low forward-voltage drop to minimize the power loss (given as the product of forward-voltage drop and the average output current) in the diode. Select fast-recovery diodes with a recovery time of less than 50ns or Schottky diodes with low junction capacitance for this purpose.

Step 9: Calculate Design Parameters for Primary-Side MOSFET

The important parameters to consider for the primary-side MOSFET (Q_P) are peak instantaneous current, RMS current, voltage stress, and power losses. Because Q_P and L_P are in series, they experience the same peak and RMS currents, so from Step 6:

$$I_{QP(MAX)} = I_{LP(MAX)} \approx 0.975A$$

and

$$I_{QP(RMS)} = I_{LP(RMS)} \approx 0.454A$$

When Q_P turns off, V_O is reflected to the primary side of the flyback transformer plus $V_{IN(MAX)}$ is applied across the drain-source of Q_P. In addition, until Q_S starts to conduct, there is no path for the leakage inductance energy to flow through. This causes the drain-source voltage of Q_P to rise even further. The factor of 1.5 in the following equation represents this additional voltage rise; however, this factor can be higher or lower depending on the transformer and PCB leakage inductances:

$$V_{QP(MAX)} \approx 1.5 \times \left(\frac{V_{O1} + V_{DS}}{n_{S1P}} \right) + V_{IN(MAX)} \approx 78.39V$$

Allowing for a reasonable design margin, the ON Semiconductor FDMA86251 was chosen for this design with the following specifications:

PARAMETER	VALUE
Maximum D-S Voltage	150V
Continuous Drain Current	2.4A
Pulsed Drain Current	12A
D-S Resistance at V_{GS} = 7.5V, I_D = 2A	237mΩ
Minimum V_{GS} Threshold V_{GSTH}	2.0V
Typical V_{GS}	6V
Maximum $Q_{G(T)}$	3.8nC
Typical Q_{GD}	1.0nC
Total Output Capacitance C_{OSS}	34pF

The power losses in Q_P can be approximated as follows:

$$P_{TOT} = P_{CON} + P_{CDS} + P_{SW} \approx 60mW$$

where:

P_{CON} is the loss due to $I_{QP(RMS)}$ flowing through the drain-source on-resistance of Q_P:

$$P_{CON} = I_{QP(RMS)}^2 \times R_{DS(ON)} \approx 49mW$$

P_{CDS} is the loss due to the energy in the drain-source output capacitance being dissipated in Q_P at turn-on:

$$P_{CDS} = \frac{1}{2} \times f_{SW} \times C_{OSS} \times V_{QP(MAX)}^2 \approx 11mW$$

And P_{SW} is the turn-on voltage-current transition loss that occurs as the drain-source voltage decreases and the drain current increases during the turn-on transition:

$$P_{SW} = \frac{1}{2} \times f_{SW} \times I_{QP(t-ON)} \times \left\{ \frac{V_{GS(PL)} - V_{GS(TH)}}{V_{GS(PL)}} \times \left(\frac{Q_{G(T)} + Q_{GD}}{I_{DRV}} \right) \right\} \approx 0mW$$

where I_{DRV} is the maximum drive current capability of the NDRV output of the MAX17690 and $I_{QP(t-ON)}$ is the instantaneous current in Q_P at turn-on. Since the flyback converter is operating in discontinuous conduction mode, $I_{QP(t-ON)}$ is zero and therefore P_{SW} is also zero.

Step 10: Select the RCD Snubber Components

Referring to Figure 4, when Q_P turns off, I_{LP} charges the output capacitance (C_{OSS}) of Q_P. When the voltage across C_{OSS} exceeds the input voltage plus the reflected secondary to primary voltage, the secondary-side diode (or synchronous switch) turns on. Since the diode (or synchronous switch) is now on, the energy stored in the primary magnetizing inductance is transferred to the secondary. However, the energy stored in the leakage inductance will continue to charge C_{OSS} since there is nowhere else for it to go. Since the voltage across C_{OSS} is the same as the voltage across Q_P, if the energy stored in the leakage inductance charges C_{OSS} to a voltage level greater than the maximum allowable drain-source voltage of Q_P, the MOSFET fails.

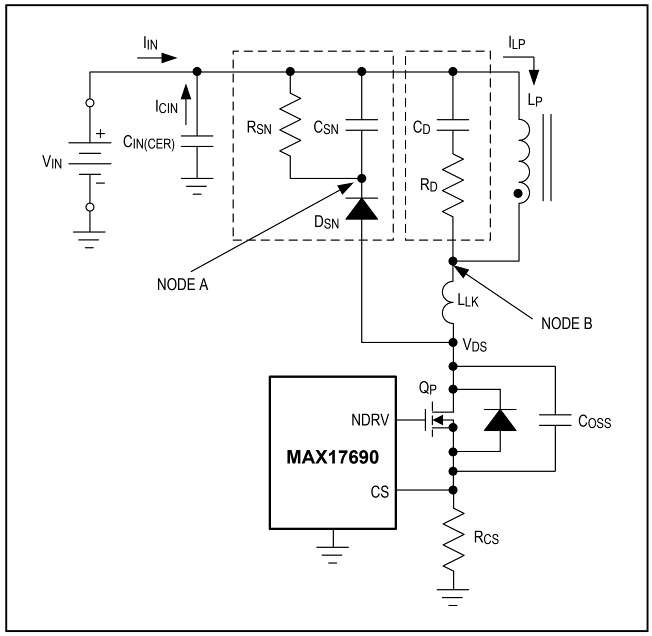

Figure 4. RCD snubber circuit.

One way to avoid this situation is to add a suitable RCD snubber across the primary winding of the transformer. In Figure 4, the snubber is labelled R_{SN}, C_{SN}, and D_{SN}.

In this situation, when Q_P turns off, the voltage at Node A is:

$$V_{NODEA} = V_{CSN} + V_{IN}$$

When the secondary-side diode (or synchronous switch) turns on, the voltage at Node B is:

$$V_{NODEB} = V_{IN} + \frac{V_O + V_F}{n_{SP}}$$

So, the voltage across the leakage inductance is:

$$V_{LLK} = V_{CSN} + V_{IN} - \left(V_{IN} + \frac{V_O + V_F}{n_{SP}} \right)$$

$$= V_{CSN} - \left(\frac{V_O + V_F}{n_{SP}} \right) = L_{LK} \times \frac{\Delta I_{SN}}{\Delta t_{SN}}$$

So:

$$\Delta t_{SN} = \frac{L_{LK} \times \Delta I_{SN}}{V_{CSN} - \left(\frac{V_O + V_F}{n_{SP}}\right)}$$

The average power dissipated in the snubber network is:

$$P_{SN} = V_{CSN} \times \frac{\Delta I_{SN} \times \Delta t_{SN}}{2 \times \tau_{SW}}$$

Substituting Δt_{SN} into this expression, we have:

$$P_{SN} = \frac{1}{2} \times L_{LK} \times \Delta I_{SN}^2 \times \frac{V_{CSN}}{V_{CSN} - \left(\frac{V_O + V_F}{n_{SP}}\right)} \times f_{SW}$$

The leakage inductance energy is dissipated in R_{SN}, so from:

$$P_{SN} = \frac{V_{CSN}^2}{R_{SN}}$$

we can calculate the required R_{SN} as follows:

$$R_{SN} = \frac{V_{CSN}^2}{\frac{1}{2} \times L_{LK} \times \Delta I_{SN}^2 \times \frac{V_{CSN}}{V_{CSN} - \left(\frac{V_O + V_F}{n_{SP}}\right)} \times f_{SW}}$$

Over one switching cycle we must have:

$$I_{SN} = \frac{V_{CSN}}{R_{SN}} = C_{SN} \times \frac{\Delta V_{SN}}{\tau_{SW}}$$

So, we can calculate the required C_{SN} as follows:

$$C_{SN} = \frac{V_{CSN}}{\Delta V_{CSN} \times R_{SN} \times f_{SW}}$$

Generally, ΔV_{CSN} should be kept to approximately 10% to 30% of V_{CSN}. Figure 5 illustrates V_{CSN}, ΔI_{SN}, and Δt_{SN}. The voltage across the snubber capacitor (V_{CSN}) should be selected so that:

$$V_{CSN} < Q_{P(DSMAX)} - V_{IN(MAX)}$$

Choosing too large a value for V_{CSN} causes the voltage on the drain of Q_P to get too close its maximum allowable drain-source voltage, while choosing too small a value results in higher power losses in the snubber resistor. A reasonable value should result in a maximum drain voltage on Q_P that is approximately 75% of its maximum allowable value. The worst-case condition for the snubber circuit occurs at maximum output power when:

$$\Delta I_{SN} = I_{LP(MAX)}$$

Assuming the leakage inductance is 5% of the primary inductance, then choosing V_{CSN} = 50V and ΔV_{CSN} = 2.5V, we get the following approximate values:

P_{SN} = 125mW

R_{SN} = 20kΩ

C_{SN} = 10nF

Finally, we consider the snubber diode (D_{SN}). This diode should have at least the same voltage rating as the MOSFET (Q_P). Although the average forward current is very low, it must have a peak repetitive current rating greater than $I_{LP(MAX)}$.

Step 11: Calculate the Required Current-Sense Resistor

From Step 4, we have the maximum input power given by:

$$P_{IN(MAX)} = \frac{P_{O(MAX)}}{\eta} = \frac{V_O \times I_{O(MAX)}}{\eta}$$

For the discontinuous flyback converter all the energy stored in L_P during the MOSFET on-time is transferred to the output during the MOSFET off-time (i.e., the full power transfer occurs during one switching cycle). Therefore, since E = P x t, we have:

$$E_{IN(MAX)} = P_{IN(MAX)} \times \tau_{SW} = \frac{V_O \times I_{O(MAX)}}{\eta \times f_{SW}}$$

The maximum input energy must be stored in L_P during the on-time of the MOSFET, so:

$$E_{IN(MAX)} = \frac{1}{2} \times L_P \times \Delta I_{LP(MAX)}^2$$

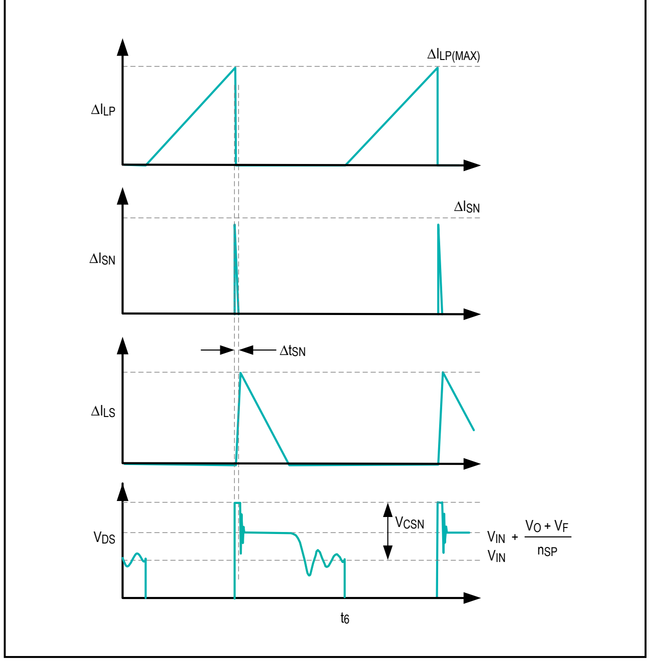

Figure 5. RCD snubber circuit waveforms.

Therefore:

$$\frac{1}{2} \times L_P \times \Delta I_{LP(MAX)}{}^2 = \frac{V_O \times I_{O(MAX)}}{\eta \times f_{SW}}$$

and

$$\Delta I_{LP} = \sqrt{\frac{2 \times V_O \times I_{O(MAX)}}{\eta \times L_P \times f_{SW}}}$$

From Step 2 we have:

$$\Delta I_{LP} = \frac{\Delta V_{RCS}}{R_{CS}}$$

so

$$R_{CS} = \Delta V_{RCS} \times \sqrt{\frac{\eta \times L_P \times f_{SW}}{2 \times V_O \times I_{O(MAX)}}}$$

Substituting values for ΔV_{RCS}, η, L_P, f_{SW}, V_O, and $I_{O(MAX)}$ we have:

$$R_{CS} \approx 103m\Omega$$

where ΔV_{RCS} = 100mV, the maximum CS current-limit threshold of the MAX17690. We can choose a standard 80mΩ resistor for R_{CS}.

Step 12: Calculate and Select the Input Capacitors

Figure 6 shows a simplified schematic of the primary side of the flyback converter and the associated current waveforms. In steady-state operation, the converter draws a pulsed high-frequency current from the input capacitor (C_{IN}). This current leads to a high-frequency ripple voltage across the capacitor according to the following expression:

$$I_{CIN} = C_{IN} \times \frac{\Delta V_{CIN}}{\Delta t}$$

It is the ripple voltage arising from the amp second product through the input capacitor.

During the Q_P on-time interval from t_0 to t_1, the capacitor is supplying current to the primary inductance L_P of the flyback transformer and its voltage is decreasing. During the Q_P off-time time interval from t_1 to t_2, no current is flowing in L_P, and current is being supplied to capacitor from the input voltage source. According to the charge balance law, the decrease in capacitor voltage during time t_0 to t_1 must equal the increase in capacitor voltage during time t_1 to t_2. So:

$$I_{CIN[t_1 \, to \, t_2]} = C_{IN} \times \frac{\Delta V_{CIN}}{(t_2 - t_1)} = \frac{V_O \times I_O}{\eta \times V_{IN}}$$

And finally, since:

$$\frac{1}{(t_2 - t_1)} = \frac{f_{SW}}{(1 - d)}$$

we have:

$$C_{IN} = \frac{V_O \times I_O}{\eta \times V_{IN}} \times \frac{1}{\Delta V_{CIN}} \times \frac{(1 - d)}{f_{SW}}$$

For maximum high-frequency ripple voltage requirement ΔV_{CIN}, we can now calculate the required minimum C_{IN}.

An additional high-frequency ripple voltage occurs at the input due to the ESR of the input capacitor. This ripple voltage is generally much smaller than the amp second product voltage ripple and can be minimized by choosing a capacitor with low ESR.

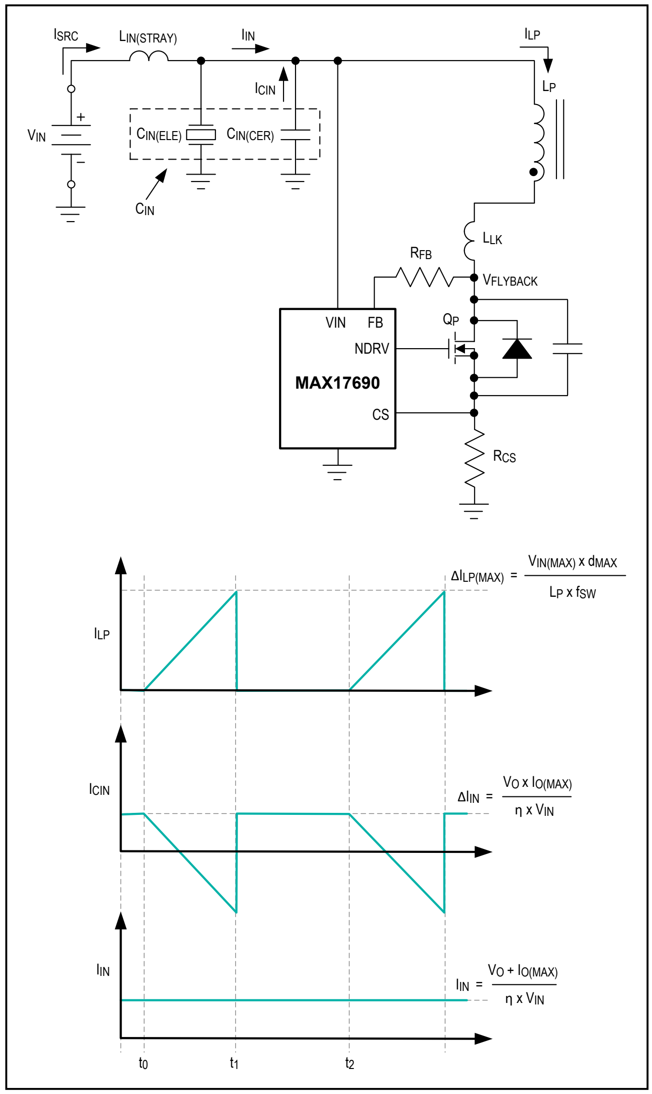

Figure 6. Primary-side circuit and currents.

There is high-frequency AC current flowing in C_{IN}, as shown in the center waveform of Figure 7. The selected capacitor must be specified to tolerate this maximum RMS current ($I_{CIN(RMS)}$). From the simplified schematic:

$$I_{LP} = I_{IN} + I_{CIN}$$

Therefore:

$$I_{CIN(RMS)} = \sqrt{I_{LP(RMS)}^2 - I_{IN(RMS)}^2}$$

where:

$$I_{IN(RMS)} = \frac{V_O \times I_O}{\eta \times V_{IN}}$$

and from Step 6:

$$I_{LP(RMS)} = \Delta I_{LP} \times \sqrt{\frac{d}{3}}$$

So:

$$I_{CIN(RMS)} = \sqrt{\frac{d}{3} \times \Delta I_{LP}^2 - \frac{V_O^2 \times I_O^2}{\eta^2 \times V_{IN}^2}}$$

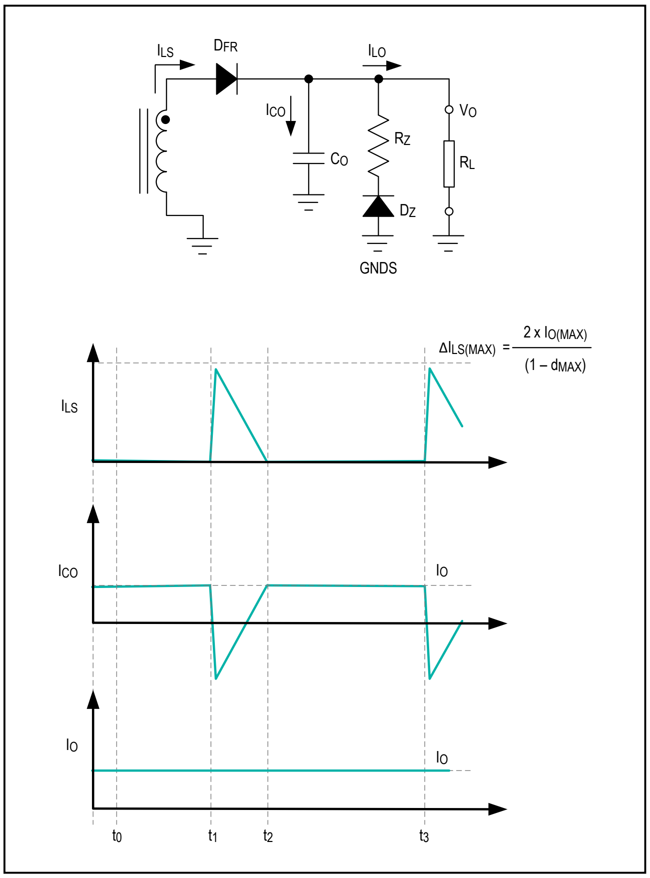

Figure 7. Secondary-side circuit and currents.

The maximum RMS current in the input capacitor occurs at d_{MAX}, $\Delta I_{LP(MAX)}$, $I_{O(MAX)}$, and $V_{IN(MIN)}$.

$$I_{CIN(RMS)} \approx 0.38A_{RMS}$$

An additional high-frequency ripple voltage is present due to the RMS current flowing through the ESR of the capacitor. Ceramic capacitors are generally used for limiting high-frequency ripple due to their high AC current capability and low ESR.

In addition to using a ceramic capacitor for high-frequency input ripple-voltage control as described above, an electrolytic capacitor is sometimes inserted at the input of a flyback converter to limit the input voltage deviation when there is a rapid output load change. A 100% load change gives rise to an input current transient of:

$$\Delta I_{IN(MAX)} = \frac{V_O \times I_{O(MAX)}}{\eta \times V_{IN(MIN)}}$$

During this transient, there is a voltage drop across any series stray inductance ($L_{IN(STRAY)}$) that exists between the input voltage source and the input capacitor of the power supply. So from:

$$\frac{1}{2} \times C_{IN} \times \Delta V_{CIN}^2 = \frac{1}{2} \times L_{IN(STRAY)} \times \Delta I_{CIN}^2$$

we have:

$$C_{IN} = L_{IN(STRAY)} \times \frac{\Delta I_{IN(MAX)}^2}{\Delta V_{CIN}^2}$$

We now have two values for C_{IN}. One for input high-frequency ripple-voltage control:

$$C_{IN(CER)} = \frac{V_O \times I_O}{\eta \times V_{IN}} \times \frac{1}{\Delta V_{CIN}} \times \frac{(1-d)}{f_{SW}}$$

and a second for transient input voltage control:

$$C_{IN(ELE)} = L_{IN(STRAY)} \times \frac{\Delta I_{IN(MAX)}^2}{\Delta V_{CIN}^2}$$

If $C_{IN(ELE)} > C_{IN(CER)}$, both ceramic and electrolytic capacitors must be used at the input of the power supply and ΔV_{CIN} should be limited to approximately 75mV to keep the AC current in the ESR of the electrolytic capacitor within acceptable limits. Otherwise, $C_{IN(ELE)}$ is not required. In this case, the value of $C_{IN(CER)}$ can be significantly reduced since there is no longer any requirement to limit ΔV_{CIN} to less than 60mV. Based on the current design specification, we have:

$$C_{IN(CER)} \approx 14.5\mu F$$

and:

$$C_{IN(ELE)} \approx 23\mu H$$

Since $C_{IN(ELE)} > C_{IN(CER)}$, an electrolytic capacitor is not required. We can now recalculate $C_{IN(CER)}$ based on ΔV_{CIN} = 300mV:

$$C_{IN(CER)} \approx 3\mu F$$

Step 13: Calculate and Select the Output Capacitor

High-frequency ripple voltage requirements are also used to determine the value of the output capacitor in a flyback converter.

Figure 7 shows a simplified schematic of the secondary side of the flyback converter and the associated current waveforms.

In steady-state operation, the load draws a DC current from the secondary side of the flyback converter. By examining the secondary current waveforms, we see that C_O is supplying the full output current (I_O) to the load during the time interval from t_2 to t_3. During this time interval, the voltage across C_O decreases. At time t_3, Q_P has just turned off and the secondary rectifying diode DFR (or the secondary synchronous switch, Q_S) starts to conduct supplying current to the load and to C_O. The charging and discharging of C_O leads to a high-frequency ripple voltage at the output according to the following expression:

$$I_{CO} = C_O \times \frac{\Delta V_{CO}}{\Delta t}$$

Again, as with the input capacitor, this is the ripple voltage arising from the amp second product through the output capacitor.

By the capacitor charge balance law, the decrease in capacitor voltage during time t_2 to t_3 must equal the increase in capacitor voltage during time t_1 to t_2. When the capacitor is discharging, we have:

$$I_{CO[t_2 \text{ to } t_3]} = C_O \times \frac{\Delta V_{CO}}{(t_3 - t_2)} = I_O$$

Finally, since:

$$\frac{1}{(t_3 - t_2)} = \frac{f_{SW}}{d}$$

we have:

$$C_O = I_O \times \frac{1}{\Delta V_{CO}} \times \frac{d}{f_{SW}}$$

At maximum output current, the discontinuous flyback converter should ideally operate on the border between discontinuous and continuous conduction modes and so d_{MAX} should be substituted in the above equation.

For maximum high-frequency ripple voltage requirement ΔV_{CO}, we can now calculate the required minimum C_O:

$$C_{O1} \approx 20\mu F$$
$$C_{O2} \approx 10\mu F$$
$$C_{O3} \approx 1\mu F$$
$$C_{O4} \approx 10\mu F$$
$$C_{O5} \approx 1\mu F$$

As with the input capacitor, an additional high-frequency ripple voltage occurs at the output due to the output capacitor's ESR and can be minimized by choosing a capacitor with low ESR.

Step 14: Setting Up the Switching Frequency

The MAX17690 can operate at switching frequencies between 50kHz and 250kHz (subject to the considerations in Step 3). A lower switching frequency optimizes the design for efficiency, whereas increasing the switching frequency allows for smaller inductive and capacitive components sizes and costs. A switching frequency of 128kHz was chosen in Step 3. Resistor R15 sets the switching frequency according to the following expression:

$$R15 = \frac{5 \times 10^6}{f_{SW}} \approx 50k\Omega$$

where R15 is in kΩ and f_{SW} is in Hz.

Step 15: Setting Up the Soft-Start Time

Capacitor C6 connected between the SS pin and SGND programs the soft-start time. A precision internal 5μA current source charges the soft-start capacitor C6. During the soft-start time, the voltage at the SS pin is used as a reference for the internal error amplifier during startup. The soft-start feature reduces inrush current during startup. Since the reference voltage for the internal error amplifier is ramping up linearly, so too is the output voltage during soft-start. The soft-start capacitor is chosen based on the required soft-start time (10ms) as follows:

$$C8 = 5 \times t_{SS} \approx 50nF$$

where C8 is in nF and t_{SS} is in ms. A standard 47nF capacitor was chosen.

Step 16: Setting Up the UVLO and OVI Resistors

A resistor-divider network of R5, R6, and R7 from V_{IN} to SGND sets the input undervoltage lockout threshold and the output overvoltage inhibit threshold. The MAX17690 does not commence its startup operation until the voltage on the EN/UVLO pin (R7/R6 node) exceeds 1.215V (typ). When the voltage on the OVI pin (R6/R5 node) exceeds 1.215V (typ), the MAX17690 will stop switching, thus inhibiting the output. Both pins have built-in hysteresis to avoid unstable turn-on/turn-off at the UVLO/EN and OVI thresholds. After the device is enabled, if the voltage on the UVLO/EN pin drops below 1.1V (typ), the controller will turn off, and after the device is OVI inhibited, it will turn back on when the voltage at the OVI pin drops below 1.1V (typ). Whenever the controller turns on, it will go through the soft-start sequence. For the current design, resistors R5 = 10kΩ, R6 = 105kΩ, and R7 = 392kΩ give rise to an UVLO/EN threshold of 5.36V and an OVI threshold of 61.6V.

Step 17: Placing Decoupling Capacitors on V_{IN} and INTVCC

As previously discussed, the MAX17690 no-opto flyback controller compares the voltage $V_{FLYBACK}$ to V_{IN}. This voltage difference is converted to a proportional current that flows in R5. The voltage across R5 is sampled and compared to an internal reference by the error amplifier. The output of the error amplifier is used to regulate the output voltage. The V_{IN} pin should be directly connected to the input voltage supply. For robust and accurate operation, a ceramic capacitor (C6 = 1µF) should be placed between V_{IN} and SGND as close as possible to the IC.

V_{IN} powers the internal low dropout regulator of the MAX17690. The regulated output of the LDO is connected to the INTVCC pin. A ceramic capacitor (C7 = 2.2µF, min) should be connected between the INTVCC and PGND pins for the stable operation over the full temperature range. Place this capacitor as close as possible to the IC.

Step 18: Setting Up the Feedback Components

R_{SET}, R_{FB}, R_{RIN}, R_{VCM}, and R_{TC} are all critically important to achieving optimum output voltage regulation across all specified line, load, and temperature ranges.

R_{SET} resistor: This resistor value is optimized based on the IC's internal voltage to current amplifier and should not be changed.

$$R10 = R_{SET} = 10k\Omega$$

R_{FB} resistor: The feedback resistor is calculated according to the following equation:

$$R_{FB} = \frac{R_{SET}}{n_{SP} \times V_{SET}} \times \left\{ V_O + V_D + V_{TC} + \frac{\delta V_{DFR}}{\delta T} \times \frac{\delta T}{\delta V_{TC}} \right\}$$
$$= 125k\Omega$$

From the MAX17690 data sheet, V_{SET} = 1V. The two resistors R8 = 100kΩ and R9 = 27kΩ form R_{FB}. Using one high-value resistor and one low-value resistor in series allows slight adjustment to the series resistance combination so that the output voltage can be fine-tuned to its required value, if necessary.

R_{RIN} resistor: The internal temperature compensation circuitry requires a current proportional to V_{IN}. R_{RIN} is calculated according to the following equation:

$$R_{RIN} \approx 0.6 \times R_{FB}$$

R_{VCM} resistor: The MAX17690 generates an internal voltage proportional to the on-time volt-second product. This enables the device to determine the correct sampling instant for $V_{FLYBACK}$ during the Q_P off-time. Resistor R6 is used to scale this internal voltage to an acceptable internal voltage limit in the device. To calculate the resistor, we must first calculate a scaling constant as follows:

$$K_C = \frac{(1 - d_{MAX}) \times 10^8}{3 \times f_{SW}} = 120$$

where d_{MAX} = 0.65 and f_{SW} = 100,000Hz. After K_C is calculated, the R12 value can be selected from the table below by choosing the resistance value that corresponds to the next largest K_C.

K_C	R12
640	0Ω
320	75kΩ
160	121kΩ
80	220Ω
40	Open

In the present case, R12 = 121kΩ.

R_{TC} resistor: The value of R_{TC} can then be calculated using the previous expression, restated below:

$$R_{TC} = -R_{FB} \times n_{SP} \times \frac{\delta T}{\delta V_{DFR}} \times \frac{\delta V_{TC}}{\delta T}$$

This completes the setup of the MAX17690 no-opto flyback controller.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/19	Initial release	—