7.5W 5V Offline Flyback Converter Using the MAX17595

MAXREFDES1187

Introduction

The MAX17595 is a peak-current-mode controller for designing wide input-voltage flyback regulators. The MAX17595 offers optimized input thresholds for universal input AC-DC converters and telecom DC-DC (36V to 72V input range) power supplies. It contains a built-in gate driver for an external n-channel MOSFET. The MAX17595 houses an internal error amplifier with 1% accurate reference, eliminating the need for an external reference. The switching frequency is programmable from 100kHz to 1MHz with an accuracy of 8%, allowing optimization of magnetic and filter components, resulting in compact and cost-effective power conversion. For EMI-sensitive applications, the MAX17595 incorporates a programmable frequency dithering scheme, enabling low-EMI spread-spectrum operation. Users can start the power supply precisely at the desired input voltage, implement input overvoltage protection, and program soft-start time. A programmable slope compensation scheme is provided to ensure stability of the peak current-mode control scheme. Hiccup-mode overcurrent protection and thermal shutdown are provided to minimize dissipation in overcurrent and overtemperature fault conditions.

- Programmable Switching Frequency Allows Optimization of the Magnetic and Filter Components, Resulting in Compact, Cost-Effective, Efficient Isolated/Nonisolated Power Supplies
- 100kHz to 1MHz Programmable Switching Frequency with Optional Synchronization
- Peak Current Mode Control Provides Excellent Transient Response—Offline (Universal Input AC) and Telecom (36V to 72V) Flyback Controller
- Programmable Frequency Dithering Enables Low EMI Spread-Spectrum Operation
- Integrated Protection Features Enhance System Reliability
- Adjustable Current Limit with External Current Sense Resistor
- Fast Cycle-By-Cycle Peak Current Limiting Hiccup-Mode Short-Circuit Protection
- Overtemperature Protection
- Programmable Soft-Start and Slope Compensation
- Input Overvoltage Protection

Hardware Specification

An offline DCM flyback converter using the MAX17595 is demonstrated for a 5V DC output application. The power supply delivers up to 1.5A at 5V. Table 1 is an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	176V AC	284V AC
Frequency	f_{SW}	125kHz	
Output Voltage	V_{OUT}	5V	
Output Voltage Ripple	ΔV_{OUT}	1% of V_{OUT} max	
Output Current	I_{OUT}	0	1.5A
Output Power	P_{OUT}	7.5W	

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing an offline discontinuous conduction mode (DCM) flyback using Maxim's MAX17595 current-mode controller. The power supply has been built and tested, details of which follow later in this document.

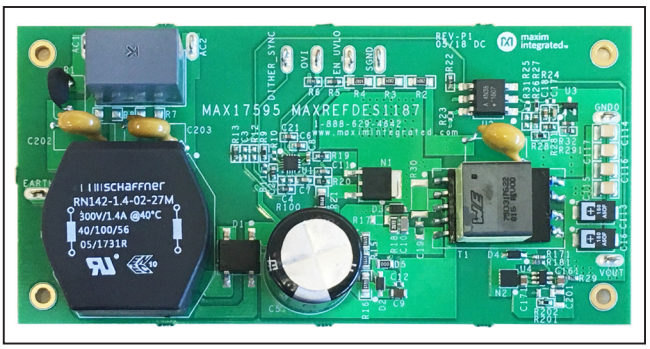

Figure 1. MAXREFDES1187 hardware.

Generic Isolated Power Supply

Figure 2 is a generic isolated power-supply block diagram. It consists of a power stage, an isolation transformer, rectifier, secondary-side error amplifier, and optocoupler to provide a feedback for the primary side control. Different isolated power supplies are different depending on how the transformer is being used in them.

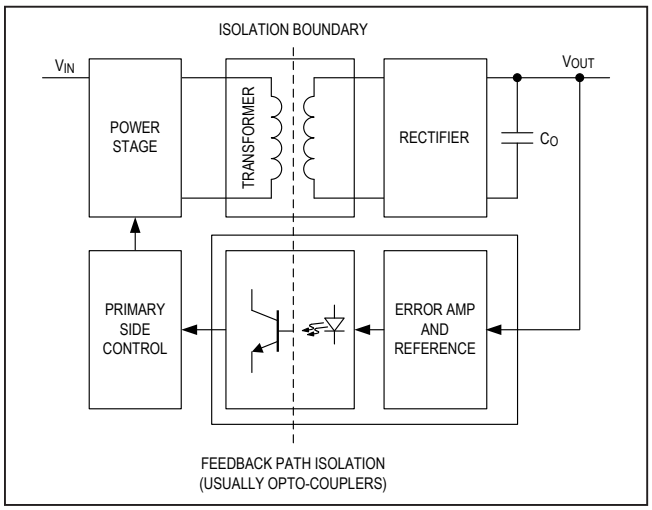

Figure 2. Generic isolated power supply.

Flyback Principle

A transformer in a flyback configuration acts differently than its usual operation of transformation of energy from primary to secondary. During a transformer's usual operation, both primary and secondary windings conduct together simultaneously to make the transfer of energy possible from primary to secondary. In a flyback configuration the primary and secondary windings do not conduct at the same time and the transformer acts more like a coupled inductor. Note that in this document we have used the following notations for the transformer turns ratio:

$$K = \frac{N_P}{N_S}$$

$$k = \frac{N_S}{N_P}$$

This means capital K for primary turns/secondary turns and small k for secondary turns/primary turns.

Figure 3 shows a simple flyback topology that consists of a transformer whose primary winding is connected to the drain of a switching MOSFET. The source of the MOSFET is connected to ground. The secondary winding is connected to the output capacitor through a rectifier diode. In this flyback configuration the current flows into the primary winding during the on time of the switching period and flows into the secondary winding during the off time of the switching period.

During the on-time when the primary switch is closed, a current, I_P, flows through the primary winding as shown in Figure 4. I_P can be written as follows:

$$I_P(t) = \frac{1}{L_P}\int_0^t V_{IN} d\tau = \frac{1}{L_P} V_{IN} t$$

The peak magnitude of the primary current can be written as follows:

$$I_{P-P} = \frac{1}{L_P}\int_0^{t_{ON}} V_{IN} d\tau = \frac{1}{L_P} V_{IN} t_{ON}$$

In the secondary winding, a negative voltage is induced due to the current flowing in to the primary. The rectifier diode is reverse-biased and no current is flowing in the secondary winding. The induced voltage in the primary can be written as:

$$V_S(t) = L_S \times \frac{dI_P(t)}{dt}$$

During the off-time when the primary switch opens as shown in Figure 5, the magnetic field in the primary winding collapses and the voltage at the winding reverses, while current keeps flowing in the same direction until the field fades away.

The secondary current I_S flows and the secondary and rectifier diode is forward-biased. Output voltage V_{OUT} is now available across the secondary coil if we ignore the forward voltage drop of the rectifier diode. The secondary winding voltage is now flown away to the primary side as $K \times V_{OUT}$. This voltage is present across the switch until the current in the secondary winding decays to zero. Total voltage available across the switch during the off-time can be written as:

$$V_{SW} = V_{IN} + K \times V_{OUT}$$

This voltage also causes the breakdown of the magnetic flux in the primary winding (no current is flowing in the primary winding after this reset). Here we can see that unlike a usual transformer action where current flows in both windings at the same time, in a flyback transformer the current flows into the primary winding during the on-time and into the secondary winding during the off-time. This is why we use the term "coupled storage inductor" for transformers used in flyback operation. It should be noted though that mechanically these transformers are like any transformer. Use in flyback operations makes transformers act differently as coupled inductors. The required duty cycle for a given input voltage and output voltage can be calculated from:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}}$$

where:

$$V_{OUT} = (V_{OUT} + V_F) \times \frac{N_P}{N_S}$$

Figure 6 shows a typical continuous conduction mode (CCM) flyback primary and secondary winding current, and Figure 7 shows a typical DCM mode flyback waveform.

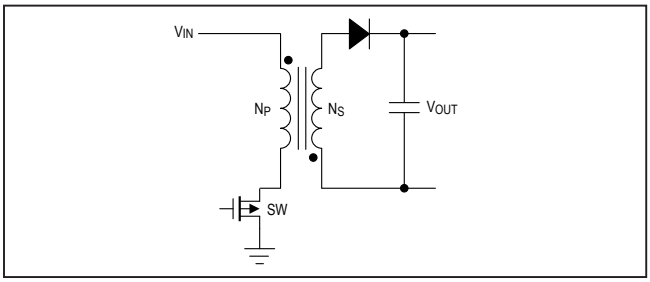

Figure 3. Simple flyback topology.

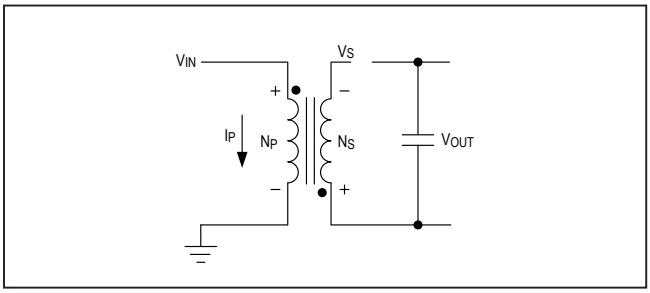

Figure 4. Flyback topology during on-time, t_{ON}.

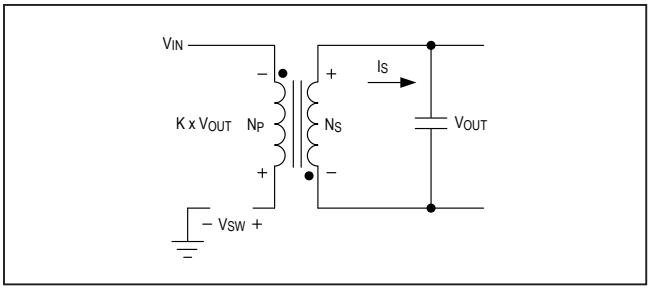

Figure 5. Flyback topology during off-time, t_{OFF}.

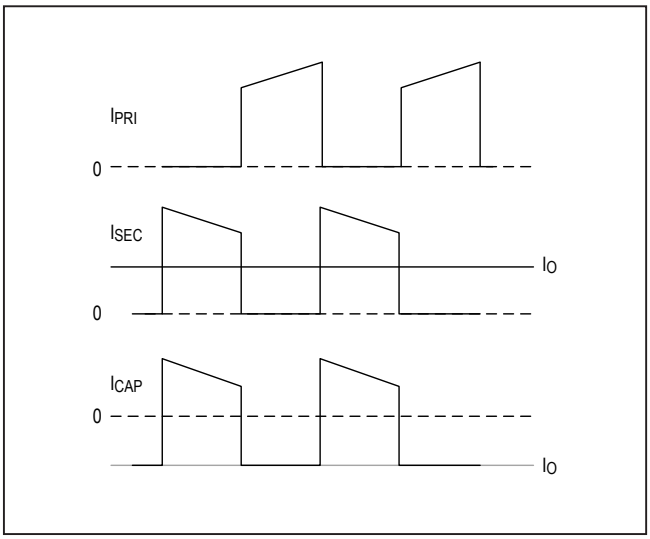

Figure 6. A typical CCM mode flyback primary and secondary winding current.

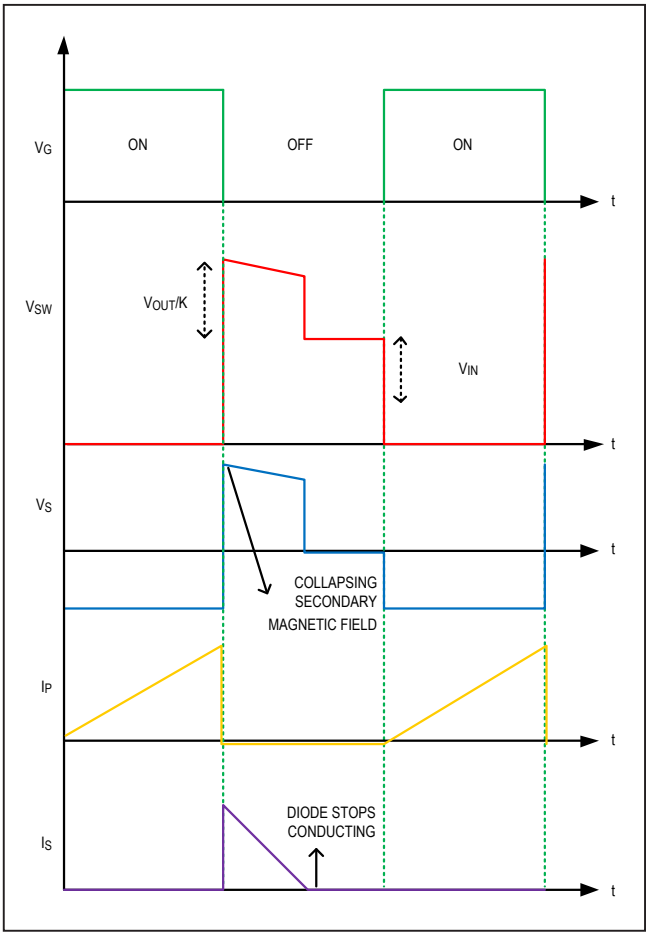

Figure 7. A typical DCM mode flyback topology waveform.

Design Procedure for Offline Flyback Using MAX17595

Now that the basic principle of the DCM flyback is understood, a practical design can be illustrated. The design parameters are obtained by using expressions given in Maxim **Application Note 5504**. This document is primarily concerned with the power stage and the feedback loop design, and is intended to complement the information contained in the MAX17595 data sheet.

Flyback converters can be operated in DCM or CCM modes. The component choices, stress level in power devices, and controller design vary depending on the operating mode of the converter. The design discussed in this document is a DCM design and expressions for calculating component values and ratings are presented to achieve the design goals.

Step 1: Switching Frequency

For offline flyback operation, the selection of switching frequency is of prime importance. Thermal limits and junction temperature of the device limits the selected switching frequency to be less than 150kHz. For this design we have selected a switching frequency of 125kHz. The MAX17595 switching frequency is programmable between 100kHz and 1000kHz with a resistor R_{RT} connected between RT and SGND. The R_{RT} is calculated as follows:

$$R_{RT} = \frac{10^{10}}{f_{SW}} \Omega$$

$$R_{RT} = \frac{10^{10}}{125k} = 80k\Omega$$

A standard 80.6kΩ resistor is selected for R_{RT}.

Step 2: Transformer Magnetizing Inductance and Turns Ratio

In a DCM flyback converter, the energy stored in the primary inductance of the flyback transformer is delivered entirely to the output. The maximum primary-inductance value for which the converter remains in DCM at all operating conditions can be calculated as:

$$L_{PRI} \le \frac{0.4 \times (V_{INMIN} \times D_{MAX})^2}{(V_{OUT} + V_D) \times I_{OUT} \times f_{sw}}$$

where:

D_{MAX} = 0.43V

V_D = 0.1V is the forward voltage drop of the rectifier diode of the secondary winding. Here we are using synchronous rectification using the MAX17606 MOSFET driver at the secondary side.

In this offline application, the DC bus voltage varies from 248.9V DC to 401.6V DC. But the actual minimum input operating voltage depends on the 100Hz ripple present on the DC bus capacitor. In this application, the ripple is assumed to be 30V and hence the minimum DC input to the converter.

$$V_{INMIN} = 176 \times 1.414 - 30 = 218.9V$$

Substituting the above values in the expression of L_{MAG} follows:

$$L_{PRI} \le \frac{0.4 \times (218.9 \times 0.43)^2}{5.1 \times 1.5 \times 125k} = 3706.1\mu H$$

The primary inductance for our design, L_{PRI} is chosen as 2mH, L_{PRI} = 2mH.

The leakage inductance of the transformer should be targeted as low as possible. For this design, we achieved a 1.5% leakage inductance of 30µH, L_{LKG} = 30µH.

A customized transformer 750317622 from Würth Elektronik® is used in this design. This transformer also fulfills the specification of turns ratio, bias winding, and primary/secondary currents requirement of the design that is calculated step by step in this document. The transformer has dielectric isolation specification of 4200V AC.

Step 3: Maximum Duty Cycle Calculation with Selected L_{PRI}

Use the following expressions to calculate the maximum duty cycle of the converter for the selected frequency and magnetizing inductance:

$$D_{NEW} = \frac{\sqrt{2.5 \times L_{PRI} \times V_{OUT} \times I_{OUT} \times f_{SW}}}{V_{INMIN}}$$

$$D_{NEW} = \frac{\sqrt{2.5 \times 2m \times 5 \times 1.5 \times 125k}}{218.9} = 0.312$$

Calculate the required transformer turns ratio (k) using the expressions as follows:

$$k = \frac{N_s}{N_p} = \frac{(V_{OUT} + V_D) \times (1 - D_{NEW})}{D_{NEW} \times V_{INMIN}}$$

$$k = \frac{N_s}{N_p} = \frac{(5 + 0.1) \times (1 - 0.312)}{0.312 \times 218.9} = 0.05$$

For the present design, k is chosen as 1:0.05.

Step 4: Calculation of Peak/RMS Current

Primary and secondary RMS and primary peak currents calculations are needed to design the transformer in switched-mode power supplies. Also, primary peak current is used in setting the current limit. Use the following expressions to calculate the primary and secondary peak and RMS currents.

$$I_{PRIPEAK} = \frac{V_{INMIN} \times D_{NEW}}{L_{PRI} \times f_{SW}} = \frac{218.9 \times 0.312}{2m \times 125kHz} = 0.273A$$

$$I_{PRIRMS} = I_{PRIPEAK} \times \sqrt{\frac{D_{NEW}}{3}} = 0.273 \times \sqrt{\frac{0.312}{3}} = 0.088A$$

$$I_{SECPEAK} = \frac{I_{PRIPEAK}}{k} = \frac{0.273}{0.05} = 5.35A$$

$$I_{SECRMS} = \sqrt{\frac{2 \times I_{OUT} \times I_{PRIPEAK}}{3 \times k}} = 2.31A$$

Step 5: Current Limit Resistor Calculation

For current limit setting, the peak current can be calculated as follows:

$$I_{LIM} = 1.2 \times I_{PRIPEAK} = 1.2 \times 0.273 = 0.328A$$

The device includes a robust overcurrent protection scheme that protects the device under overload and short-circuit conditions. A current-sense resistor, connected between the source of the MOSFET and PGND, sets the peak current limit. The current-limit comparator has a voltage trip level ($V_{CS-PEAK}$) of 300mV. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{305m}{I_{MOSFET}} = \frac{305m}{0.328} = 928m\Omega$$

where I_{MOSFET} is the peak current flowing through the MOSFET. A typical 910mΩ current-sense resistor is selected, R_{CS} = 910mΩ.

Step 6: MOSFET Selection

MOSFET selection criteria includes maximum drain voltage, peak/RMS current in the primary, and the maximum allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum V_{DS} rating must be higher than the worst-case drain voltage as follows:

$$V_{DSMAX} = V_{INMAX} + \left(\frac{2.5 \times (V_{OUT} + Vd)}{k}\right)$$

$$V_{DSMAX} = 401.6 + \left(\frac{2.5 \times (5 + 0.1)}{0.05}\right) = 650.6V$$

For this application, the 800V 2.5A n-channel MOSFET IPD80R2K4P7 from Infineon® is selected as the primary MOSFET.

Step 7: Snubber Selection

RCD snubbers reduce the maximum voltage stress on the MOSFET by clamping the voltage level. However, they also dissipate power and reduce efficiency. They might not always be required, but it is always a good idea to leave placeholders in the board for RCD and RC snubbers. Ideally, the external MOSFET experiences a drain-source voltage stress equal to the sum of the input voltage and reflected voltage across the primary winding during the off period of the MOSFET. In practice, parasitic inductors and capacitors in the circuit, such as leakage inductance of the flyback transformer, cause voltage overshoot and ringing in addition to the ideally expected voltage stress. Snubber circuits are used to limit the voltage overshoots to safe levels within the voltage rating of the external MOSFET. The snubber capacitor can be calculated using the following expression:

$$C_{SNUB} = \frac{2 \times L_{LK} \times I_{PRIPEAK}^2 \times k^2}{V_{OUT}^2}$$

$$C_{SNUB} = \frac{2 \times 30\mu \times 0.273^2 \times 0.05^2}{5^2} = 471.7pF$$

Considering the derating of the capacitor, we selected a capacitor of value 560pF, C_{SNUB} = 560pF.

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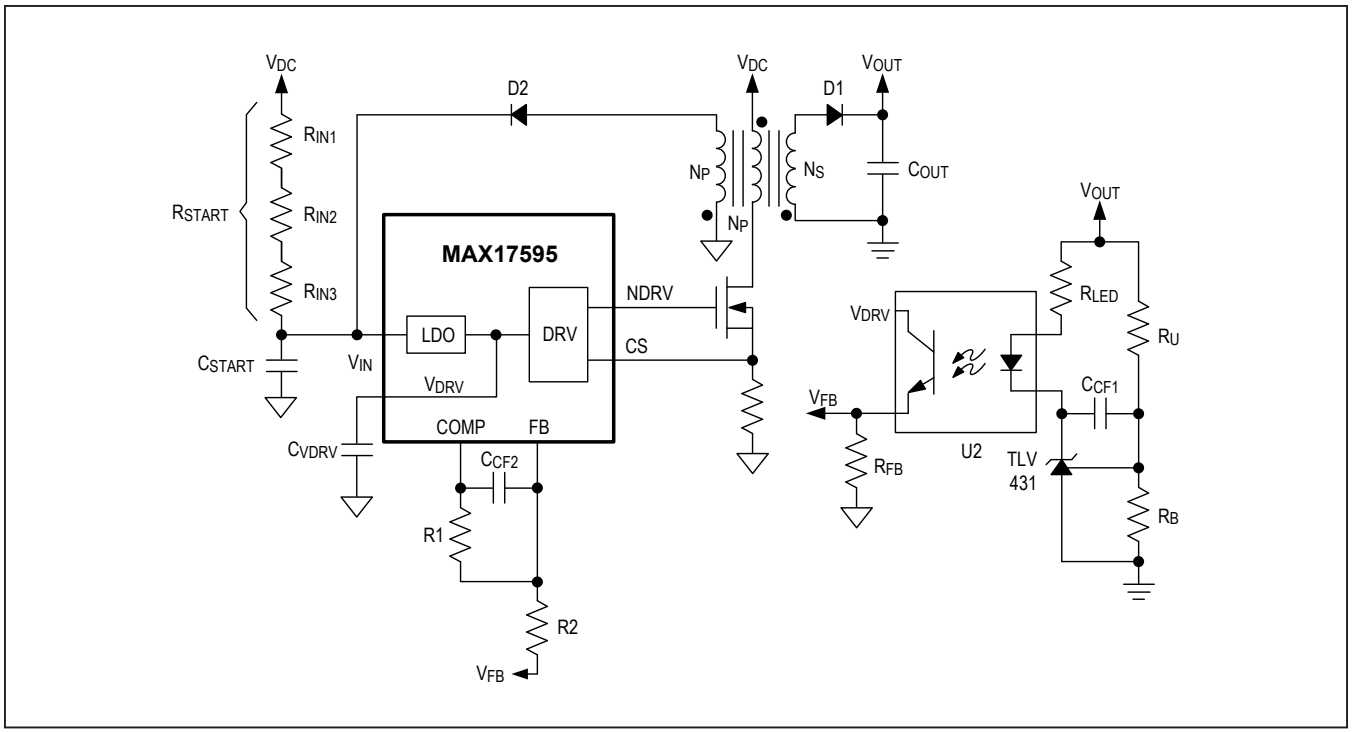

Figure 8. Bias winding configuration.

The power that must be dissipated in the snubber resistor is calculated using the following expressions:

$$P_{SNUB} = 0.833 \times L_{LKG} \times I_{PRIPEAK}^2 \times f_{SW}$$

$$P_{SNUB} = 0.833 \times 30\mu \times 0.273^2 \times 125k = 234mW$$

The snubber resistor is calculated based on the following expression:

$$R_{SNUB} = \frac{6.25 \times V_{OUT}^2}{P_{SNUB} \times k^2} = \frac{6.25 \times 5^2}{0.234 \times 0.05^2} = 254.5k\Omega$$

A standard resistor of 261kΩ 660mW is selected, R_{SNUB} = 261kΩ.

The voltage rating of the snubber diode is:

$$VD_{SNUB} = V_{INMAX} + (2.5 \times \frac{V_{OUT}}{k})$$

$$VD_{SNUB} = 401.2 + (2.5 \times \frac{5}{0.05}) = 645.8V$$

An 800V, 1A diode S1KL from Taiwan Semiconductor is selected as the snubber diode for this design.

Step 8: Selection of Secondary MOSFET

The maximum operating drain-source rating of the secondary MOSFET must be higher than the sum of the output voltage and the reflected input voltage. We use the following expression to calculate the secondary diode voltage rating:

$$V_{SEC} = 1.25 \times (k \times V_{INMAX} + V_{OUT})$$

$$V_{SEC} = 1.25 \times (0.05 \times 401.6 + 5) = 31.95V$$

For this application a 40V, 40A, MOSFET BSZ040N04LSG from Infineon is selected as a secondary MOSFET.

Step 9: Bias Winding Supply Configuration

The MAX17595 is implemented with a 20V V_{IN} UVLO wake-up level with 13V hysteresis to optimize the size of bias capacitor. A simple RC circuit is used to start up the MAX17595. To sustain the operation of the circuit, the input supply to the IC is bootstrapped through diode D2 as shown in Figure 8.

Use V_{BIAS} = 12V. Bias winding turns ratio k_b can be calculated as follows:

$$k_b = k \times \frac{V_{BIAS} + V_{D2}}{V_{OUT} + V_{D1}} = 0.05 \times \frac{12 + 0.8}{5 + 0.1} = 0.128$$

In isolated applications where a bias winding configuration is used to power up the MAX17595, C_{START} can be calculated as follows:

$$C_{START} = 0.75 \times (C_{DRV} + 0.1 \times I_{IN} \times t_{SS} + 0.04 \times t_{SS} \times Q_G \times f_{SW})$$

C_{START} is the startup capacitor, C_{DRV} is the cumulative capacitor used at the DRV pin, I_{IN} is the MAX17595 quiescent current, t_{SS} is the soft-start time, V_{OUT} is the output voltage, C_{OUT} is the output capacitor used, and Q_G is the gate charge of the primary n-channel MOSFET.

Select:

$$C_{DRV} = 1\mu F$$

$$I_{IN} = 2mA$$

$$Q_G = 6nC$$

$$t_{SS} = 12ms$$

$$C_{START} = 0.75 \times (1\mu + 0.1 \times 2m \times 12m + 0.4 \times 12m \times 6n \times 125k)$$

$$C_{START} = 2.82\mu F$$

It is recommended to consider the derating of the startup capacitor. A typical value of 4.7µF is selected as C_{START}, C_{START} = 4.7µF.

R_{START} can be calculated as follows:

$$R_{START} = \frac{(V_{START} - 10) \times 50}{1 + C_{START}} k\Omega$$

where C_{START} is in µF.

$$R_{START} = \frac{(218.9 - 10) \times 50}{1 + 4.7} = 1832.4k\Omega$$

R_{START} is divided into three equal-value resistors of 610.8kΩ each. Standard 1206 resistor value of 619kΩ 250mW is selected for R_{IN1}, R_{IN2}, and R_{IN3}, respectively.

$$R_{IN1} = R_{IN2} = R_{1N3} = 619k\Omega$$

Step 10: Feedback Resistor Selection R_U, R_B

For all the applications that use a startup network to bias the V_{IN} pin during the power-up sequence, calculate the feedback potential divider using the following formulas:

$$R_B = \frac{10 \times (30 \times C_{START} - 20 \times C_{DRV} - I_{IN} \times t_{SS})}{V_{OUT} \times C_{OUT} \times (I_{IN} + Q_G \times f_{SW})}$$

$$R_B = \frac{10 \times (30 \times 4.7\mu - 20 \times 1\mu - 2m \times 12m)}{5 \times 360.9\mu \times (2m + 6n \times 125kHz)} = 163.1\Omega$$

A standard resistor of 162Ω is selected, R_B = 162Ω.

$$R_U = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_B$$

where V_{REF} is the reference set by the secondary-side controller (V_{REF} = 1.24V for TLV431 is used in this design).

$$R_U = \left(\frac{5}{1.24} - 1\right) \times 162 = 0.491k\Omega$$

A standard resistor of 0.487kΩ is selected, R_U = 0.487kΩ.

Step 11: Soft-Start Capacitor

The soft-start period for the devices can be programmed by selecting the value of the capacitor C_{SS} connected from the SS pin to SGND. Capacitor C_{SS} can be calculated as:

$$C_{SS} = 8.264 \times t_{SS}$$

where t_{SS} is expressed in ms and the resultant value of C_{SS} is in nF.

$$C_{SS} = 8.264 \times t_{SS} = 8.264 \times 12 = 99.17nF$$

A standard 100nF is selected as the soft-start capacitor, C_{SS} = 100nF.

Step 12: Input Capacitor Selection

The MAX17595 is optimized to implement offline AC-DC applications. In such applications, the input capacitor must be selected based on either the ripple due to the rectified line voltage, or based on holdup-time requirements. Holdup time can be defined as the time period over which the power supply should regulate its output voltage from the instant the AC power fails.

For the flyback converter, the input capacitor supplies the input current when the diode rectifier is off. The voltage discharge on the input capacitor, due to the input average current, should be within the limits specified. Assuming 25% ripple present on input DC capacitor, the input capacitor can be calculated as follows:

$$C_{IN} = \frac{0.045 \times P_{LOAD}}{\eta \times V_{INPK}^{2}}$$

where:

η = Target efficiency = 87% (For offline flyback with low voltage, high current outputs, the achieved efficiency is less than the target because of relatively high losses.)

P_{LOAD} = 5 × 0.7 = 7.5W

V_{INPK} = Peak voltage at minimum AC voltage = 248.9V

$$C_{IN} = \frac{0.045 \times 7.5}{0.87 \times 248.9^{2}} = 6.26\mu F$$

Step 13: Output Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of a certain percentage of the rated output current so that the output voltage deviation is contained to 3% of the rated output voltage. The output capacitance can be calculated by using the below expressions:

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}} \right)$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

where I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, and f_C is the target closed-loop crossover frequency. In our application, we selected f_C = 5kHz, typical bandwidth at nominal voltage for isolated applications to minimize noise and proportionally increase the gain.

$$I_{STEP} = 0.5 \times I_{OUT} = 0.5 \times 1.5 = 0.75A \text{ (50\% of } I_{OUT})$$

$$\Delta V_{OUT} = 0.03 \times 5 = 150mV \text{ (3\% of } V_{OUT}, \text{typ})$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{5k} + \frac{1}{125k} \right) = 74\mu s$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}} = \frac{0.75 \times 74\mu}{0.150} = 370\mu F$$

Due to the DC-bias characteristics, 4 × 47µF 10V MLCC capacitors are selected as C_{OUT} for this design.

MLCC capacitor values change with temperature and applied voltage. Refer to the capacitor data sheets to select capacitors that guarantee the required output capacitance across the operating range. For design calculations, use the worst-case derated value of capacitance, based on temperature range and applied voltage. We have also used 2 x tantalum polymer capacitors with a value of 150µF in parallel with the MLCCs. The worst-case total value of all the capacitors is 360.9µF.

For the flyback converter, the output capacitor supplies the load current when the main switch is on, and therefore the output voltage ripple is a function of load current and duty cycle. Use the following expression to estimate the output capacitor ripple:

$$\Delta V_{COUT} = \frac{I_{OUT} \times \left[I_{PRIPEAK} - (k \times I_{OUT}) \right]^{2}}{I_{PRIPEAK}^{2} \times f_{SW} \times C_{OUT}}$$

$$\Delta V_{COUT} = \frac{1.5 \times \left[0.273 - (0.05 \times 1.5) \right]^{2}}{0.273^{2} \times 125kHz \times 360.9\mu} = 17.2mV$$

Step 14: Loop Compensation

Optocoupler feedback is used in isolated flyback converter designs for precise control of isolated output voltage. Figure 9 shows the overall scheme of the optocoupler feedback.

Use R_{FB} = 470Ω (typ), for an optocoupler transistor current of 1mA. Select R1 = 49.9kΩ and R2 = 22kΩ (typical values) to use the full range of available COMP voltage. U3 is a low-voltage adjustable shunt regulator with a 1.24V reference voltage. In this design a 1.24V, 0.5% shunt regulator TLV431BFTA from Diodes Inc. is selected.

Calculate R_{LED} using the following expression:

$$R_{LED} = 400 \times CTR \times (V_{OUT} - 2.7)$$

$$R_{LED} = 400 \times 1 \times (5 - 2.7) = 0.920k\Omega$$

A standard 0.931kΩ resistor is selected, R_{LED} = 0.931kΩ.

The bandwidth of typical optocouplers limits the achievable closed-loop bandwidth of opto-isolated converters. Considering this limitation, the closed-loop crossover frequency can be chosen at the nominal input voltage by selecting f_C = 5kHz. Closed-loop compensation values are designed based on the open-loop gain at the desired crossover frequency, f_C. The open-loop at f_C is calculated using the following expressions.

$$f_P = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}} = \frac{1.5}{\pi \times 5 \times 360.9\mu} = 264.5Hz$$

$$G_{PLANT} = \frac{f_P}{f_C} \times \sqrt{\frac{L_{PRI} \times f_{SW} \times V_{OUT}}{8 \times I_{OUT}}} \times \frac{V_{IN}}{V_{IN} \times R_{CS} + 50 \times 10^{3} \times L_{PRI}}$$

$$G_{PLANT} = \frac{264.5}{5kHz} \times \sqrt{\frac{2m \times 125k \times 5}{8 \times 1.5}} \times \frac{325.26}{325.6 \times 910m + 50 \times 10^{3} \times 2m}$$

$$G_{PLANT} = 0.05 \times 10.2 \times 0.862 = 0.466$$

Three controller configurations are suggested in **Application Note 5504** based on open-loop gain and the R_{LED} value. For typical designs, the current transfer ratio (CTR) of the optocoupler designs can be assumed to be unity. It is known that the comparator and gate-driver delays associated with the input voltage variations affect the opto-coupler CTR. Depending on the optocoupler selected, variations in CTR causes wide variations in bandwidth of the closed-loop system across the input-voltage operating range. It is recommended to select an optocoupler with less CTR variations across the operating range. Checking the condition as stated in **Application Note 5504**:

$$G_{PLANT} \times CTR \times \frac{R_{FB}}{R_{LED}} \times \frac{R_1}{R_2} =$$

$$0.466 \times 1 \times \frac{470}{0.931k} \times \frac{49.9k}{22k} = 0.545$$

As 0.545 < 0.8, therefore, as stated in **Application Note 5504**, configuration 1 is selected. Figure 10 is a typical schematic of configuration 1. The R_F value can be calculated from the expression below:

$$R_F = \left[\frac{R_{LED} \times R2}{G_{PLANT} \times CTR \times R_{FB} \times R1} - 1\right] \times R_U$$

$$R_F = \left[\frac{0.931k\Omega \times 22k\Omega}{0.466 \times 1 \times 470 \times 49.9k\Omega} - 1\right] \times 0.487k\Omega = 0.416k\Omega$$

A typical value of 0.412kΩ is selected as R_F, R_F = 0.412kΩ. The C_F value can be calculated from the expression below:

$$C_F = \frac{1}{2\pi \times (R_U + R_F) \times f_P} =$$

$$\frac{1}{2\pi \times (0.487k\Omega + 0.412k\Omega) \times 264.5} = 669.5nF$$

A standard 680nF capacitor is selected as C_F, C_F = 680nF. The C_{CF1} value can be calculated from the expression below:

$$C_{CF1} = \frac{1}{\pi \times R_F \times f_{SW}}$$

$$= \frac{1}{\pi \times 0.412k\Omega \times 125kHz} = 6183pF$$

A standard 5600pF capacitor is selected as C_{CF1} = 5600pF.

Step 15: EN/UVLO and OVI Setting

The device's EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable input UVLO pin. The device does not commence startup operation unless the EN/UVLO pin voltage exceeds 1.21V. The device turns off if the EN/UVLO pin voltage falls below 1.15V. A resistor-divider from the input DC bus to ground can be used to divide down and apply a fraction of the input DC voltage (V_{DC}) to the EN/UVLO pin. The values of the resistor-divider can be selected so the EN/UVLO pin voltage exceeds the 1.23V turn-on threshold at the desired input DC bus voltage. The same resistor-divider can be modified with an additional resistor (R_{OVI}) to implement input overvoltage protection in addition to the EN/UVLO functionality as shown in Figure 11.

When voltage at the OVI pin exceeds 1.21V the devices stop switching and resume switching operations only if voltage at the OVI pin falls below 1.15V. For given values of startup DC input voltage (V_{START}) and input overvoltage-protection voltage (V_{OVI}), the resistor values for the divider can be calculated as follows:

Select R_{OVI} = 24.9kΩ.

$$R_{EN} = R_{OVI} \times \left(\frac{V_{OVI}}{V_{START}} - 1\right)$$

where V_{OVI} = maximum allowed overvoltage = 290 ×1.414 = 410.12V.

$$R_{EN} = 24.9k \times \left(\frac{410.12}{218.9} - 1\right) = 21.75k\Omega$$

A standard 22kΩ resistor is selected, where R_{EN} = 22kΩ.

The same resistor-divider can be modified to implement input overvoltage protection. When the voltage at the OVI pin exceeds 1.215V (typ), the device stops switching. The device resumes switching operations only if the voltage at the OVI pin falls below 1.1V (typ).

$$R_{SUM} = [R_{OVI} + R_{EN}] \times \left[\frac{V_{START}}{1.21} - 1\right]$$

$$R_{SUM} = [24.9k + 22k] \times \left[\frac{218.9}{1.21} - 1\right] = 8393k\Omega$$

In universal AC input applications, R_{SUM} may need to be implemented as equal resistors in series (R_{DC1}, R_{DC2}, and R_{DC3}) so that voltage across each resistor is limited to its maximum operation voltage.

$$R_{DC1} = R_{DC2} = R_{DC3} = \frac{8393}{3}k\Omega = 2.79M\Omega$$

A standard 2.8MΩ resistor is selected for R_{DC1}, R_{DC2}, and R_{DC3}.

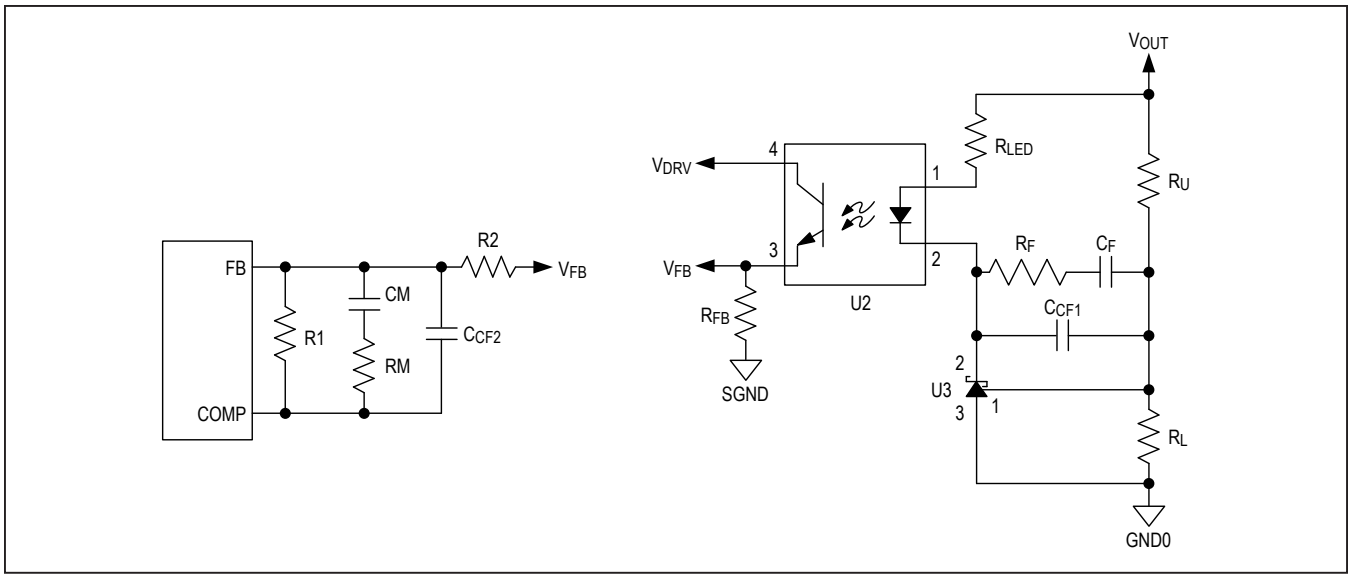

Figure 9. A typical optocoupler-based feedback compensation.

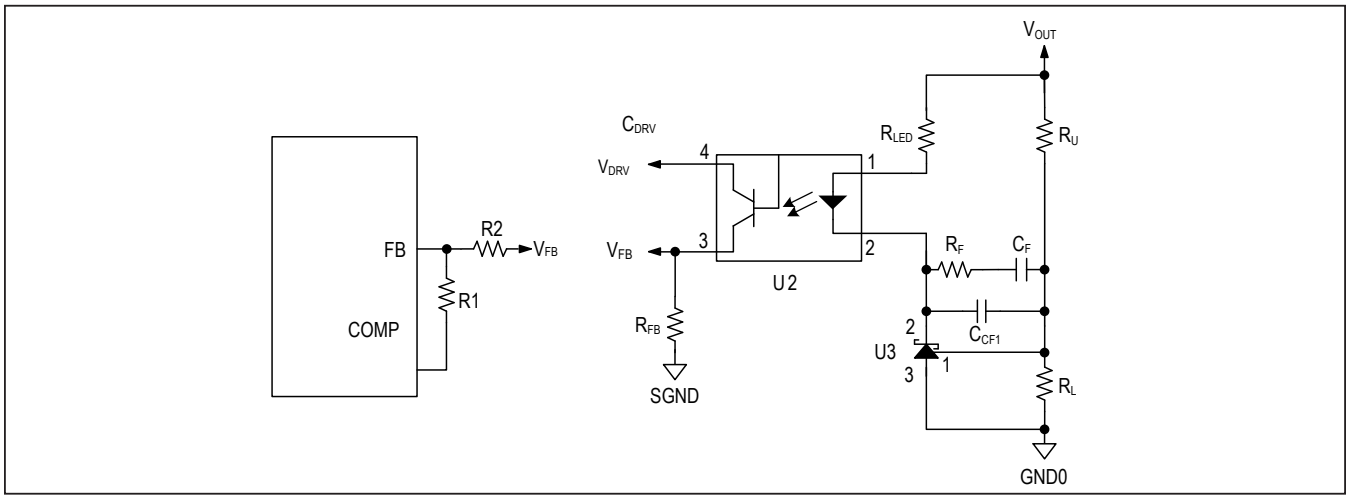

Figure 10. Optocoupler feedback compensation configuration 1 schematic.

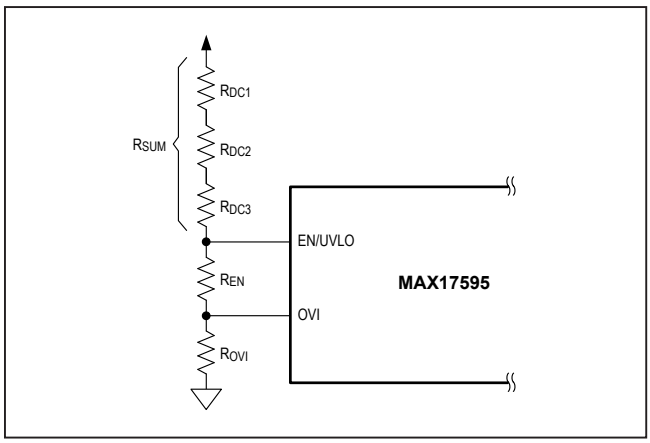

Figure 11. Programming EN/UVLO and OVI.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/18	Initial release	—