

Introduction

Power over Ethernet (PoE) is a technology that allows network cables to deliver power to a powered device (PD) via power-sourcing equipment (PSE) or midspan, and has many advantages over traditional methods of delivering power. The MAXREFDES1149 reference design is a 36V~57V input to 12V/1A output flyback PoE PD power module to be used in Ethernet equipment that needs the 12V power supply to be isolated from the primary Ethernet power. PoE allows power and data to be combined, removing the need for altering the AC mains infrastructure and can be installed by non-electricians. PoE is an intelligent system that is designed with protection at the forefront, preventing overload, underpowering, and installation errors, while allowing simple scalability and reliability. A high-efficiency, no-opto isolated flyback converter minimizes power loss with efficiencies greater than 89%, allowing reductions in excessive heat, longer IC lifetime, and maximum power available to the PD. Ultra-small packaging and no Schottky diode reduce the overall design size.

Other features include the following:

- IEEE® 802.3af/at Compliance
- 2-Event Classification
- No Schottky-Synchronous Operation for High Efficiency and Reduced Cost
- Ultra-Compact Layout
- Peak Efficiency > 89%
- 3mm × 3mm, 16-Pin TQFN (MAX17690), 6-Lead SOT23 (MAX17606), and Thermally Enhanced, 3mm × 3mm, 10-Pin TDFN (MAX5969A) Packages

Hardware Specification

This reference circuit consists of the MAX5969A PD controller and the MAX17690 no-opto isolated flyback controller. A 1GbE RJ45 magnetic jack is also included and two diode bridges for separating DC power provided by an end-span or midspan PoE system. The MAX17690 is a no-opto peak current-mode controller for design of wide input-voltage flyback converters. The reference design operates over a 36V to 57V input voltage range, and provides up to 1A at 12V output. The switching frequency is programma-

ble from 50kHz to 250kHz, allowing optimization of filter components and resulting in compact and cost-effective power conversion. This design is set to switch at 100kHz. Opto-coupler or third winding is not needed to derive feedback signal across isolation boundary.

The MAX17606 is the MOSFET driver. By replacing the secondary diode with a MOSFET, the MAX17606 improves the efficiency and makes the thermal management easier. Table 1 shows the design specification overview.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Voltage	V_{IN}	36V	48V	57V
Output Voltage	V_{OUT}		12V	
Output Current	I_{OUT}			1A
Output Power	P_{OUT}			12W
Peak Efficiency	η			89%

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed technical guide to designing a complete interface for a PD to comply with the IEEE 802.3af/at standard in a PoE Class 3 system and provide an isolated, high-efficiency flyback converter.

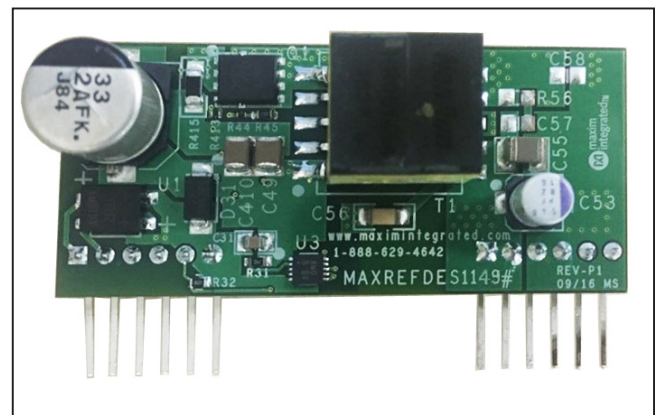


Figure 1. MAXREFDES1149 hardware.

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MAX5969A PD Interface

A PoE system delivers power and data to an end device (PD) typically through an RJ45 cable power from an end-span (PSE) or a midspan. The power is separated from the data through diode bridges to deliver a typical 48V for efficient power transfer, which is low enough to be considered a safe voltage and removes the need to rewire AC mains and saves cost.

Although this voltage is safe for humans, it still can damage equipment if not properly delivered. This is where MAX5969A classification is required, ensuring the equipment can handle the power delivery. Before the PSE can enable power to a connected IP camera or other PD, it must perform a signature detection.

Signature Detection

Signature detection uses a lower voltage to detect a characteristic signature of IEEE-compatible PDs (a 24.9k Ω resistance). Once this signature has been detected, the PSE knows that higher voltages can be safely applied. The PSE applies two voltages on V_{IN} in the range 1.4V to 10.1V (1V step minimum) and then records the current measurements at the two applied voltages. The PSE then computes the change in current when each voltage was applied ($\Delta V/\Delta I$) to ensure the presence of the 24.9k Ω signature resistor. See Figure 2.

Classification

In classification mode, the PSE classifies the PD based on the power consumption required. This design is a Class 4 system and uses 2-event classification to efficiently manage power distribution. (The IEEE 802.3af/at standard defines only Class 0 to 4 and Class 5 for any special requirement.)

An external resistor (R_{CLS}) of 30.9 Ω connected from CLS to V_{SS} sets the classification current. The PSE determines

the class of a PD by applying a voltage at the PD input and measuring the current sourced from the PSE.

When the PSE applies a voltage between 12.6V and 20V, the MAX5969A exhibits a current of 36.4mA to 43.6mA. The PSE uses the classification current information to classify the power requirement of the MAX5969A PD. The classification current includes the current drawn by R_{CLS} and the supply current of the MAX5969A so the total current drawn by the PD is within the IEEE 802.3af/at standard figures. The classification current is turned off whenever the device is in power mode. See Table 2.

2-Event Classification

During 2-event classification, a Type 2 PSE probes PD for classification twice. In the first classification event, the PSE presents an input voltage between 12.6V and 20V and the MAX5969A presents the programmed load, I_{CLASS} . The PSE then drops the probing voltage below the mark-event threshold of 10.1V and the MAX5969A present the mark current, I_{MARK} . This sequence is repeated one more time.

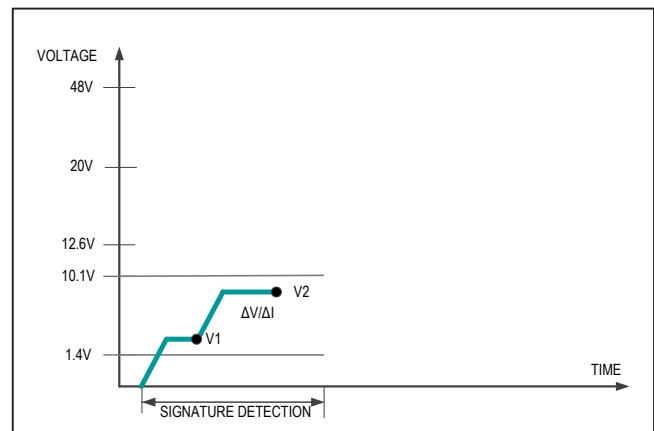


Figure 2. Signature detection.

Table 2. Classification Current

CLASS	MAXIMUM POWER USED BY PD (W)	R_{CLS} (Ω)	V_{IN}^* (V)	CLASS CURRENT SEEN AT V_{IN} (mA)		IEEE 802.3af/at PSE CLASSIFICATION CURRENT SPECIFICATION (mA)	
				MIN	MAX	MIN	MAX
0	0.44 to 12.95	619	12.6 to 20	0	4	0	5
1	0.44 to 3.94	117	12.6 to 20	9	12	8	13
2	3.84 to 6.49	66.5	12.6 to 20	17	20	16	21
3	6.49 to 12.95	43.7	12.6 to 20	26	30	25	31
4	12.95 to 25.5	30.9	12.6 to 20	36	44	35	45
5	> 25.5	21.3	12.6 to 20	52	64	—	—

* V_{IN} is measured across the MAX5969A input V_{DD} to V_{SS} .

Power Mode

The final stage after detection and classification of a newly connected PD is to enable power. The 48V supply from the PSE is connected to the PD through the RJ45 cable. Once enabled, the PSE continues to monitor how much current is being delivered to the PD and cuts power to the cable if the power drawn is not within the correct range. This protects the PSE against overload and underpowering, and ensures that the PSE is disconnected from the cable if the PD is unplugged or faulted.

The MAX5969A enters power mode when V_{IN} rises above the undervoltage lockout threshold (V_{ON}). When V_{IN} rises above V_{ON} , the MAX5969A turns on the internal n-channel isolation MOSFET to connect GND to RTN. The open-drain power-good output (PG) remains low for a minimum of t_{DELAY} until the power MOSFET fully turns on to keep the downstream DC-DC converter disabled during inrush. The PG open-drain output is connected to small-signal transistors to prevent the DC converters from powering up before the power from the PD is allowable.

Design Considerations for MAX5969A and MAX17690

MAX5969A

Place the input capacitor, classification resistor, and transient voltage suppressor as close as possible to the MAX5969A. Use large SMT component pads for power dissipating devices such as the MAX5969A and the external diodes. Use short and wide traces for high-power paths.

The MAX5969A enters undervoltage lockout when the input voltage drops below 37.3V. When the input drops

below this value the isolation MOSFET switches off, disconnecting the 48V from the buck converters. The MAX5969A exits undervoltage lockout when the input exceeds 37.3V, where the isolation MOSFET switches on again, connecting the MAX17690 converters.

MAX17690

The MAX17690 is a peak current mode, fixed-frequency switching controller specifically designed for the isolated flyback topology operating in Discontinuous Conduction Mode (DCM). The device senses the isolated output voltage directly from the primary-side flyback waveform during the off-time of the primary switch. No auxiliary winding or optocoupler is required for output voltage regulation. Figure 3 shows the reference design block diagram.

The MAX17690 is designed to operate over a wide 4.5V to 60V supply range. The switching frequency is programmable from 50kHz to 250kHz. An EN/UVLO pin allows the user to turn on/off the power supply precisely at the desired input voltage. The MAX17690 provides an input overvoltage protection through the OVI pin. The MAX17690's 7V internal LDO output makes it suitable for switching both logic-level and standard MOSFETs used in flyback converters. With 2A/4A source/sink currents, the MAX17690 is ideal for driving low $R_{DS(ON)}$ power MOSFETs with fast gate-transition times. The MAX17690 provides an adjustable soft-start feature to limit the inrush current during startup.

The MAX17690 provides temperature compensation for the output diode-forward-voltage drop. The device has robust hiccup-protection and thermal-protection schemes, and come in a space-saving, 16-pin, 3mm x 3mm TQFN package with a temperature range from -40°C to +125°C.

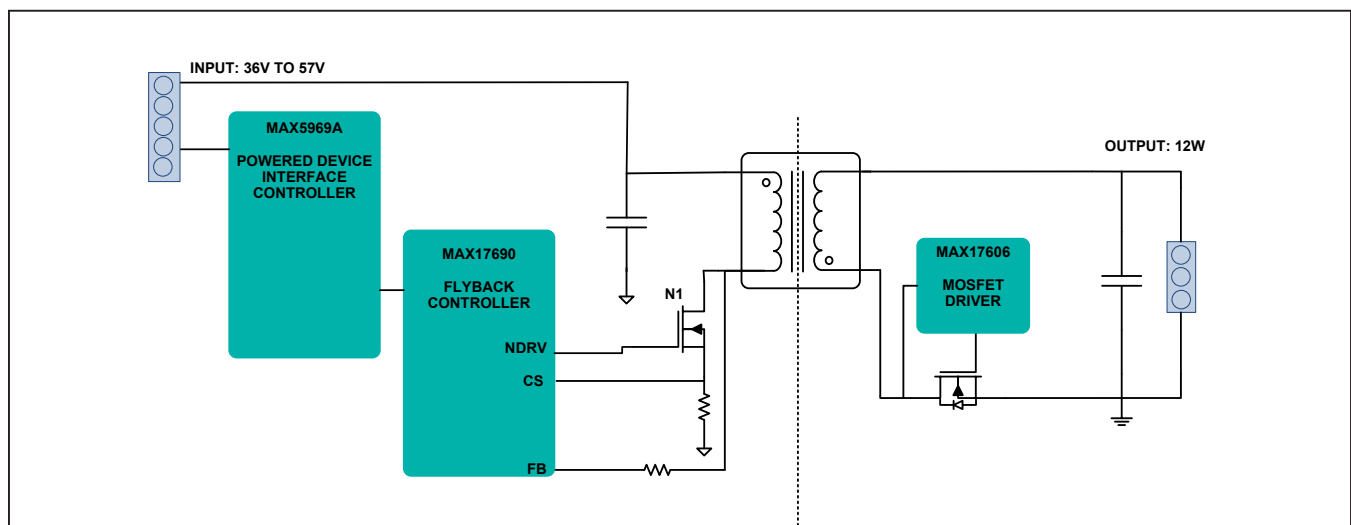


Figure 3. MAXREFDES1149 block diagram.

Design Procedure for the MAX17690

Step 1: Duty-Cycle Selection

Use the V_{INMIN} and V_{INMAX} from the selected specifications in the below equation to calculate the maximum duty cycle, D_{MAX} .

$$D_{MAX} = \frac{V_{INMAX}}{V_{INMAX} + 2 \times V_{INMIN}}$$

Step 2: Switching Frequency Selection

Then calculate the switching frequency:

$$f_{SW} < 720000 \times D_{MAX} \times \frac{V_{INMIN}}{V_{INMAX}}$$

Step 3: Transformer Magnetizing Inductance and Turns Ratio

Once the switching frequency and duty cycle are selected, the transformer magnetizing inductance (L_{MAG}) can be calculated from the energy balance equation given in the IC data sheet:

$$L_{MAG} = \frac{0.4 \times (V_{INMIN} \times D_{MAX})^2}{V_{OUT} \times I_{OUT} \times f_{SW}}$$

Step 4: Output Capacitor Selection

The output capacitor is usually sized to support a 50% step load of the maximum output current in the application, so the output voltage deviation is contained to $\pm 3\%$ of the output voltage change.

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

where I_{STEP} is the load current step, $t_{RESPONSE}$ is the response time of the controller, and ΔV_{OUT} is the allowable output voltage deviation.

$$t_{RESPONSE} \cong \frac{0.33}{f_C} + \frac{1}{f_{SW}}$$

Consider DC bias and aging effects while selecting the output capacitor. DC bias on a ceramic capacitor has a dramatic effect on the capacitance value. Refer to the capacitor's data sheet for capacitance vs. voltage graphs.

Step 5: Soft-Start Capacitor Selection

The capacitor connected between the SS pin and SGND programs the soft-start time. Internally generated 5 μ A of precise current source charges the soft-start capacitor. When the EN/UVLO voltage is above 1.215V (typ), the device initiates a soft-start sequence. During the soft-start time, the SS pin voltage is used as a reference for the internal error amplifier. The soft-start feature reduces the input inrush current during startup. The reference ramp-up allows the output voltage to increase monotonically from zero to the target output value.

$$C_{SS} = 5 \times t_{SS}$$

Set $t_{SS} = 5\text{ms}$, so $C_{SS} = 25\text{nF}$.

Design Resources

Download the complete set of [Design Resources](#) including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—

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