5V/4A Synchronous Buck Converter using the MAX18066

MAXREFDES1139

Introduction

This reference design MAXREFDES1139 uses the MAX18066, which is a current-mode, synchronous, DC-DC buck converter which delivers an output current up to 4A with high efficiency. The MAXREFDES1139 operates from an input voltage of 10.8V to 13.2V and provides an output voltage of 5V. It features a pulse-width modulation (PWM) mode operation with an internally fixed switching frequency of 500kHz and automatically enters skip mode at light loads. The current-mode control architecture simplifies compensation design and ensures a cycle-by-cycle current limit and fast response to line and load transients. A high gain transconductance error amplifier allows flexibility in setting the external compensation. It has internal MOSFETs that provide better efficiency, minimize electromagnetic interference (EMI), reduce board space, and provide higher reliability. There are additional features which include an externally adjustable soft-start, independent enable input and power-good output for power sequencing. This reference design is ideal for distributed power systems, notebook computers, nonportable consumer applications, and pre-regulation applications.

Hardware Specification

In this document, the MAX18066, a current-mode, synchronous, DC-DC buck converter is demonstrated for a 5V output application. The power supply delivers up to 4A. Figure 1 shows the MAXREFDES1139 hardware, while Table 1 shows an overview of the design specifications.

Table 1. Design Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Voltage	V_{IN}	10.8V	12V	13.2V
Output Voltage	V_{OUT}		5V	
Output Current	I_{OUT}		4A	
Output Ripple	ΔV_{OUT}		1%	
Input Ripple	ΔV_{IN}		1%	
Output Undershoot	V_{US}		3%	
Output Overshoot	V_{OS}		3%	
Frequency	f_{SW}		500kHz	
Efficiency	η		94.8%	

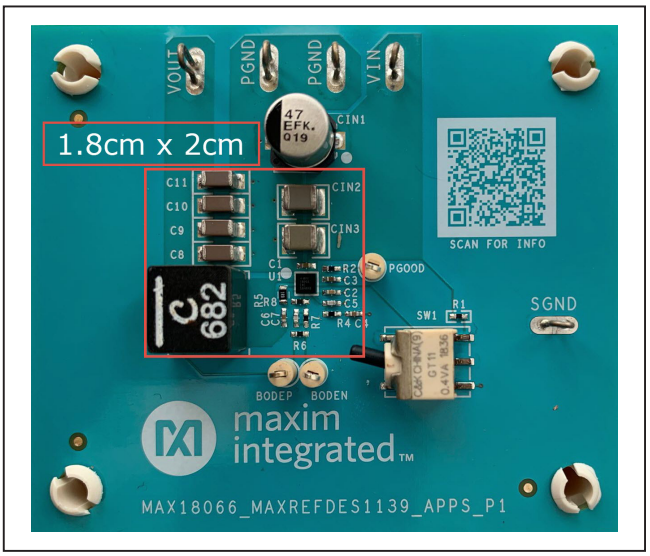

Figure 1. MAXREFDES1139 hardware.

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Designed–Built–Tested

This document describes the hardware shown in Figure 2 . It provides a detailed systematic technical guide to design a step-down (buck) DC-DC converter using the Maxim's MAX17501 synchronous step-down DC-DC converter. The power supply has been built and tested, and details which follow later in this document.

Design Procedure for MAXREFDES1139

Step 1: Input Capacitor

For a step-down converter, input capacitor C_{IN} helps to reduce the input ripple voltage, despite the discontinuous input AC current. A low equivalent series resistance (ESR) capacitors are preferred to minimize the voltage ripple due to ESR. For the low-ESR input capacitors, size C_{IN} uses the following formula:

$$C_{IN} = \frac{I_{LOAD}}{f_{SW} \times \Delta V_{IN\_RIPPLE}} \times \frac{V_{OUT}}{V_{IN}}$$

$$C_{INmin} = \frac{4 \times 5}{500000 \times 0.01 \times 10.8 \times 10.8} = 34.3\mu F$$

Two 47µF X5R TMK325ABJ476MM capacitors are used for the input capacitor. An additional 47µF electrolytic capacitor EEE-FK1E470P can be added in parallel to the ceramic capacitors to provide necessary damping for potential oscillations caused by a longer input power path and for reducing line side ripples.

Step 2: Inductor

Typically, the inductor value is chosen to have current ripple equal to 30% of load current. Inductance is calculated with the following formula:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{5}{500000 \times 0.3 \times 4} \times \left(1 - \frac{5}{13.2}\right) = 5.175\mu H$$

where f_{SW} is the internally fixed switching frequency of 500kHz and ΔI_L is the estimated inductor ripple current:

$$\Delta I_L = LIR \times I_{LOAD} = 0.3 \times 4 = 1.2A$$

where LIR is the inductor current ratio. Considering the worst-case for a minimum switching frequency of 450kHz, a 6.8µH COILCRAFT inductor XAL8080-682ME is chosen with a DCR value of 14.5mΩ. In addition, the peak inductor current, $I_{LPEAK}\left(I_{LOAD} + \frac{\Delta I_L}{2} = 4 + \frac{0.3 \times 4}{2} = 4.6A\right)$, is below both the minimum high-side current-limit value (7.7A, typ), and the inductor saturation current rating I_{LSAT}.

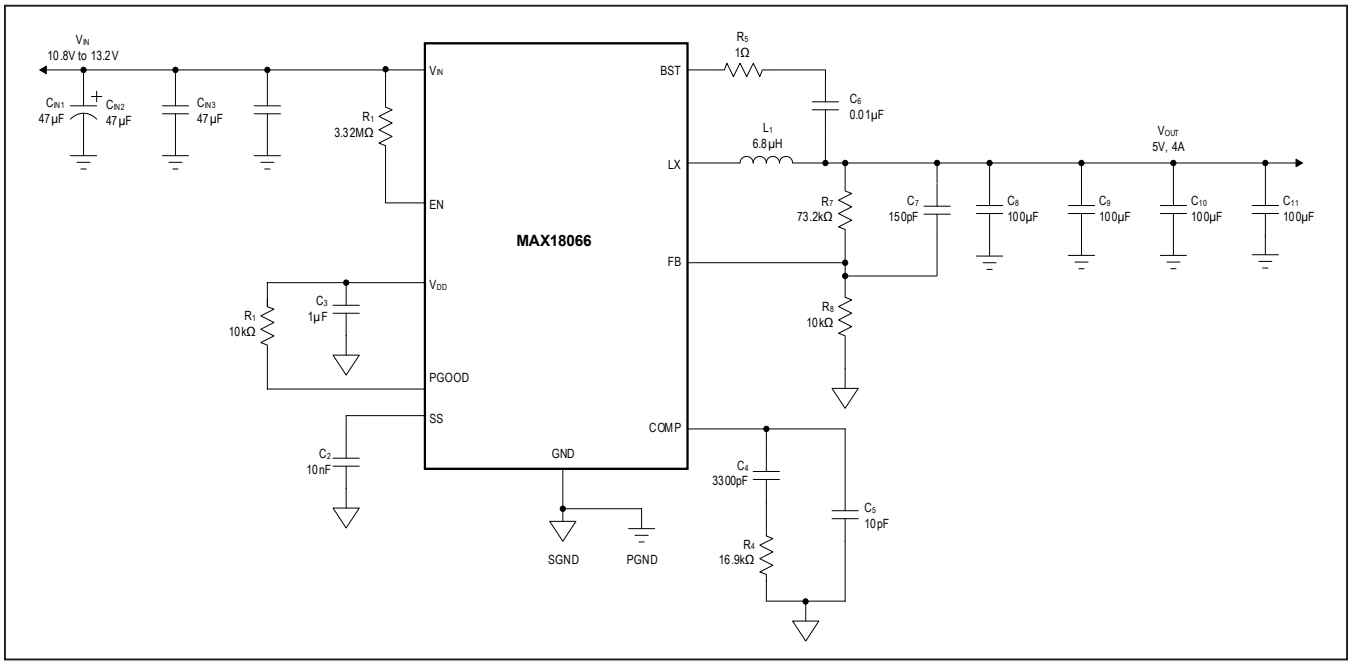

Figure 2. MAX18066 Circuit (5V Output, 4A Load Current, 500kHz Switching Frequency).

Step 3: Output Capacitor

The output capacitor is selected to support a step load of 50% of the load current specified in the design specifications, so the output-voltage deviation is contained to +/-3% of the output-voltage change. The output capacitance based on the Load Transient is determined by the load step current (ΔI_{LOAD}), the allowable output-voltage deviation (ΔV_{OUT_OS}), the target closed loop cross-over frequency (f_{CO}). The capacitance is calculated using the following equation provided in the data sheet:

$$C_{OUT} = \frac{\Delta I_{LOAD}}{3 f_{CO} \times \Delta V_{OUT\_OS}} = \frac{2}{3 \times 50000 \times 0.03 \times 5} = 88.9\mu F$$

The ESR of the output capacitor also affects the overall stability. Furthermore, the output capacitor chosen should be able to keep the output ripple within defined limits. The output ripple is composed of the output capacitance and ESR. The ripple due to the equivalent series inductance (ESL) is neglected. When using ceramic capacitors, which generally have low-ESR, ripple due to capacitance dominates. For calculation purpose, it is assumed that 90% of the total output ripple is contributed by capacitance.

$$\Delta V_{OUT} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$
$$V_{RIPPLE(C)} = 0.9 \times \Delta V_{OUT} = 0.9 \times 0.01 \times 5 = 45mV$$
$$V_{RIPPLE(ESR)} = 0.1 \times \Delta V_{OUT} = 0.1 \times 0.01 \times 5 = 5mV$$

The peak-to-peak inductor current is calculated using the following formula:

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{5}{500000 \times 0.0000068} \times \left(1 - \frac{5}{12}\right) = 0.86A$$

The output Capacitance and ESR is calculated based on ripple as below:

$$V_{RIPPLE(C)} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$
$$COUT_{min} = \frac{\Delta I_{P-P}}{8 \times V_{RIPPLE(C)} \times f_{SW}} = \frac{0.86}{8 \times 0.045 \times 500000} = 4.7\mu F$$
$$V_{RIPPLE(ESR)} = \Delta I_{P-P} \times ESR$$
$$ESR_{max} = \frac{V_{RIPPLE(ESR)}}{\Delta I_{P-P}} = \frac{0.005}{0.86} = 5.8m\Omega$$

The maximum of above calculated output capacitance values, which is 88.9µF, is considered for component selection. The nominal capacitance of the capacitor is derated based on the bias voltage. So, considering 20% tolerance, capacitors in parallel with total actual capacitance value greater than or equal to 106µF should be sufficient to achieve the specifications. The capacitor C3216X5R1A107M160AC shown in Figure 3 is chosen as it offers 28.76µF actual capacitance considering DC bias and 1.75mΩ of ESR. The voltage rating of the capacitor is 10V, which is significantly greater than the output voltage.

Step 4: Soft-Start Capacitor

The soft-start capacitor connected from the SS pin to GND programs the soft-start period. The soft-start is used to reduce the inrush current by ramping up the output voltage slowly. A longer soft-start time reduces the charging rate of the output capacitor and limits the inrush current.

The soft-start capacitor is related to the soft-start current and soft-start time by the following equation:

$$C_2 = \frac{I_{SS} \times t_{SS}}{V_{FB}} = \frac{5\mu A \times 1ms}{0.606V} = 8.25nF$$

The output capacitance (C_{OUT}) and the output voltage determine the minimum required soft-start capacitor by following the equation given below:

$$C_2 \geq \frac{C_{OUT} \times V_{OUT} \times I_{SS}}{(I_{HSCL} - I_{OUT}) \times V_{FB}}$$
$$C_2 \geq \frac{106\mu \times 5 \times 5\mu}{(7.7 - 4) \times 0.606}$$
$$C_2 \geq 1.182nF$$

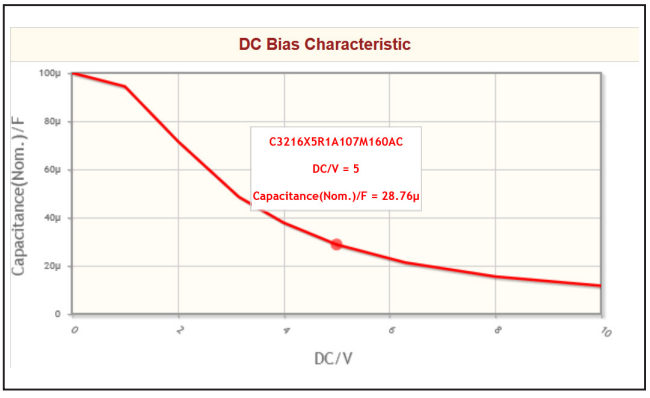

Figure 3. Output Capacitor DC Bias.

C_2 of 10nF which is sufficiently above the minimum requirement is chosen.

Step 5: Resistor Divider Network

The MAX18066 offers an adjustable output voltage from 0.606V to 90% of the Input Voltage. The output voltage is set by placing a resistor divider from V_{OUT} to the ground (GND) using resistors R_7 and R_8. A typical lower feedback resistor for R_8 is selected as 10kΩ±1% which is connected from FB to GND. The upper feedback resistor R_7 is calculated as:

$$R_7 = R_8 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$
$$= 10k \times \left(\frac{5}{0.606} - 1\right)$$
$$= 72.5k\Omega$$

Hence, R_7= 73.2kΩ ±1% is selected which is connected from V_{OUT} to FB.

Step 6: Compensation Network

1) Desired crossover frequency is chosen as $f_{CO} = f_{SW}/10 = 50kHz$.
2) As the MAX18066 is operated with peak current-mode control, type-II PI controller is used for compensation. The compensation resistor R_4 is calculated as follows:

$$R_4 = \frac{R_7 + R_8}{R_8} \times \frac{2\pi f_{CO} \times C_{OUT}}{g_{MV} \times g_{MC}}$$

Where g_{MV} = 1.6mS and g_{MC} = 9S are error-amplifier transconductance and current sense to COMP transconductance, respectively. Replacing the other parameters per selected components earlier, R_4 = 19.24kΩ

3) The compensation capacitor C_4 is calculated as below:

$$C_4 \geq \frac{5}{2\pi \times f_{CO} \times R_4}$$
$$C_4 \geq 827pF$$

4) The phase leading capacitor C_7 is added which helps to reduce the phase lag of the damped half-frequency double pole. Adding a second zero near but below the desired crossover frequency increases both the closed-loop phase margin and crossover frequency. The capacitor C_7 is calculated as follows:

$$C_7 < \frac{1}{2\pi \times f_{CO} \times (R_7 \,||\, R_8)}$$
$$C_7 < 362pF$$

5) To get a stable compensation network, the order of pole-zero must be as follows:

$$f_{P1} < f_{P2} \leq f_{Z1} < f_{CO} < f_{ZFF} < f_{P3} < f_{Z2}$$

The following equations are used to calculate the pole and zero locations. For more details, refer to the MAX18066 data sheet.

$$f_{P1} = \frac{g_{MV}}{2\pi \times C_4 \times 10^{AVEA(dB)/20}}$$

$$f_{P2} = \frac{1}{2\pi \times C_{OUT} \times \left(\frac{1}{R_{LOAD}} + \frac{[K_S \times (1-D) - 0.5]}{f_{SW} \times L}\right)}$$

Where, K_S is the slope compensation factor, D is the duty cycle and L is the inductance.

$$f_{P3} = \frac{f_{SW}}{2}$$
$$f_{Z1} = \frac{1}{2\pi \times R_4 \times C_4}$$
$$f_{Z2} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

6) The parallel compensation capacitor of C_5 = 10pF is selected for high frequency pole.
7) To get the pole-zero order as mentioned in the previous comment and based on the AC Loop simulation in EE-SIM shown in Figure 4, compensation components are selected as R_4 = 16.9kΩ ±1%, C_4 = 3300pF and C_7 = 150pF.

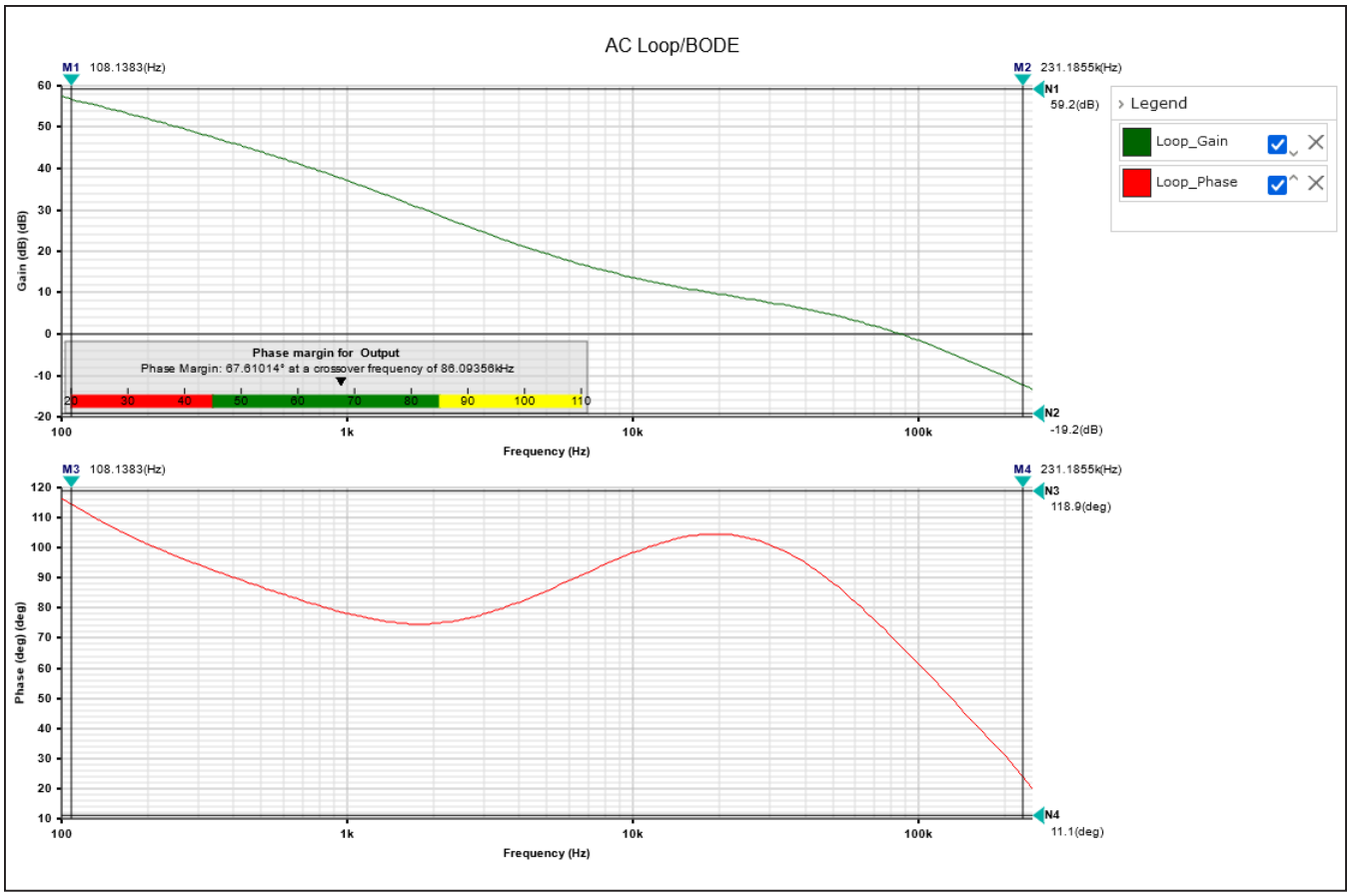

Figure 4. AC Loop Simulation using EE-SIM tool.

Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/21	Initial release	—