# 2.5V/3A, Synchronous Step-Down Converter Using the MAX18066

MAXREFDES1127

## Introduction

The MAXREFDES1127 demonstrates how to build a DC-DC buck converter using the MAX18066 for 2.5V DC output applications from a 10.8V to 13.2V input. This reference design delivers up to 3A at 2.5V output. This design uses a two-layer board.

The MAX18066 current-mode, synchronous, DC-DC buck converters deliver an output current up to 4A with high efficiency. The devices operate from an input voltage of 4.5V to 16V and provide an adjustable output voltage from 0.606V to 90% of the input voltage. The devices are ideal for distributed power systems, notebook computers, non-portable consumer.

The devices feature a pulse-width modulation (PWM) mode operation with an internally fixed switching frequency of 500kHz capable of 90% maximum duty cycle. The devices automatically enter skip mode at light loads. The current-mode control architecture simplifies compensation design and ensures a cycle-by-cycle current limit and fast response to line and load transients. Additional features include an externally adjustable soft-start, independent enable input and power-good output for power sequencing, and thermal shutdown protection. The devices offer overcurrent protection (high side sourcing) with hiccup mode during an output short-circuit condition. The devices ensure safe startup when powering into a pre-biased output.

## Hardware Specification

A small size, high-efficiency, synchronous step-down converter using the MAX18066 is shown for a 2.5V/3A application. Table 1 provides an overview of the design specification. The measured data and waveforms from the hardware set up can be found in the Test results.

### Table 1. Design Specification

| PARAMETER | SYMBOL | MIN | TYP | MAX |
|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | 10.8V | 12V | 13.2V |
| Frequency | $f_{SW}$ | | 500kHz | |
| Efficiency | η | | >85% | |
| Output Voltage | $V_{OUT}$ | | 2.5V | |
| Load Step | $I_{STEP}$ | | 2A to 3A | |
| Transient Deviation | $\Delta V_{OUT}$ | | 75mV | |
| Output Voltage Ripple | $V_{PK-PK}$ | | 25mV | |
| Output Current | $I_{OUT}$ | 0A | — | 3A |
| Output Power | $P_{OUT}$ | | 7.5W | |

## Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed, systematic technical guide for the design of a buck converter using the MAX18066 for high voltage and smaller size. For the device operation details, refer to the MAX18066 data sheet and the MAX18066 EV kit data sheet. The power supply has been built and tested, details of which follow later in this document.


*Figure 1. MAXREFDES1127 Hardware.*

## Quick Start

### Required Equipment

- AC-DC Power Supply: Chroma Systems 62015L-60-6
- Electronic Load: Keithley® 2380-120-60
- Oscilloscope: Teledyne® LeCroy® WaveSurfer® 3024z
- Multimeter: Keithley DMM6500

### Procedure

The reference design is fully assembled and tested. Follow these steps to verify board operation:

1) Connect the positive and negative terminals of the power supply to the input connector.
2) Set the power-supply voltage to 12V and the current limit to 3A.
3) Turn on the power supply.
4) Verify that $V_{OUT}$ is close to 2.5V using the digital multimeter (DMM).
5) Verify that the switching frequency is close to 500kHz by monitoring the switching node voltage with the oscilloscope.

## Design Procedure for a High-Efficiency Buck Converter

For this reference design, the design process is divided into the following stages:

- Output-Voltage Selection
- Inductor Selection
- Input Capacitor Selection
- Output Capacitor Selection
- Compensation Network
- BIAS Capacitor Selection
- Soft Start Capacitor Selection
- PCB Layout Guidelines

This document complements the information contained in the MAX18066 data sheet.

The following design parameters are used throughout this document:

$V_{IN}$ = Input voltage

$V_{OUT}$ = Output voltage

$I_{OUT}$ = Output current

$f_{SW}$ = Switching frequency

D = Duty cycle

$\Delta I_{L(P-P)}$ = Peak to Peak Inductor Ripple Current

### Step 1: Output-Voltage Selection

Set the output voltage using the R5 and R6 resistors. $V_{FB}$ is the internal reference voltage, and its minimum value is 0.6V.

$$R5 = R6\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

Setting $V_{OUT}$ = 2.5V and $V_{FB}$ = 0.6V gives

$$R5 = R6 \times 3.1667$$

select R6 = 10kΩ, which gives R5 = 31.6kΩ.

### Step 2: Inductor Selection

Inductor is selected based on LIR. LIR is the ratio of the peak-to-peak inductor current ripple to the average value of the inductor current. We have chosen an inductor value to produce a current ripple ($\Delta I_L$) equal to 50% of load current, giving a LIR of 0.5.

Inductance value required to meet the current ripple:

$$L1 = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times I_{OUT} \times LIR}$$

$$= \frac{(12 - 2.5) \times \left(\frac{2.5}{12}\right)}{500k \times 3 \times 0.5}$$

$$= 2.63uH$$

Off the shelf inductor of 2.2µH is chosen.

Additionally, we must ensure that the following relationships are satisfied:

$$I_{LSAT} > I_{PEAK} = I_{OUT} + \frac{\Delta I_{L(P-P)}}{2}$$

and

$$I_{LRMS} > I_{RMS} = \sqrt{I_{OUT}^2 + \frac{1}{12}\Delta I_{L(P-P)}^2}$$

and

$$\Delta I_{L(P-P)} = \frac{V_{OUT}}{f_{sw} \times L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where,

$I_{LSAT}$ - Rated Saturation Current of the Inductor

$I_{LRMS}$ - Rated RMS Current of the Inductor

$I_{PEAK}$ - Peak Current through the Inductor

$I_{LRMS}$ - RMS Current through the Inductor

Hence:

$$I_{PEAK} = 3.9A$$
and
$$I_{RMS} = 3.045A$$

We choose the Coilcraft® XAL1060-222ME with 2.2µH inductance and 20A $I_{LSAT}$ and 24A $I_{LRMS}$ saturation current.

## Step 3: Input Capacitor Selection

The input capacitor RMS current requirement ($I_{RMS}$) is defined by the following equation:

$$I_{RMS} = \frac{I_{OUT(MAX)} \times \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where $I_{OUT(MAX)}$ is the maximum load current. $I_{RMS}$ has a maximum value when the input voltage equals twice the output voltage ($V_{IN}$ = 2 x $V_{OUT}$), so $I_{RMS}$ = $I_{OUT(MAX)}$/2. Required RMS current rating of the input capacitor is 1.5A.

The following equation shows the capacitor requirement for a target voltage ripple at the input:

$$C_{IN} = \frac{I_{OUT} \times \left(\frac{V_{OUT}}{V_{IN}}\right)}{f_{SW} \times \Delta V_Q}$$

$I_{OUT}$ is the maximum output current in amps and $f_{SW}$ is the switching frequency. Input capacitor is designed for an Input voltage ripple ($\Delta V_Q$) of 1%. Here $C_{IN}$ = 12.86µF. Due to the capacitor's DC bias characteristic and temperature characteristics, some margin should be reserved. We have used a combination of ceramic and electrolytic capacitors to meet both the capacitance and RMS current requirement. Hence, we have chosen Electrolytic capacitance = 47µF and Ceramic capacitance = (10µF || 0.1µF) for this design.

## Step 4: Output Capacitor Selection

Use the following equations to calculate the output capacitance value due to load transient:

$$C_{OUT} = \frac{\Delta I_{LOAD}}{3 \times f_{CO} \times \Delta V_{OUT}}$$

$\Delta I_{LOAD}$ is the load step current in amps and $f_{CO}$ is the unity gain bandwidth (or zero-crossing frequency). Output capacitor is designed for an output voltage overshoot of 3% for 1A load change and zero-crossing frequency of 50kHz. Here $C_{OUT}$ is calculated as 88.88µF. Due to the capacitor's DC bias characteristic and temperature characteristics, some margin should be reserved. Hence ceramic capacitors of capacitance = 2×47µF is used in this design.

For the capacitance chosen the output voltage ripple due to ESR and capacitance are calculated as:

$$\Delta V_{ESR} = ESR_{OUT} \times \Delta I_{L(P-P)}$$

$$\Delta V_Q = \frac{\Delta I_{L(P-P)}}{8 \times C_{OUT} \times f_{SW}}$$

$\Delta V_{ESR}$ is calculated as 3mV and $\Delta V_Q$ is calculated as 4.82mV. So, the total output voltage ripple comes as 7.82mV which is within the specified limit of 25mV.

## Step 5: Compensation Network

The IC uses the current mode-control scheme for a buck controller. A series resistor (R7) and a capacitor (C13) is required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering. For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a non-ceramic output-capacitor loop, add another compensation capacitor (C14) from COMP to GND to cancel this zero.

We chose R7 = 5.11kΩ, C13 = 8.2nF and C14 = 120pF. An additional RC circuit was added across the top feedback resistor to boost the phase margin. A R5 = 31.6kΩ and C15 = 820pF are selected.

## Step 6: Bias Capacitor Selection

The internal circuitry of the IC requires a 5V bias supply. An internal 5V linear regulator generated this supply. The $V_{DD}$ pin is bypassed with a 1µF ceramic capacitor (C4) to guarantee stability under full-load condition.

## Step 7: Soft Start Capacitor Selection

The devices utilize a soft start feature to ramp up the regulated output voltage slowly to reduce input inrush current during startup. Connect a capacitor of 0.1uF (C7) from SS to GND to set the startup time to 12ms.

## Step 8: PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching power losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity.

Follow the guidelines below for a good PCB layout:

- All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. If the loop area is made very small, then the inductance reduces because the inductance of a current-carrying loop is proportional to the area enclosed by the loop. Additionally, small current loop areas reduce radiated EMI.
- A ceramic input filter capacitor should be placed close to the IC's $V_{IN}$ pins. Also, its ground loop to GND should be short. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bias capacitor for the $V_{DD}$ pin should also be placed close to the pin to reduce the effects of trace impedance. Its ground loop to GND should be short.
- When routing circuitry around the IC, the analog small-signal ground and power ground for switching currents must be kept separate. They should be connected where switching activity is minimal, typically the return terminal of the $V_{DD}$ bias capacitor. Doing so helps keep the analog ground quiet. The ground plane should be kept continuous and unbroken as far as possible. No trace-carrying, high-switching current should be placed directly over any ground plane discontinuity.
- PCB layout also affects the thermal performance of the design. A few thermal vias that connect to a large ground plane should be provided under the IC's exposed pad for efficient heat dissipation. The PCB size, copper thickness, and board layer numbers affect the temperature dissipation capacity of the board. For this reference design, it can support a 3A load current with 2oz of copper, two layers, and 61mm x 46mm board.

## Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 8/21 | Initial release | — |