Low EMI, 5V/3.5A, Synchronous Buck DC-DC Converter Using the MAX17504

MAXREFDES1049

Introduction

The MAXREFDES1049 is a DC-DC buck power supply that delivers up to 3.5A at 5V from a 7.5V to 60V supply voltage. It is designed for equipment that needs to pass the electromagnetic interference (EMI) compliance testing.

The MAXREFDES1049 employs techniques that use the buck regulators to generate voltage lower than the input voltage. This document explains how the MAX17504 peak-current-mode PWM converter can be used to generate 5V from an input voltage of 7.5V to 60V. This document also illustrates how to achieve high EMI performance using a proper filter with good PCB layout and shielding techniques. This reference design passed the conducted emission (CE) test of CISPR 22 class B. An overview of the design specification is shown in Table 1.

The MAX17504 high-efficiency, high-voltage, synchronously rectified step-down converter with dual integrated MOSFETs operates over a 4.5V to 60V input. The converter can deliver up to 3.5A and generate output voltage from 0.9V to 90% V_{IN}. Built-in compensation across the output voltage range eliminates the need for external components. The feedback (FB) regulation is accurate to within ±1.1% over -40°C to +125°C. The device is available in a compact (5mm x 5mm) TQFN lead (Pb)-free package with an exposed pad. Simulation models are available.

Designed–Built–Tested

This reference design describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to design a buck converter using the MAX17504 step-down controller. The EMI line filter selection and PCB layout are also introduced in this document. The power supply has been built and tested, details of which follow later in this document.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	7.5V	60V
Switching Frequency	f_{SW}	500kHz	
Peak Efficiency	η	93%	
Duty Cycle	D	8%	67%
Output Voltage	V_{OUT}	4.97V	5.05V
Output Current	I_{OUT}	0A	3.5A
Output Voltage Ripple	ΔV_{OUT}	50mV	
Output Power	P_{OUT}	17.5W	

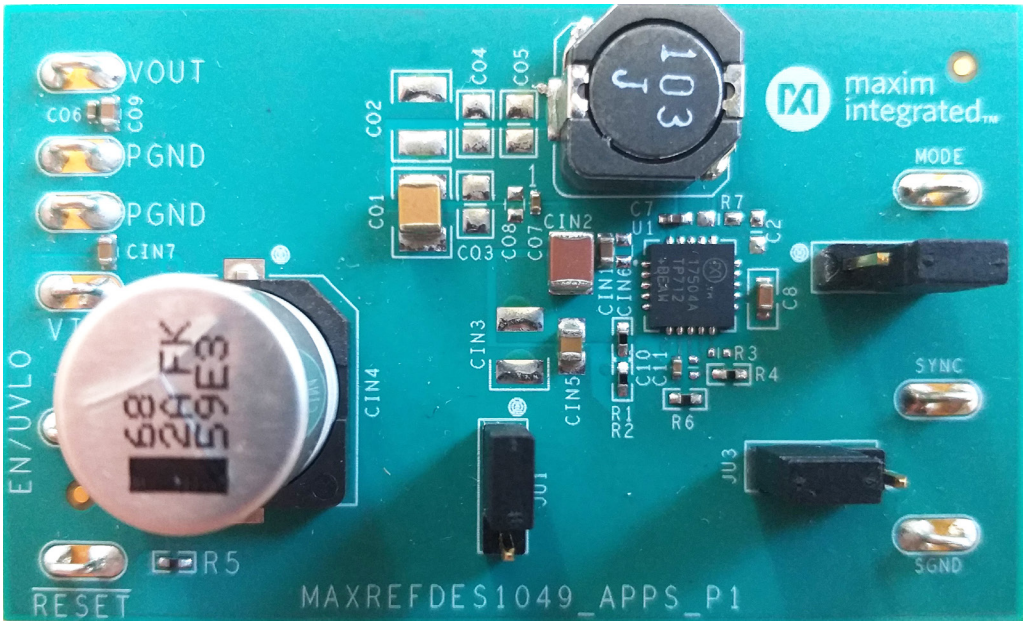

Figure 1. MAXREFDES1049 hardware.

Synchronous Buck Converter

In low-voltage, high-current applications, synchronous buck converters are more efficient than conventional buck converters because synchronous converters use MOSFETs, rather than conventional catch diodes. As a result, the power they dissipate in off-periods is reduced significantly. In a steady state, the low-side MOSFET is driven to complement the high-side MOSFET. In other words, whenever one of these switches is on, the other is off. In steady-state conditions, the complementary switching of high-side and low-side MOSFETs regulates V_{OUT} to its set value.

Figure 2 is a simple circuit diagram of the basic operation of a synchronous buck converter. The main operation depends on the current in the inductor operated through the Q1 main switch (generally a MOSFET) and the Q2 secondary switch. Initially, when Q1 is in the on-state and Q2 is in the off-state, the current starts flowing from the source through Q1, the inductor, and then to the load. The operation time of Q1 depends on the duty cycle. The current through the inductor then charges the inductor. During this interval, when the switch is in the on-state, Q2 is in reverse bias and does not conduct.

For the next interval, when Q1 is in the off-state, the charged energy stored in the inductor starts discharging, at which time the circuit must be closed. Because the inductor is being discharged, the polarities of the inductor reverse, and the Q2 conducting state becomes forward-biased. When the duty cycle is very low, the inductor's charging time is less than the discharging time. Because Q2 is in the on-state during the discharging time, Q2 conducts for a longer period than Q1.

The synchronous rectifier switch is open when the main switch is closed and vice versa. To prevent cross-conduction when both the top and bottom switches are on simultaneously, a break-before-make switching scheme must be employed. A diode must continue to conduct during the interval between the opening of the main switch and the closing of the synchronous-rectifier switch (dead time). When a MOSFET is used as a synchronous switch, the current normally flows in reverse (i.e., source to drain), which allows the integrated body diode to conduct current during the dead time. When the synchronous rectifier switch closes, the current flows through the MOSFET channel. Because of the low-channel resistance for power MOSFETs, the standard forward drop of the rectifying diode can be reduced to a few millivolts. Synchronous rectification can provide efficiencies well above 90%.

Figure 3 shows various waveforms for the synchronous buck topology. During the first cycle when Q1 conducts, the input current gradually rises and flows through the inductor and capacitor. This results in the energy being stored in the inductor and the capacitor. During the second cycle, Q1 turns off, and after some dead time, Q2 turns on. This results in the energy stored in the magnetic field of the inductor being released back into the circuit. As the energy stored in the inductor dissipates, the capacitor starts discharging and keeps the current flowing until the next cycle.

Note that the MOSFETs Q1 and Q2 cannot be on simultaneously, as this results in the input being connected to the ground. Therefore, a time interval, such as dead time, must be present between the on-states of the MOSFETs.

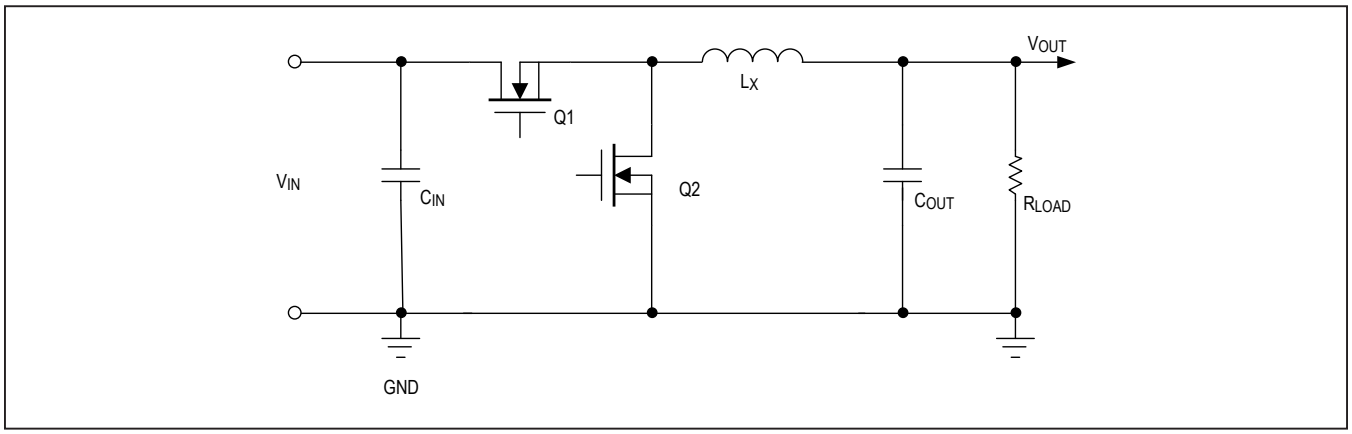

Figure 2. Synchronous buck converter topology.

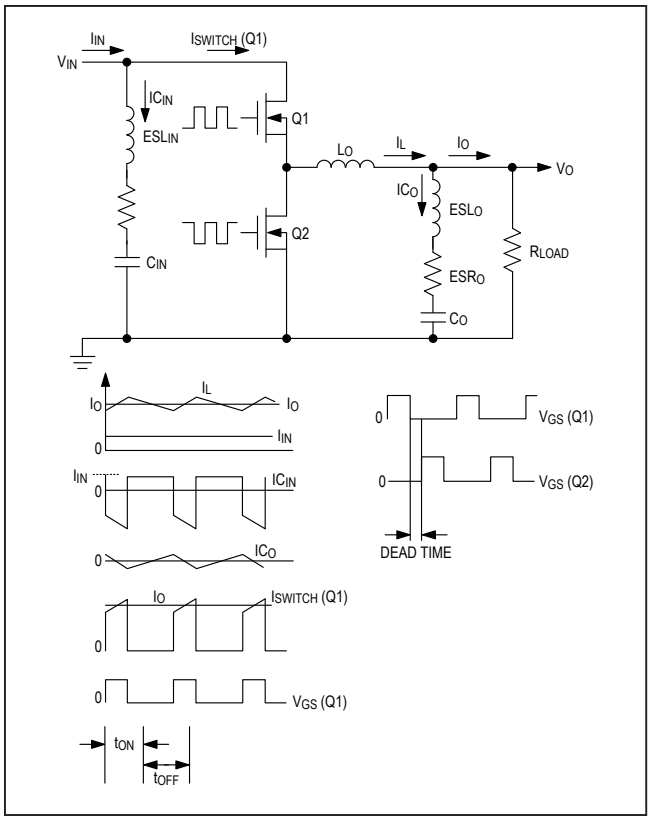

Figure 3. Synchronous buck waveforms.

Design Procedure for a High-Efficiency Buck Converter

For this reference design, the design process is divided into the following stages: switching frequency selection, inductor and capacitor selection, output voltage selection, EMI filter design, and PCB layout guidelines. This document complements the information contained in the MAX17504 data sheet.

The following design parameters are used throughout:

V_{IN} = Input voltage

V_{OUT} = Output voltage

I_{OUT} = Output current

f_{SW} = Switching frequency

D = Duty cycle

Step 1: Selecting the Switching Frequency

The switching frequency of the MAX17504 can be programmed from 100kHz to 2.2MHz by using a resistor connected from RT to SGND. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} \cong \frac{21 \times 10^3}{f_{SW}} - 1.7$$

where R_{RT} is in kiloohms and f_{SW} is in kilohertz. Leaving the RT pin open causes the device to operate at the default switching frequency of 500kHz. 500kHz is chosen for this reference design.

Step 2: Selecting the Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces the noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 × V_{OUT}), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}$/2=1.75A.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high ripple current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where D is the duty ratio of the controller (D = V_{OUT}/V_{IN}), f_{SW} is the switching frequency, ΔV_{IN} is the allowable input voltage ripple, and η is the efficiency.

In applications where the source is located far from the MAX17504 input, add an electrolytic capacitor in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor. Additional ceramic capacitors with a low value (i.e., 0.1µF or 0.01µF) placed at the input could bypass high frequency noise and improve EMI performance.

Step 3: Selecting the Inductor

Three key inductor parameters must be specified for device operation: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductance value as shown in the following equation:

$$L = \frac{V_{OUT}}{f_{SW}} = \frac{5V}{500 \times 10^3 Hz} = 10\mu H$$

where V_{OUT} and f_{SW} are nominal values.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The inductor saturation current (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value of 5.1A.

Step 4: Selecting Output Capacitors

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output voltage deviation is contained to 3% of the output voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{2}{f_{SW}} \right)$$

where I_{STEP} is the step load current, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, f_C is the target closed-loop crossover frequency, and f_{SW} is the switching frequency. For the MAX17504, select f_C to be 1/9th of f_{SW} if the switching frequency is less than or equal to 500kHz. If the switching frequency is more than 500kHz, select f_C to be 55kHz. Derating of ceramic capacitors with DC voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor vendors.

Step 5: Setting the Output Voltage

The MAX17504 delivers up to 3.5A and 0.9V to 90% V_{IN} output voltage. Set the output voltage with a resistive voltage-divider connected from the positive terminal of the output capacitor (V_{OUT}) to SGND. Connect the center node of the divider to the FB pin. Calculate resistor R4 from the output to FB as follows:

$$R_4 = \frac{216 \times 10^3}{f_C \times C_{OUT}}$$

where R4 is in kiloohms, f_C is in kilohertz, and C_{OUT} is in microfarads.

For the MAX17504, choose f_C to be 1/9th of the switching frequency (f_{SW}) if the switching frequency is less than or equal to 500kHz. If the switching frequency is more than 500kHz, select f_C to be 55kHz. For the MAX17504S, select f_C to be 1/10th of fSW if f_{SW} is less than or equal to 1MHz. If f_{SW} is more than 1MHz, select f_C to be 100kHz.

Calculate resistor R6 from FB to SGND as follows:

$$R_6 = \frac{R_4 \times 0.9}{(V_{OUT} - 0.9)}$$

Step 6: Design for the EMI Compliance

This reference design used Application Note 6729: *Mitigating EMI for a CISPR 22-Compliant Power Solution* to design the EMI line filter and layout the PCB. For the detailed theory of conducted and radiated emission, refer to Application Note 6729: *Mitigating EMI for a CISPR 22-Compliant Power Solution*.

Design for the EMI Line Filter

A π-filter, shown in Figure 4, placed between the input source and the power converter reduces the conducted emissions from the power converter. Select the filter components by performing the following steps:

- Determine the input impedance (R_{IN})
- Design the EMI filter

To determine R_{IN}, first calculate the output load (R_O) and the operating duty cycle (D) by using the following equations:

$$R_O = \frac{V_O}{I_O} = \frac{5V}{3.5A} = 1.43\Omega$$

$$D_{MAX} = \frac{V_O}{V_{IN(MIN)}} = \frac{5V}{7.5V} = 0.67$$

The worst-case closed-loop input impedance of a buck converter for all frequency is then determined as follows:

$$D_{MAX} = \frac{V_O}{V_{IN(MIN)}} = \frac{5V}{7.5V} = 0.67$$

The minimum input impedance occurs when the converter is operating at minimum input supply voltage.

Next, design the EMI filter with an output impedance that is less than 10db lower than R_{IN}. The addition of the input filter can affect the performance of the DC-DC converter. To minimize the effect, the output impedance of the filter must always be less than the input impedance of the power converter for all frequencies up to the converter's crossover frequency.

The output impedance of the LC filter at its highest value, the resonance frequency, is 10dB less than the input impedance of the buck converter, which is approximately equal to one-third of the input impedance (1.1Ω).

PCB Layout for EMI Compliance

The PCB layout has a significant effect on the EMI compliance. A bad PCB layout can ruin a power converter with perfect electrical design. For this reference design, some of the best practices to minimize EMI noise sources in a PCB layout are to minimize high di/dt current loops and to use a Faraday shield.

To minimize high di/dt current loops, place L_O, C_O, and S_2 close together to minimize the I_2 current loop. Place this entire group of components close to S_1 and C_I to also minimize the I_1 current loop. Figure 5 shows L_O, C_O, S_2, I_2, S_1, C_I, and I_1.

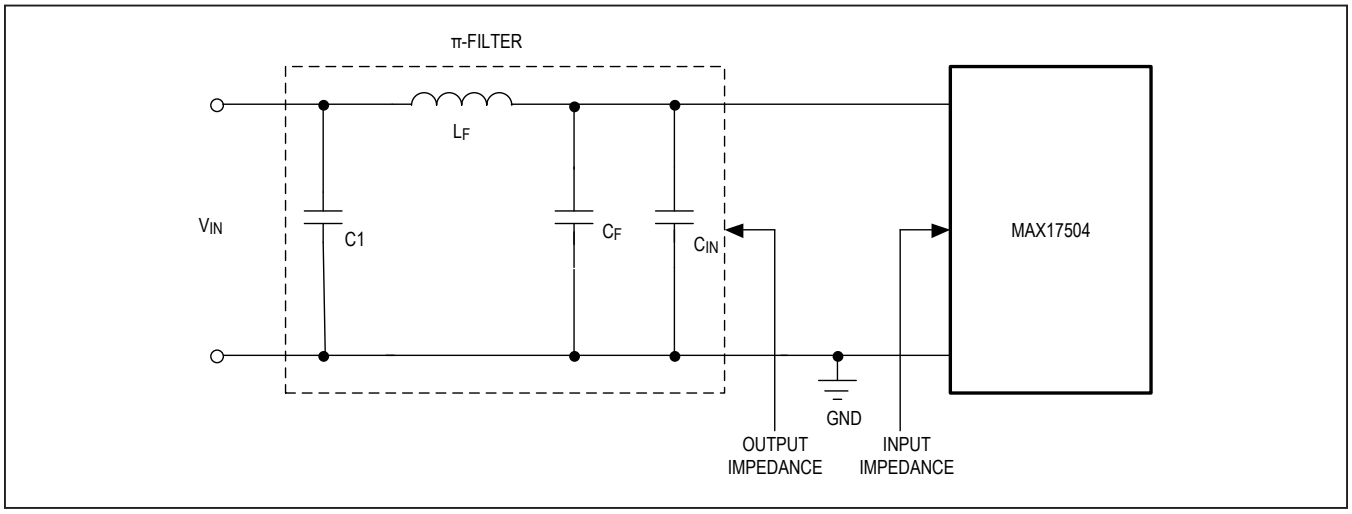

Figure 4. Conducted EMI input filter, inserted between input and a power module.

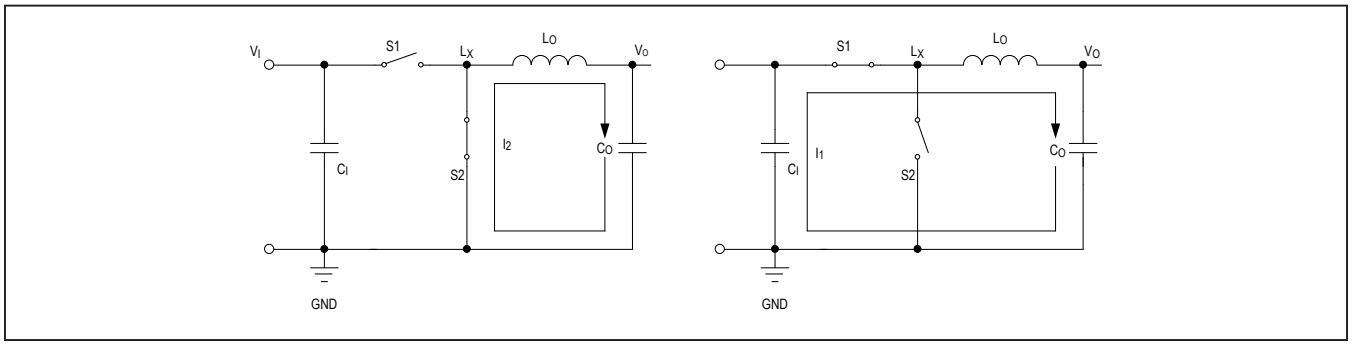

Figure 5. Buck converter's high di/dt current loops.

A Faraday shield or cage is an enclosure used to block electromagnetic fields. Two common ways to implement a Faraday shield in a power system are as follows:

- A cage made of conductive material (such as copper) that encloses the entire power system or equipment. The electromagnetic field is contained inside the cage. However, this approach is usually expensive because of the cost of the cage material and additional assembly labor.
- A layout with shielding ground planes on both the top and bottom of the PCB connected by a via to mimic a Faraday cage. All high di/dt loops are placed in the inner layers of the PCB so that the Faraday cage shields the magnetic field from radiating outward. This method, depicted in Figure 6, is at a lower cost and usually adequate to contain EMI.

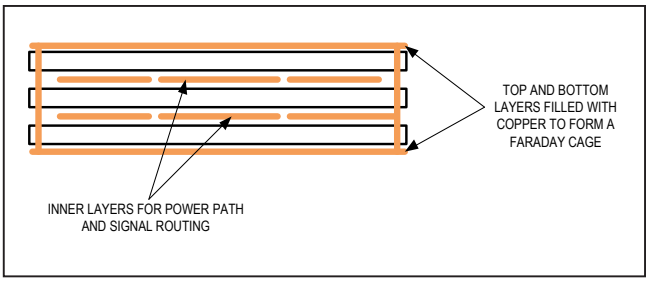

Figure 6. Faraday shield applied on a multi-layer PCB board.

Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/19	Initial release	—