# Automotive 1.3MP Camera Module with Power over Coax Using the MAX96707

MAXREFDES1041#

## Introduction

The MAXREFDES1041 is an automotive camera module design using the MAX96707. The reference design contains the AR0143 1.3MP image sensor, which outputs RAW, 8-bit parallel image data to the MAX96707serializer. The MAX96707 serializes the image data and outputs the valid pixel data together with the HSYNC, VSYNC, and control signal through one coax cable.

Main features include the following:

- Meets AEC-Q100 Automotive Specification
- Works with all Maxim GMSL Deserializers
- Supports Power over Coax (PoC)
- Reduces EMI and Shielding Requirements
- Allows 15m Coax Cable with Multiple Inline Connectors
- Used in ADAS Camera Systems

## Hardware Specification

The MAXREFDES1041 includes the following major components: serializer, image sensor, and two power-management ICs (PMICs). The design is powered through 7V~12V PoC. The image sensor captures the image, then outputs the image data through the digital video parallel (DVP) interface. Then, the serializer serializes the parallel signal to a serial signal and outputs that signal through the coax cable. The PMICs are used as power supply for the sensor and serializer.

### Table 1. Design Specification

| PARAMETER | SYMBOL | MIN | TYP | MAX |
|---|---|---|---|---|
| Power Supply | $V_{CC}$ | 5V | 8V | 17V |
| Supply Current | $I_{CC}$ | — | 0.264A | — |

## Designed – Built – Tested

This document describes the hardware shown in Figure 1 and Figure 2. It provides a detailed, systematic technical guide to design an automotive camera application using the MAX96707. This reference design includes two boards: a sensor board and a power board. The sensor board includes the MAX96707 serializer and the ON Semiconductor® AR0143 image sensor. The power board includes a power over coax (PoC) filter circuit, DC/DC power regulator circuits, and a coax cable connector. The system has been built and tested, details of which follow later in this document.

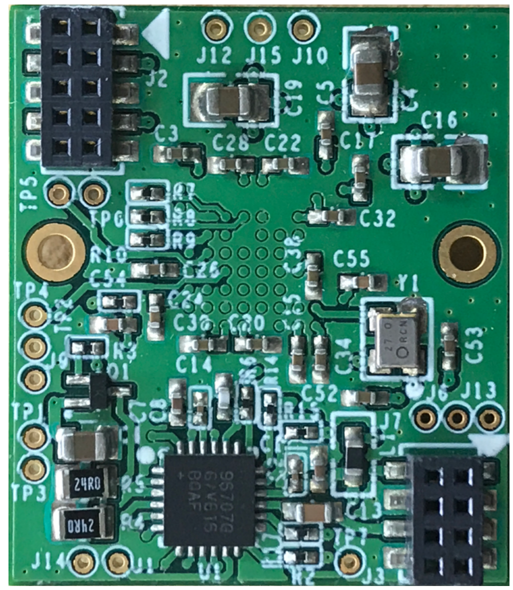

*Figure 1. MAXREFDES1041 sensor board.*

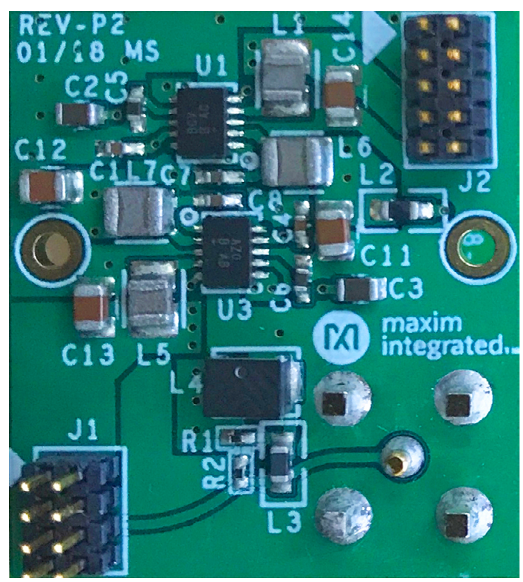


*Figure 2. MAXREFDES1041 power board.*

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## Design Procedure

### Step 1: PoC Design

This design uses PoC for the power supply. The goal of the PoC filter circuit is to deliver a clean DC supply to the input of the switching regulators. The PoC process involves four steps: filtering power, allowing for voltage loss, minimizing power noise, and increasing noise margin.

#### Filtering Power

The signal on the cable has a forward channel and a reverse channel. For the forward channel, the maximum data rate is 1.74Gbps and the minimum data rate is 500Mbps, which corresponds to a bandwidth requirement of 250MHz to 870MHz. As the filter for the forward channel, we chose a MPZ1608S601A ferrite bead, which has a resistance of over 300Ω from 100MHz to 1000MHz. For the reverse channel, the frequency is fixed at 1MHz, so we chose a 47μH inductor to filter 1MHz noise.

#### Allowing for Power Loss

The recommended voltage level of the PoC source for this design is 7V~12V. If the power sourcing is lower than 7V, then we must also calculate the total DC resistance to check whether the components are suitable for power loss. Assuming that the PoC supply voltage from the deserializer is 5V and from the regulator $V_{OUT}$-$V_{IN}$ is 0.2V, the regulator output is 3.3V. Therefore, the allowable voltage drop should be less than 1.3V. Table 2 shows the DC resistance for components in the power line.

The supply current for the AR0143 sensor is 200mA. Using Ohm's Law of IR = V, we find that 200mA x 2.75Ω = 0.55V < 1.3V, which meets the requirements.

#### Power Noise Reduction

The camera sensor has a lot of circuitry that is idle during blanking pixels. Therefore, the current goes up and down at both line rate and frame rate, which will generate power noise. The horizontal sync signal follows active/blanking pixels. In the circuit, a RZE002P02 MOSFET is used to increase the current when a blanking pixel occurs.

#### Increasing Noise Margin

The MAX96707 has a high-immunity mode, which can increase the noise margin for the device. Pulling up the GPO/HIM pin high through a resistor can set the device into high-immunity mode.

### Step 2: DC/DC Power Design

#### Selecting Regulators

Because this reference design is targeted at automotive applications, there are a few considerations when choosing the regulators and other components.

- The total solution size must be as tiny as possible, which means it is best to choose regulators that integrate MOSFETs, compensation networks, and feedback resistor-dividers to eliminate external circuitry.
- The regulator must be AEC-Q100 rated.
- The power rails for the MAX96707 are:
  - $V_{DVDD}$ = $V_{AVDD}$ = 1.8V
  - $V_{IODD}$ = 1.8V~3.6V
- The power rails for the AR0143AT are:
  - $V_{DVDD}$ = 1.2V
  - $V_{AVDD}$ = 2.8V
  - $V_{IODD}$ = 1.8V or 2.8V

After considering all of these requirements, we chose the MAX20019ATBD/V+ and MAX20019ATBB/V+ for the power supply, both of which are 500mA, dual step-down converters for automotive cameras. The MAX20019ATBD/V+ can provide 2.8V and 1.2V, while the MAX20019ATBB/V+ can provide 1.8V.

### Table 2. Component DC Resistance

| COMPONENT | | COMPONENT LENGTH (m) | RESISTANCE (Ω) | DC RESISTANCE TOTALS (Ω) | NOTES |
|---|---|---|---|---|---|
| Connector pairs | Rosenberger® FAKRA connectors | 2 | 0.1 | 0.2 | One connector pair at serializer, one at deserializer |
| Cable(s) | Leoni 302 | 15 | 0.1 | 1.5 | Sum of core and shield resistance per meter |
| L3 | MPZ1608S601A | 1 | 0.15 | 0.15 | — |
| L4 | ADL3225V-470M | 1 | 0.9 | 0.9 | — |
| R Total | — | — | — | 2.75 | — |

*Rosenberger is a registered trademark of Rosenberger Hochfrequenztechnik GmbH & Co.*

### Selecting Output Inductors

Three key inductor parameters must be specified for operation with the regulators: inductance value (L), inductor saturation current (ISAT), and DC resistance (RDC). To select the inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency (which is fixed at 2.2MHz), input voltage, output voltage, and selected LIR then determine the inductor value as Table 3 shows.

In this design, we chose L6 = 3.3µH, L7 = 3.3µH, L1 = 2.2µH, and L2 = 2.2µH.

### Selecting Output Capacitors

The minimum output capacitance should be 22µF ceramic with an X7S or X7R rating. The value and quality of this capacitor is critical, as it sets the dominant pole of the loop.

### Selecting Input Capacitors

The recommended system input capacitor is 10µF with and X5R rating or better. The input capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

## Step 3: Sensor Board Design

### External Clock Source for AR0143

In this design, a 27MHz clock source is needed for the camera sensor. The Kyocera® KC2520B27 was chosen.

### Connection between AR0143 and MAX96707

The deserializer output pins (DOUT(11:0)) are the parallel data output protocol for the sensor, and they are connected to the serializer input pins (DIN(11:0)) of the MAX96707. The AR0143 FRAME_VALID pin is connected to the MAX96707 DIN13/VS pin for vertical sync. The AR0143 LINE_VALID pin is connected to the MAX96707 DIN12/HS for horizontal sync.

## Step 4: Layout Guidelines

### Power-Supply Circuits and Bypassing for MAX96707

The serializer uses an AVDD and DVDD of 1.7V to 1.9V. All inputs and outputs, except for the serial output, derive power from DVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

### High-Frequency Signals

Separate the LVCMOS logic signals and CML/coax high-speed signals to prevent crosstalk. Use at least a four-layer PCB with separate layers for power, ground, CML/coax, and LVCMOS logic signals. Use a 50Ω trace for the single-ended output when driving coax. Route the PCB traces for differential CML in parallel to maintain the differential characteristic impedance. Avoid via arrays. Keep PCB traces that make up a differential pair equal in length to avoid skew within the differential pair.

### Power over Coax Circuits

Traces should be the same width as normally used for power traces carrying 0.5A. For best results, note that wider traces have lower DC resistance and inductance. Good practices are to keep trace width equal to the width of the smallest component, have a ground plane underneath traces and components, and arrange components to give the shortest trace possible. Place the smallest inductor as close as possible to the high-speed trace to minimize high-frequency attenuation. Make the inductor and damping resistor pads part of the trace, rather than making them a stub. Traces should only have curves or angles of 45 degrees or less (try to avoid the use of right angles); rotate the surface-mount components to accommodate, if necessary.

## Table 3. Inductor Values for Typical $V_{IN}$, $V_{OUT}$, and $I_{OUT}$ Requirements

| $V_{SUP}/V_{OUT}$ (V) | 12/3.3 | 8/3.3 | 7/3.3 | 7/2.8 | 3.3/1.8 | 2.8/1.8 |
|---|---|---|---|---|---|---|
| **Inductor(µH), $I_{LOAD}$ = 300mA** | 10 | 6.8 | 6.8 | 6.8 | 2.2 | 2.2 |
| **Inductor(µH), $I_{LOAD}$ = 300mA** | 8.2 | 4.7 | 3.3 | 3.3 | — | — |

*Kyocera is a registered trademark of Kyocera Corporation.*

### Step 5: Reverse Control Channel Initialization

The MAX96707 serializer can pair with any Maxim deserializer parts. If using the MAX9286 as the deserializer, the device address of the MAX9286 is 0x90 and the device address of the MAX96707 is 0x80. The steps to initialize the $I^2C$ connection between the serializer and deserializer in high-immunity mode are shown in Table 4.

Once the initialization setup for the $I^2C$ connection for the MAX9286 and MAX96707 is complete, the reverse control channel can directly access the AR0143AT through address 0x20. For detailed register settings of the AR0143AT, see the AR0143 data sheet.

## Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

### Table 4. Reverse Channel Setup Procedure

| STEP | OPERATION | DEVICE | SLAVE ID | REGISTER | VALUE | NOTES |
|---|---|---|---|---|---|---|
| H1 | Read | Des | 0x90 | 0x1C | 0xXX | Read register 0x1C to read the value of the reserved bits. |
| H2 | Write | Des | 0x90 | 0x1C | 0xFX | Set the deserializer to high-immunity mode. |
| H3 | Delay | — | — | — | 2ms | Wait 2ms after any change to reverse the channel settings. |
| H4 | Write | Ser | 0x80 | 0x4D | 0xC0 | Set the serializer to coax and high-immunity mode. |
| H5 | Delay | — | — | — | 2ms | Wait 2ms after any change to reverse the channel settings. |
| H6 | Write | Des | 0x90 | 0x1C | 0xFX | Set the deserializer to high-immunity mode. |
| H7 | Delay | — | — | — | 2ms | Wait 2ms after any change to reverse the channel settings. |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/19 | Initial release | — |