4A, 1.8V Step-Down DC-DC Converter with Integrated Switches Using MAX15050

MAXREFDES1021

Introduction

The MAX15050 is a high-efficiency switching regulator that delivers up to 4A load current at output voltages from 0.6V to (0.9 x V_{IN}). The device operates from 2.9V to 5.5V, making it ideal for on-board point-of-load and postregulation applications. The total output-voltage accuracy is within ±1% over load, line, and temperature.

The MAX15050 features 1MHz fixed-frequency PWM operation, and pulse-skip mode to improve light-load efficiency. The high operating frequency allows for small-size external components. The low-resistance on-chip nMOS switches ensure high efficiency at heavy loads while minimizing critical parasitic inductances, making the layout a much simpler task with respect to discrete solutions.

The device incorporates a high-bandwidth (> 26MHz) voltage-error amplifier. The voltage-mode control architecture and the voltage-error amplifier permit a Type III compensation scheme to achieve maximum loop bandwidth, up to 200kHz. High loop bandwidth provides fast transient response, resulting in less required output capacitance and allowing for all-ceramic capacitor designs.

The output overload hiccup protection and peak current limit on both high-side and low-side MOSFETs provide for ultra-safe operation in the cases of short-circuit conditions, severe overloads, or in converters with bulk electrolytic capacitors.

The output voltage is adjustable by using two external resistors at the feedback or by applying an external reference voltage to the REFIN/SS input.

The MAX15050 offers a programmable soft-start time using one capacitor to reduce input inrush current. A built-in thermal shutdown protection ensures safe operation under all conditions. Other features include the following:

- 20µA Startup Current in UVLO
- Programmable Input Undervoltage Lockout
- Programmable Input Overvoltage Protection
- Switching Frequency Synchronization
- Adjustable Soft-Start
- Programmable Slope Compensation
- Fast Cycle-by-Cycle Peak Current Limit
- 70ns Internal Leading-Edge Current-Sense Blanking
- Hiccup Mode Output Short-Circuit Protection

Hardware Specification

In this document, a step-down DC-DC converter using the MAX15050 is demonstrated for a 1.8V output application. The power supply delivers up to 4A at 1.8V. Table 1 shows an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	2.9V	5.5V
Frequency	f_{SW}	1MHz	
Efficiency	η	90%	
Output Voltage	V_{OUT}	1.8V	
Output Voltage Ripple	ΔV_{OUT}	0.018V	
Output Current	I_{OUT}	4A	
Output Power	P_{OUT}	7.2W	

Designed–Built–Tested

This document describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to designing a step-down (buck) converter using Maxim's MAX15050 voltage mode controller. The power supply has been built and tested, details of which follow later in this document.

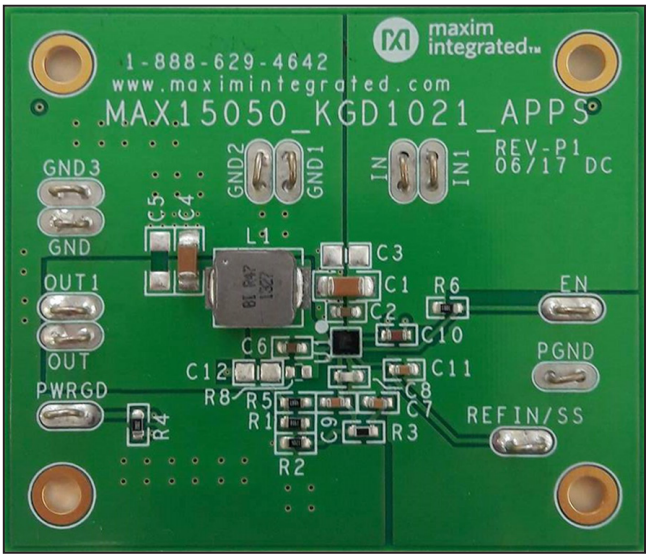

Figure 1. MAXREFDES1021 hardware.

Buck Converter

The buck converter is the most commonly used type of switching regulator. A switching regulator is a circuit that uses a power switch, an inductor, and a diode to transfer energy from the input to the output of the circuit. These components can be rearranged to form various topologies of the switching regulator. Feedback and control circuitry is often nested around these circuits to regulate the energy transfer and maintain a constant output.

The main advantage to using switching regulators instead of linear regulators is that switching regulators are far more efficient. They can reach efficiencies of over 90%, whereas linear regulators have a typical 40% efficiency rating.

As mentioned, there are various types of switching regulators, including the following:

- A buck regulator: where voltage is stepped down from input to output.
- A boost regulator: where voltage is stepped up from input to output.
- A buck-boost regulator: where voltage can be stepped up or down from input to output. These can also come in a variety of forms.

The reference circuit in Figure 2 is a buck converter. The 2.9V to 5.5V input voltage is stepped down to 1.8V at the output. Buck converters are also useful because while stepping down the voltage, they step up the current, allowing for relatively high output currents to be available. This circuit has a maximum output current of 4A.

Buck Converter Operation

The main components of a buck converter are the power switch (which usually comes in the form of a MOSFET), the inductor, and the diode. As the MOSFET is switched on and off, a magnetic field is generated in the inductor. When the switch is on (or closed), current flows into the inductor and through the output. When the switch is off (or open), due to the magnetic field current still flows from the inductor to the output load. This is explained in more detail below.

Transistor Switch "On" Period

When the transistor switch is on, it supplies the output load with current. Initially current flow to the load is restricted as energy is also being stored in the inductor. The current in the load and the charge on the output capacitor therefore build up relatively slowly in comparison with the switch-on time of the MOSFET. During the on period there is a large voltage across the diode that causes it to be reverse-biased.

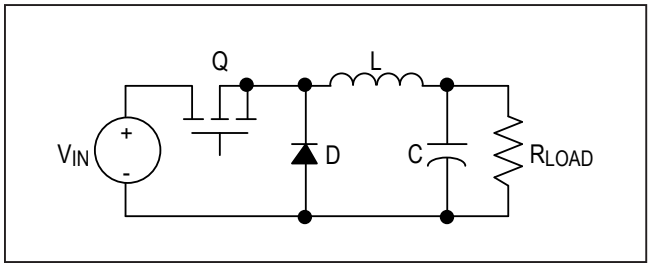

Figure 2. Buck converter topology.

Transistor Switch "Off" Period

When the transistor switch is off, the energy that had been stored in the inductor's magnetic field is released. The voltage across the inductor is now in reverse polarity, and sufficient stored energy is available to maintain current flow while the transistor is open. The reverse polarity of the inductor allows current to flow in the circuit via the load and the diode, which is now forward-biased. Once the inductor has been drained of the majority of its stored energy, the load voltage begins to fall, and the charge stored in the output capacitor then becomes the main source of current. This leads to the ripple waveform shown in Figure 3.

MAX15050 Control Circuitry

The controller logic block is the central processor that determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator and generates the driver signals for both high-side and low-side MOSFETs. The control logic block controls the break-before-make logic and the timing for charging the bootstrap capacitors. The error signal from the voltage-error amplifier is compared with the ramp signal generated by the oscillator at the PWM comparator to produce the required PWM signal. The high-side switch turns on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the V_{COMP} signal or the current-limit threshold is exceeded. The low-side switch then turns on for the remainder of the oscillator cycle.

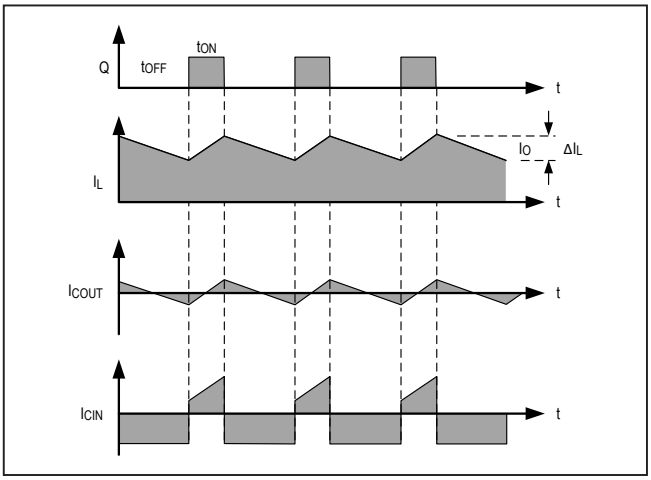

Figure 3. Buck waveforms.

Design Procedure for Step-Down Regulator Using MAX15050

Now that the principle of operation of the buck regulator is understood, a practical design example can be illustrated. The converter design process can be divided into several stages: power stage design and the feedback loop. This document is primarily concerned with the power stage design and the feedback loop, and is intended to complement the information contained in the MAX15050 data sheet.

The following design parameters are used throughout this document:

V_{IN} = Input voltage

V_{OUT} = Output voltage

V_{FB} = Feedback voltage

I_{OUT} = Output current

f_{SW} = Switching frequency

D = Duty cycle

The above symbols are sometimes followed by parentheses to indicate whether minimum or maximum values of the parameters are intended, for example, minimum input voltage is intended by the symbol $V_{IN(MIN)}$. Unless otherwise noted, typical values are intended. Refer to the schematic, available online with the reference design documents.

Switching Frequency

The MAX15050 features a 1MHz fixed switching frequency, allowing the user to achieve all-ceramic capacitor designs and fast transient responses. The high operating frequency minimizes the size of external components.

Step 1: Setting the Output Voltage

The output voltage can be adjusted from 0.6V to (0.9 x V_{IN}) by changing the values of R1 and R2. To determine the value of the resistor-divider, first select R1 between 2kΩ and 10kΩ, then use the following equation to calculate R2:

$$R2 = (V_{FB} \times R1)/V_{OUT} - V_{FB})$$

where V_{FB} is equal to the reference voltage at REFIN/SS and V_{OUT} is the output. If no external reference is applied at REFIN/SS, the internal reference is automatically selected and V_{FB} becomes 0.6V. In this case, R2 is not needed for V_{OUT} = 0.6V. In this circuit, R1 is 8.06kΩ and R2 is 4.02kΩ. This means V_{OUT} = 1.8V.

Step 2: Selecting the Inductor

For the step-down topology, the inductor value is given by:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times V_{IN} \times LIR \times I_{OUT(MAX)}}$$

where LIR is the ratio of the inductor ripple current to full load current at the minimum duty cycle and f_{SW} is the switching frequency (1MHz). Choose LIR between 20% and 40% for best performance and stability. Assuming V_{OUT} = 1.8V, V_{IN} = 2.9V and $I_{OUT(MAX)}$ = 4A, then:

$$L = \frac{1.8V \times (2.9V - 1.8V)}{1MHz \times 2.9V \times 0.4 \times 4A} = 0.43\mu H$$

Step 3: Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage-rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Estimate the output voltage ripple due to the output capacitance, ESR, and ESL as follows:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

and:

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \times ESL$$

or:

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{OFF}} \times ESL$$

whichever is higher, where the peak-to-peak inductor current (I_{P-P}) is:

$$I_{P-P} = \frac{(V_{IN} - V_{OUT})}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Use these equations for initial output-capacitor selection. Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output-voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output-voltage ripple decreases with larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

For this circuit:

$$I_{P-P} = \frac{2.9V - 1.8V}{1MHz \times 0.47\mu H} \times \frac{1.8V}{2.9V} = 1.45A$$

Following the above equations, the recommended minimum output capacitance is 22µF for the MAX15050.

Step 4: Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the device. The total input capacitance must be equal to or greater than the value given by the following equation to keep the input ripple voltage within the specification and minimize the high-frequency ripple current being fed back to the input source:

$$C_{IN(MIN)} = \frac{D \times t_S \times I_{OUT}}{V_{IN-RIPPLE}}$$

where $V_{IN-RIPPLE}$ is the maximum-allowed input ripple voltage across the input capacitors and is recommended to be less than 2% of the minimum input voltage, D is the duty cycle (V_{OUT}/V_{IN}), t_S is the switching period ($1/f_{SW}$) = 1µs, and I_{OUT} is the output load.

The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source, but are instead shunted through the input capacitor. The input capacitor must meet the ripple current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where I_{RIPPLE} is the input ripple RMS current.

Step 5: IN and V_{DD} Decoupling

To decrease the noise effects due to the high switching frequency and maximize the output accuracy of the MAX15050, decouple V_{IN} with a 22µF capacitor in parallel with a 0.1µF capacitor from V_{IN} to GND. Also decouple V_{DD} with a 2.2µF capacitor from V_{DD} to GND. Place these capacitors as close as possible to the device.

Step 6: Compensation Network

The power transfer function consists of one double pole and one zero. The double pole is introduced by the inductor, L1, and the output capacitor, C_{OUT}. The ESR of the output capacitor determines the zero. The double pole and zero frequencies are given as follows:

$$f_{P1\_LC} = f_{P2\_LC} = \frac{1}{2\pi \times \sqrt{L \times C_O \times \left(\frac{R_O + ESR}{R_O + R_L}\right)}}$$

$$f_{Z\_ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

where R_L is equal to the sum of the output inductor's DC resistance (DCR) and the internal switch resistance, $R_{DS(ON)}$. A typical value for $R_{DS(ON)}$ is 25mΩ. R_{OUT} is the output load resistance, which is equal to the rated output voltage divided by the rated output current. ESR is the total equivalent series resistance of the output capacitor. If there is more than one output capacitor of the same type in parallel, the value of the ESR in the above equation is equal to that of the ESR of a single output capacitor divided by the total number of output capacitors.

The MAX15050 high switching frequency allows the use of ceramic output capacitors. Since the ESR of ceramic capacitors is typically very low, the frequency of the associated transfer function zero is higher than the unity-gain crossover frequency, f_C, and the zero cannot be used to compensate for the double pole created by the output inductor and capacitor. The double pole produces a gain drop of 40dB/decade and a phase shift of 180°. The compensation network must compensate for this gain drop and phase shift to achieve a stable high-bandwidth closed-loop system. Therefore, use Type III compensation. Type III compensation possesses three poles and two zeros with the first pole, f_{P1_EA}, located at zero frequency (DC). Locations of other poles and zeros of the Type III compensation are given by:

$$f_{Z1\_EA} = \frac{1}{2\pi \times R1 \times C1}$$

$$f_{Z2\_EA} = \frac{1}{2\pi \times R3 \times C3}$$

$$f_{P2\_EA} = \frac{1}{2\pi \times R2 \times C3}$$

$$f_{P3\_EA} = \frac{1}{2\pi \times R1 \times C2}$$

The above equations are based on the assumptions that C1 >> C2, and R3 >> R2, which are true in most applications. Placements of these poles and zeros are determined by the frequencies of the double pole and ESR zero of the power transfer function. It is also a function of the desired closed-loop bandwidth. The following section outlines the step-by-step design procedure to calculate the required compensation components for the MAX15050. See Figure 4 for reference.

The zero-cross frequency of the closed-loop, f_C, should be between 10% and 20% of the switching frequency, f_{SW} (1MHz). A higher zero-cross frequency results in faster transient response. Once f_C is chosen, C1 is calculated from the following equation:

$$C1 = \frac{1.5625\left(\frac{V_{IN}}{V_{P-P}}\right)}{2 \times \pi \times R3 \times \left(1 + \frac{R_L}{R_O}\right) \times f_C}$$

where $V_{P-P} = 1V_{P-P}$ (typ).

Due to the underdamped nature of the output LC double pole, set the two zero frequencies of the Type III compensation less than the LC double-pole frequency to provide adequate phase boost. Set the two zero frequencies to 80% of the LC double-pole frequency. Hence:

$$R1 = \frac{1}{0.8 \times C1} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

$$C3 = \frac{1}{0.8 \times R3} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

Setting the second compensation pole, f_{P2_EA}, at f_{Z_ESR} yields:

$$R2 = \frac{C_O \times ESR}{C3}$$

Set the third compensation pole at 1/2 the switching frequency (500kHz) to gain phase margin. Calculate C2 as follows:

$$C2 = \frac{1}{\pi \times R1 \times f_S}$$

These equations provide accurate compensation when the zero-cross frequency is significantly higher than the double-pole frequency. When the zero-cross frequency is near the double-pole frequency, the actual zero-cross frequency is higher than the calculated frequency. In this case, lowering the value of R1 reduces the zero-cross frequency. Also, set the third pole of the Type III compensation close to the switching frequency (1MHz) if the zero-cross frequency is above 200kHz to boost the phase margin. The recommended range for R3 is 2kΩ to 10kΩ. Note that the loop compensation remains unchanged if only R4's resistance is altered to set different outputs.

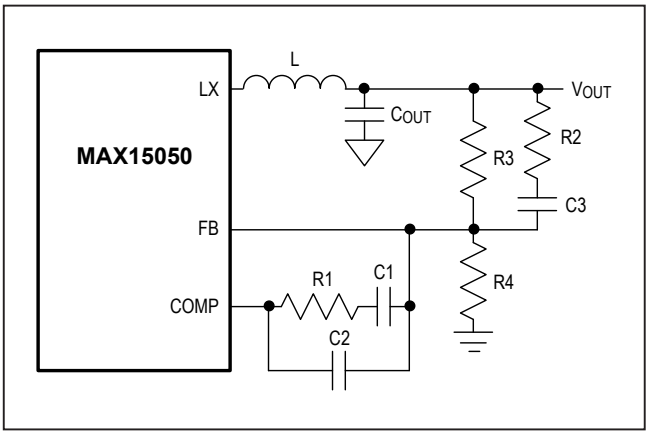

Figure 4. MAX15050 compensation network.

Design Resources

Download the complete set of **Design Resources** including the schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/17	Initial release	—