Boost, Single-Output, -73V to -35V Input, 5V/100mA Output DC-DC Converter Using the MAX668

MAXREFDES1004

Introduction

The MAX668/MAX669 constant-frequency, pulse-width modulating (PWM), current-mode DC-DC controllers are designed for a wide range of DC-DC conversion applications, including step-up, SEPIC, flyback, and isolated-output configurations. Power levels of 20W or more can be controlled with conversion efficiencies of over 90%. The input voltage range of 1.8V to 28V supports a wide range of battery and AC-powered inputs. An advanced BiCMOS design features low operating current (220µA), adjustable operating frequency (100kHz to 500kHz), soft-start, and a SYNC input, allowing the MAX668/MAX669 oscillator to be locked to an external clock.

The MAX669 is optimized for low input voltages with a guaranteed start-up voltage of 1.8V. It requires bootstrapped operation (IC-powered from boosted output) and supports output voltages of up to 28V. The MAX668 operates with inputs as low as 3V and can be connected in either a bootstrapped or non-bootstrapped (IC-powered from input supply or other source) configuration. When not bootstrapped, it has no restriction on output voltage. Both ICs are available in an extremely compact 10-pin µMAX® package.

Benefits and features:

- 1.8V Minimum Start-Up Voltage (MAX669)
- Wide Input Voltage Range (1.8V to 28V)
- Tiny 10-Pin µMAX Package
- Current-Mode PWM and Idle Mode Operation
- Adjustable 100kHz to 500kHz Oscillator or SYNC Input
- 220µA Quiescent Current
- Logic-Level Shutdown
- Soft-Start

Hardware Specification

A negative input, positive output DC-DC converter using the MAX668 is demonstrated for a 5V DC output application. The power supply delivers up to 100mA at 5V. An overview of the design specification is shown in Table 1 below.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	-73V	-35V
Switching Frequency	f_{SW}	125kHz	
Peak Efficiency	η	70%	
Output Voltage	V_{OUT}	4.9V	5.1V
Output Voltage Ripple	ΔV_{OUT}	20mV	
Output Current	I_{OUT}	0A	100mA
Output Power	P_{OUT}	0.5W	

Designed–Built–Tested

This reference design describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to design a negative input, positive output boost converter using Maxim's MAX668 current mode controller. The power supply has been built and tested, details of which follow later in this document.

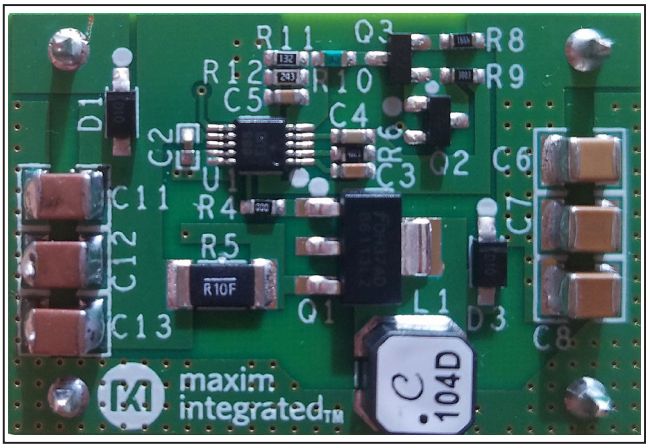

Figure 1. MAXREFDES1004 hardware.

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Boost Converter

A boost converter (step-up converter) is a DC-DC power converter that steps up voltage (while stepping down current) from its input to its output. The key principle that drives the boost converter is the tendency of an inductor to resist changes in current by creating and destroying a magnetic field. In a boost converter, the output voltage is always higher than the input voltage. A schematic of a boost power stage is shown in Figure 2.

Figure 3 shows that when the switch is on, current flows through the inductor in a clockwise direction and the inductor stores some energy by generating a magnetic field. The polarity of the left side of the inductor is positive. During this period, the diode D1 is reverse bias, so there's no current flow through the diode.

Figure 4 shows that when the switch is off, current is reduced as the impedance is higher. The magnetic field previously created is destroyed to maintain the current toward the load. Thus, the polarity is reversed (meaning the left side of the inductor is negative). As a result, two sources are in series, causing a higher voltage to charge the capacitor through the diode D1.

In a steady-state operating condition, the average voltage across the inductor over the entire switching cycle is zero. This implies that the average current through the inductor is also in a steady state. This is an important rule governing all inductor-based switching topologies. Taking this one step further, we can establish that for a given charge time, t_{ON}, and a given input voltage and with the circuit in equilibrium, there is a specific discharge time, t_{OFF}, for an output voltage. Because the average inductor voltage in steady state must equal zero, we can calculate for the boost circuit as follows:

$$V_{IN} \times t_{ON} = t_{OFF} \times V_L$$

And because:

$$V_{OUT} = V_{IN} + V_L$$

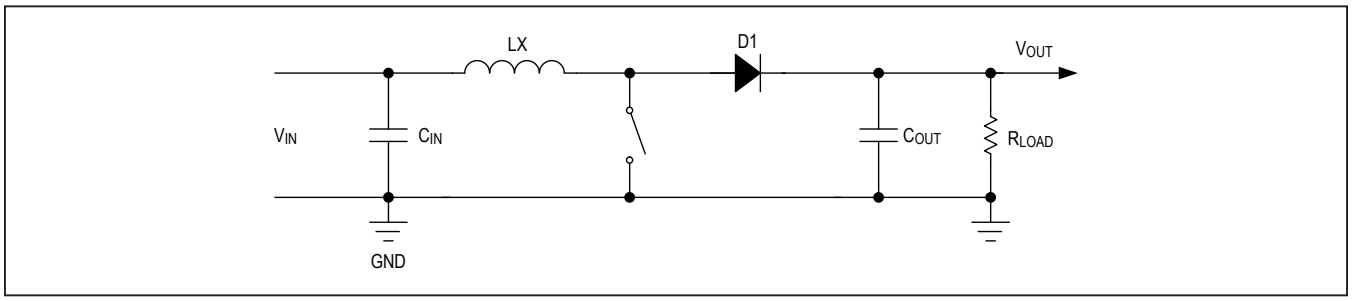

Figure 2. Boost converter topology.

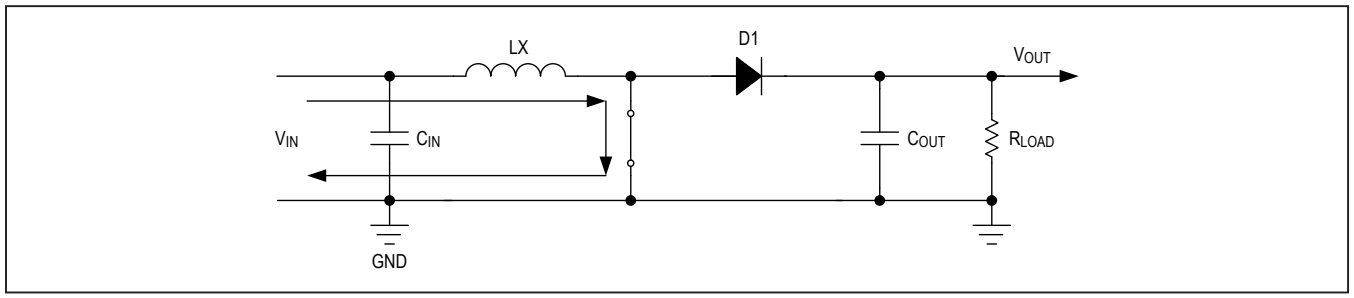

Figure 3. Switch on-period equivalent circuit.

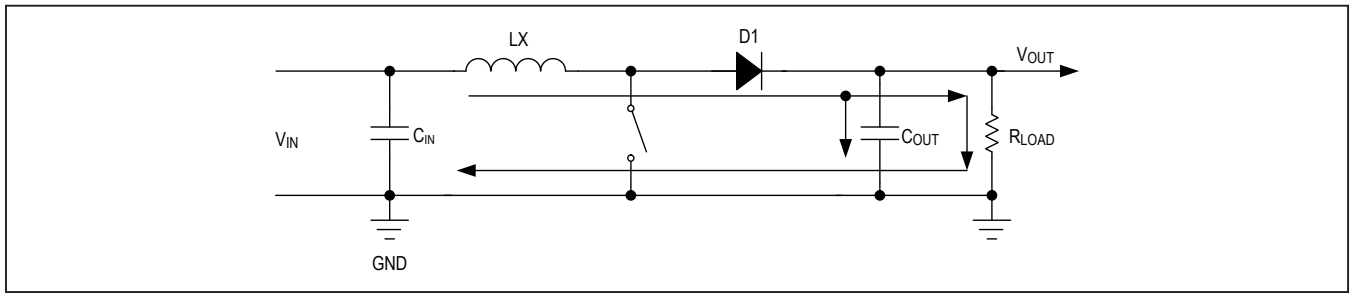

Figure 4. Switch off-period equivalent circuit.

we can then establish the following relationship:

$$V_{OUT} = V_{IN} \times \left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

Using the relationship for duty cycle (D):

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

Then for the boost circuit:

$$V_{OUT} = \frac{V_{IN}}{1 - D}$$

Design Procedure

Now that the principle of operation of the boost is understood, a practical design example can be illustrated. The converter design process can be divided into several stages: negative input, positive output boost design, power stage design, and setup of the MAX668 boost current mode controller. This document is primarily concerned with the negative input stage. Positive output boost design, the power stage design, and the other circuit is intended to complement the information contained in the MAX668 data sheet with details on how to set up the protection functions of the controller.

The following design parameters are used throughout:

V_{IN} = Input Voltage

V_O = Output Voltage

I_O = Output Current

f_{OSC} = Switching Frequency

I_{PEAK} = Peak Inductor Current

I_{LDC} = Average DC Input Current

The above symbols are sometimes followed by parentheses to indicate whether minimum or maximum values of the parameters are intended, for example: minimum input voltage is intended by the symbol $V_{IN(MIN)}$. Otherwise typical values are intended. In addition, through the design procedure, reference is made to the schematic in another document.

Step 1: Negative Input, Positive Output Boost Design

Figure 5 is a schematic of the negative input, positive output boost converter. Because the input voltage range is -73V to -35V, which is negative, and its absolute value is much higher than the input voltage range of the MAX668, it's necessary to connect the negative input voltage to the ground of MAX668 and use a resistor (R1), a capacitor (C1), and a 6.2V Zener diode to supply the MAX668.

Two PNP transistors level shift a feedback signal from the 5V output to the IC's FB input. The two PNP transistors Q1 and Q2 are always on, so V2 is approximately 0.5V lower than the ground while V1 is 0.5V higher than V2. That is, the voltage of V1 is the same as the ground voltage. So, the voltage on R3 is the output voltage that we want. As long as the current flow through R3 doesn't change, the output voltage would be a steady voltage that we can set. The feedback input voltage V_{FB} of the MAX668 is 1.25V, so the current that flows through R5 is V_{FB}/R5. As the emitter current and collector current of Q1 are equal, we can conclude that V_{OUT}/R3 = V_{FB}/R5. This equation could be used to set the output voltage. For example, assume the output voltage is 5V, R5 = 1.25kΩ, and V_{FB} = 1.25V, then R3 = 5kΩ.

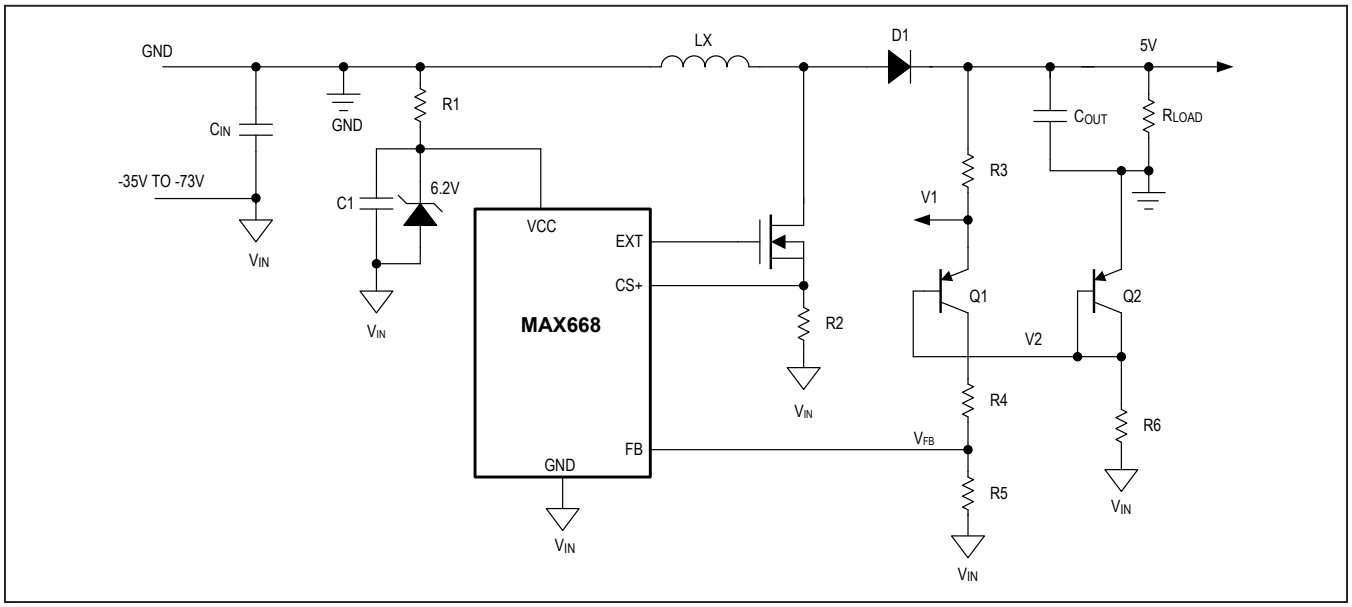

Figure 5. Negative input, positive output boost block diagram.

Step 2: Set the Switching Frequency

The oscillator frequency is set by a resistor, R_{OSC}, connected from FREQ to GND. R_{OSC} must be connected, whether or not the part is externally synchronized R_{OSC} is in each case:

$$R_{OSC} = \frac{5 \times 10^{10}}{f_{OSC}}$$

The 125kHz operating frequency, for example, is set with R_{OSC} = 400kΩ.

Step 3: "Digital" Soft-Start

The MAX668/MAX669 feature a "digital" soft start, which is preset and requires no external capacitor. Upon start-up, in five steps over 1024 cycles of f_{OSC} or f_{SYNC}, the peak inductor increments from 1/5 of the value set by R_{CS} to the full current-limit value. For example, with an f_{OSC} of 200kHz, the complete soft-start sequence takes 5ms.

Step 4: Determining Inductance Value

For most MAX668/MAX669 boost designs, the inductor value (L_{IDEAL}) can be derived from the following equation, which picks the optimum value for stability based on the MAX668/MAX669's internally set slope compensation:

$$L_{IDEAL} = \frac{V_{OUT}}{4 \times I_{OUT} \times f_{OSC}} = \frac{5}{4 \times 0.1 \times 125 \times 10^3} = 100uH$$

The MAX668/MAX669 allow significant latitude in inductor selection if L_{IDEAL} is not a convenient value. This might happen if L_{IDEAL} is a not a standard inductance (such as 10µH, 22µH, etc.) or if L_{IDEAL} is too large to be obtained with suitable resistance and saturation-current rating in the desired size. Inductance values smaller than L_{IDEAL} can be used with no adverse stability effects; however, the peak-to-peak inductor current (I_{LPP}) rises as L is reduced. This has the effect of raising the required I_{LPK} for a given output power and requiring larger output capacitance to maintain a given output ripple. An inductance value larger than L_{IDEAL} can also be used, but output-filter capacitance must be increased by the same proportion that L has to L_{IDEAL}. See the *Step 9: Output Capacitor Selection* section for more information on determining output filter values. Due to the MAX668/MAX669's high switching frequencies, inductors with a ferrite core or equivalent are recommended. Powdered iron cores are not recommended due to their high losses at frequencies over 50kHz.

Step 5: Determining Peak Inductor Current

The peak inductor current required for a particular output is:

$$I_{PEAK} = I_{LDC} + \frac{I_{LLP}}{2} = 0.117 + \frac{0.377}{2} = 0.3055A$$

where I_{LDC} is the average DC input current and I_{LPP} is the inductor peak-to-peak ripple current. The I_{LDC} and I_{LPP} terms are determined as follows:

$$I_{LDC} = \frac{I_O \times (V_{OUT} + V_D)}{V_{IN} - V_{SW}} = \frac{0.1 \times (40 + 0.5)}{35 - 0.3} = 0.117A$$

where V_D is the forward voltage drop across the Schottky rectifier diode (D1), and V_{SW} is the drop across the external FET, when on.

$$I_{LPP} = \frac{(V_{IN} - V_{SW})(V_{OUT} + V_D - V_{IN})}{L \times f_{OSC} \times (V_{OUT} + V_D)} = \frac{(35 - 0.3)(40 + 0.5 - 35)}{100 \times 10^{-6} \times 125 \times 10^3 \times (40 + 0.5)} = 0.377A$$

Once the peak inductor current is selected, the current-sense resistor (R_{CS}) is determined by:

$$R_{CS} = \frac{85mV}{I_{PEAK}} = \frac{85mV}{0.3055} = 0.278\Omega$$

Step 6: Power MOSFET Selection

The MAX668/MAX669 drive a wide variety of N-channel power MOSFETs (NFETs). Because LDO limits the EXT output gate drive to no more than 5V, a logic-level NFET is required. Best performance, especially at low input voltages (below 5V), is achieved with low-threshold NFETs that specify on-resistance with a gate-source voltage (V_{GS}) of 2.7V or less. When selecting an NFET, key parameters can include:

- Total gate charge (Q_g)
- Reverse transfer capacitance or charge (C_{RSS})
- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Minimum threshold voltage ($V_{TH(MIN)}$)

At high switching rates, dynamic characteristics (parameter 1 and parameter 2 above) that predict switching losses might have more impact on efficiency than $R_{DS(ON)}$, which predicts DC losses. Q_g includes all capacitances associated with charging the gate. In addition, this parameter helps predict the current needed to drive the gate at the selected operating frequency. The continuous LDO current for the FET gate is:

$$I_{GATE} = Q_g \times f_{OSC}$$

For example, the MMFT3055L has a typical Q_g of 7nC (at V_{GS} = 5V); therefore, the I_{GATE} current at 500kHz is 3.5mA. Use the FET manufacturer's typical value for Q_g in the above equation, since a maximum value (if supplied) is usually too conservative to be of use in estimating I_{GATE}.

Step 7: Diode Selection

The MAX668/MAX669's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. Ensure that the diode's average current rating is adequate using the diode manufacturer's data, or approximate it with the following formula:

$$I_{DIODE} = I_{OUT} + \frac{I_{PEAK} - I_{OUT}}{3} =$$

$$0.1 + \frac{0.3055 - 0.1}{3} = 0.1685A$$

Also, the diode reverse breakdown voltage must exceed V_{OUT}. For high output voltages (50V or above), Schottky diodes might not be practical because of this voltage requirement. In these cases, use a high-speed silicon rectifier with adequate reverse voltage.

Step 9: Output Capacitor Selection

The minimum output filter capacitance that ensures stability is determined using the following formula:

$$C_{OUTMIN} = \frac{7.5 \times \frac{L}{L_{IDEAL}}}{2\pi \times R_{CS} \times f_{OSC} \times V_{INMIN}} =$$

$$\frac{7.5 \times 1}{6.28 \times 0.278 \times 125 \times 10^3 \times 35} = 0.98\mu F$$

where $V_{IN(MIN)}$ is the minimum expected input voltage. Typically $C_{OUT(MIN)}$, though sufficient for stability, is not adequate for low output voltage ripple. Because output ripple in boost DC-DC designs is dominated by capacitor equivalent series resistance (ESR), a capacitance value 2 or 3 times larger than $C_{OUT(MIN)}$ is typically needed. Low-ESR types must be used. Output ripple due to ESR is:

$$V_{RIPPLE(ESR)} = I_{PEAK} \times ESR_{COUT}$$

Step 10: Input Capacitor Selection

The input capacitor (C_{IN}) in boost designs reduces the current peaks drawn from the input supply and reduces noise injection. The value of C_{IN} is largely determined by the source impedance of the input supply. High source impedance requires high input capacitance, particularly as the input voltage falls. Because step-up DC-DC converters act as "constant-power" loads to their input supply, input current rises as input voltage falls. Consequently, in low-input-voltage designs, increasing C_{IN} and/or lowering its ESR can add as many as 5 percentage points to conversion efficiency. A good starting point is to use the same capacitance value for C_{IN} as for C_{OUT}.

Trademarks

Design Resources

For the complete set of design resources, including schematics, bill of materials, and PCB layout, go to **www.maximintegrated.com/AN6700** and click on the **Design Resources** tab.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—