Real-World Charged Board Model (CBM) Failures

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Abstract – ICs that are robust to ESD at the component-level may be damaged by ESD at the board-level. Two case studies show that real-world Charged Board Model (CBM) ESD damage is typically more severe than HBM or CDM damage. Consequently, CBM damage can be easily mistaken for EOS damage. A high-capacitance yet compact PCB evaluation board facilitates qualitative CBM testing using conventional CDM test systems. Based on the case studies and CBM test results, guidelines are provided on how to minimize the likelihood of real-world CBM failures.

I. Introduction

The ESDA & JEDEC Human Body Model (HBM) is a mature, well-understood ESD model for simulating charge transfer from a person's finger to an electronic component. However, consistent with industry findings [1-3], in Analog Devices, Inc.'s experience, the HBM rarely simulates real-world ESD failures for one or more of the following primary reasons:

- Most component manufacturers and users have effective controls against HBM ESD events.
- The latest-generation package styles such as mBGAs, LGAs, SOTs, SC70s, & CSPs with mm-range dimensions are often effectively too small for people to handle with fingers.
- Most high-volume component and board manufacturing uses automated equipment; humans rarely actually touch components (even relatively large ones) during such manufacturing.
- Any real-world HBM ESD events typically have much faster rise times and lower overall energy than the events simulated by the ESDA & JEDEC HBM models [4].

A review of ADI's Failure Analysis (FA) database on internal and customer IC rejects shows that the vast majority of real-world ESD failures can be simulated by Charged Device Model (CDM), Charged Strip Model (CSM), or Charged Board Model (CBM) testing [5,6]. The CSM test method simulates failures of ICs assembled and tested in matrix (or strip) form. For customer returns where the ESD damage cannot be simulated via HBM, CDM, or CSM testing, a CBM test method was developed to successfully replicate the damage observed on real-world failures.

The CSM work previously referenced showed that ICs immune to CDM damage at the singulated package-level may be highly susceptible to CSM damage at the strip-level since strip capacitance may be far greater than package capacitance. Similarly, others have shown that ICs robust to HBM & CDM damage at the package-level may be susceptible to CBM damage at the board-level depending on the Printed Circuit Board (PCB) design / board capacitance [1, 7-11]. This is a critical finding since IC users sometimes erroneously believe that PCBs are inherently robust to ESD if all the individual components on the PCB have high HBM & CDM ESD withstand voltages.

This paper provides two case study examples of ICs that are robust to ESD at the component-level but were nonetheless damaged by ESD at the board-level. The damage was simulated via Field-Induced Charged Board Model (FICBM) testing using a conventional CDM test system. For a given charge voltage, the CBM discharge waveforms had much higher peak currents than the corresponding CDM discharge waveforms. Thus, the CBM damage was more severe than the CDM damage. In some cases, the CBM damage was so severe that it could easily be mistaken for EOS damage. The susceptibility of a given IC to CBM damage is a complex function of variables including the IC on-chip protection network; the IC package design; the size of the power planes on the PCB; and the number of power supply pins on the IC tied to the power planes.

II. Objectives of this Work

This work documents for the first time the physical failure analysis results of real-world CBM ESD failures, along with the simulation results from a CBM test method that was successfully used to replicate these failures. This work thus helps semiconductor, Electronic Manufacturing Services (EMS), and Original Equipment Manufacturer (OEM) companies recognize CBM ESD damage that could otherwise be incorrectly attributed to EOS or other damage. Using two unrelated case studies, this work:

- Details the damage seen on real-world CBM failures;
- Describes a board-level CBM test method used to replicate the damage seen on real-world failures;
- Discusses the corrective actions to eliminate these CBM failures;
- Explores the relationship between the PCB design and the corresponding IC CBM robustness;
- Provides guidelines on how to minimize the likelihood of real-world CBM damage.

III. Real-World ESD Failures

A. Case Study 1 (Dual Op Amp IC)

1. Overview

During board-level testing, a customer experienced a high failure rate (6.7%) on a double-level-metal submicron CMOS Dual Operational Amplifier packaged in an 8-lead SOIC package. The failure mode was consistently a resistive short (typically <100Ω) between pins 2 (-IN A) and 4 (V- / substrate) that rendered the Side A Op Amp non-functional. Interestingly, although each PCB used five of these same Dual Op Amp ICs, the failing units were always from the same board location (Position #5). Given the high failure rate, this board dependency ruled-out the possibility that the failing Dual Op Amps were defective as received by the customer. A thorough review of the customer's application circuit showed no reason that the Absolute Maximum Ratings of the Position #5 Dual Op Amp would ever be exceeded.

2. Failure Analysis Results

FA of the Dual Op Amp board failures consistently revealed emission sites at the anode of the input EOS/ESD protection diode between pins 2 and 4. Subsequent de-processing showed that these emission sites were due to silicon damage and melted / reflowed AlCu that shorted this protection diode (see Figure 1).

Neither Human Body Model (HBM) nor Field-Induced Charged Device Model (FICDM) testing was able to replicate the relatively severe damage seen on the customer board failures. At the component-level, this Dual Op Amp in an 8-lead SOIC is robust to ESD events, passing at least 2000V HBM and 1000V FICDM testing to ESDA standards. Testing at 3000V HBM or 1500V FICDM caused the bias current at the input pins to exceed the 50 pA maximum specification, but the Dual Op Amp samples remained fully functional. Not surprisingly, the damage at the EOS/ESD protection diodes on the high-voltage HBM & FICDM samples was much more subtle than that shown in Figure 1; i.e., the AlCu did not melt / reflow.

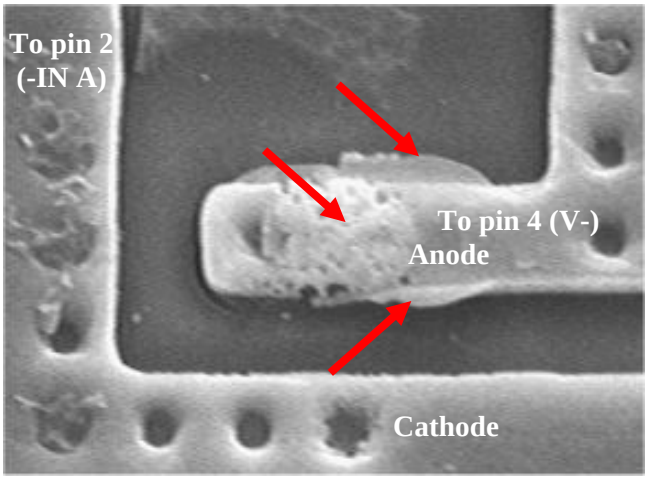


Figure 1: Scanning Electron Microscope (SEM) image of the melted / reflowed AlCu (see arrows) at the anode of the input protection diode on a customer Dual Op Amp board failure. Note: The sample was deprocessed to the METAL1 layer.

3. Evaluation Board CBM Simulation

The well-defined CDM simulates a charged component discharging just before it comes in contact with a conductive object that is at or near ground potential. Detailed test methods [12,13] exist for conducting CDM testing using commercially available systems. These test methods and systems were developed in terms of individual components. In an attempt to duplicate the damage shown in Figure 1, a Field-Induced Charged Board Model (FICBM) test environment was developed and implemented in a manner similar to a method described by Lin [14]. The CBM simulates a charged PCB discharging just before contact is made with a conductive object that is at or near ground potential.

For the present work, a KeyTek Verifier Robotic CDM test system was used for FICBM testing of PCBs. This test system has a 127 mm (5") diameter field charging plate covered by a thin (~13 μm) Mylar tape dielectric layer. This system conforms to ESD Association Standard Test Method STM5.3.1-1999 [12] and produces discharge waveforms that pass waveform verification testing with both 4 pF and 30 pF verification modules. For PCBs, the STM5.3.1-1999 7:1 ratio requirement for charging plate area to component (a PCB in this case) area was not met, but this was an inherent limitation of the existing commercial systems that are targeted for testing small, single components.

Since the PCB that experienced high failure rates of the Dual Op Amp at Board Position #5 was expensive and proprietary, this PCB was not available for FICBM testing. Therefore, a compact, high-capacitance Evaluation Board (EB) was used for CBM test purposes. This EB consisted of a decapsulated Dual Op Amp (i.e., the die was exposed) in a 150 mil, 8-lead SOIC package soldered at the center of a small (3" long x 3" wide x 60 mil thick) two-layer FR4 board. The bottom layer consisted of a 1.4 mil thick copper V- / ground power plane that covered the entire EB, while the top layer consisted of a 1.4 mil thick copper V+ power plane that covered the surface of the EB except for the eight test pads that were connected to the SOIC package pads via 24 mil wide copper traces. The V- and V+ pins on the Dual Op Amp were connected to the ground and V+ power planes, respectively, while the remaining pins were connected to traces / test pads that were floating. No other components were soldered to the EB.

The FICBM test method for each EB was as follows:

1. The EB was centered on the charging plate (see Figure 2). In this configuration, the EB capacitance measured between the ground plane and the field charging plate was ~1.6 nF.
2. The charging plate was raised to +125V and then the pin 2 (-IN A) PCB test pad (see Figure 2) was discharged. Consistent with the methodology in ESDA STM5.3.1-1999, this was repeated two more times.
3. The I-V characteristics between pads 2 (-IN A) and 4 (V-) were checked for degradation.
4. The charging plate was brought to –125V and then test pad 2 was discharged. This was repeated two more times.
5. The I-V characteristics between pads 2 and 4 were again checked for degradation.
6. Consistent with the procedure in Steps 2-5, pad 2 on the same EB was subjected to FICBM testing in 125V charge voltage increments until degradation was observed in the I-V characteristics between pads 2 and 4.

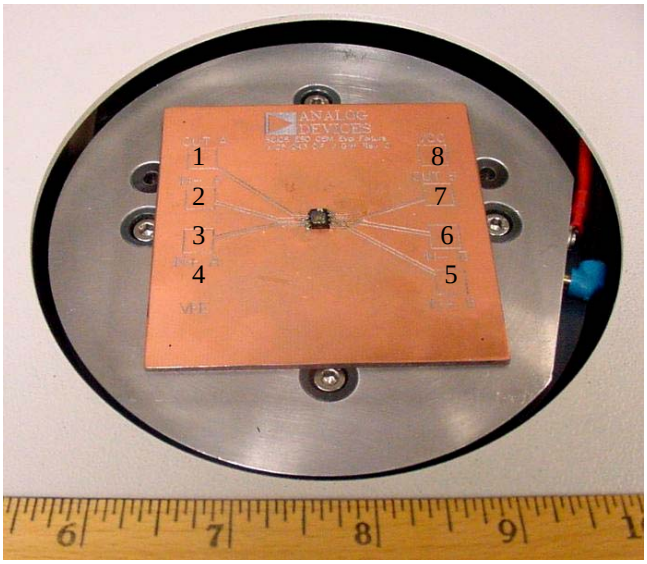


Figure 2: FICBM test method setup for the Evaluation Board with the decapsulated Dual Op Amp and eight labeled test pads.

4. Evaluation Board CBM Simulation Results

For three samples that were FICBM tested as per the previous section (III.A.3), no degradation occurred to the Dual Op Amps after ±250V stressing but leakage was detected between pads 2 (-IN A) and 4 (V-) after -375V stressing. On three new samples that were FICBM tested at ±500V, a resistive short of <100Ω occurred between pads 2 and 4 after -500V stressing. FA of the -500V FICBM failures consistently revealed emission sites at the anode of the input EOS/ESD protection diode between pins 2 and 4. Subsequent de-processing revealed silicon damage and melted / reflowed AlCu at this protection diode (see Figure 3). Thus, FICBM testing at -500V successfully replicated the failure mode and failure mechanism observed on the real-world board failures (reference Figure 1). CBM stressing of fresh samples at higher voltages resulted in severe damage that could easily be mistaken for EOS damage. Figure 4 shows the catastrophic damage at the input EOS/ESD protection diode after -625V FICBM stressing. For negative charge voltage magnitudes of 625V and above, the AlCu anode interconnect was completely fused open.

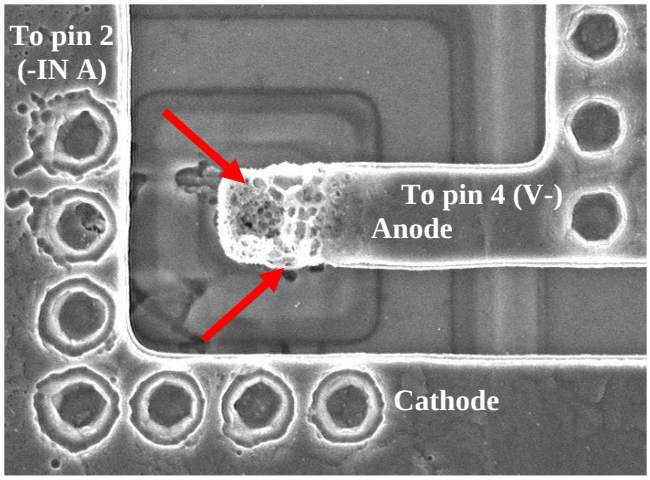


Figure 3: SEM image of the melted / reflowed AlCu (see arrows) at the anode of the input protection diode on a Dual Op Amp that was stressed on an Evaluation Board at -500V FICBM. Note: The sample was deprocessed to the METAL1 layer.

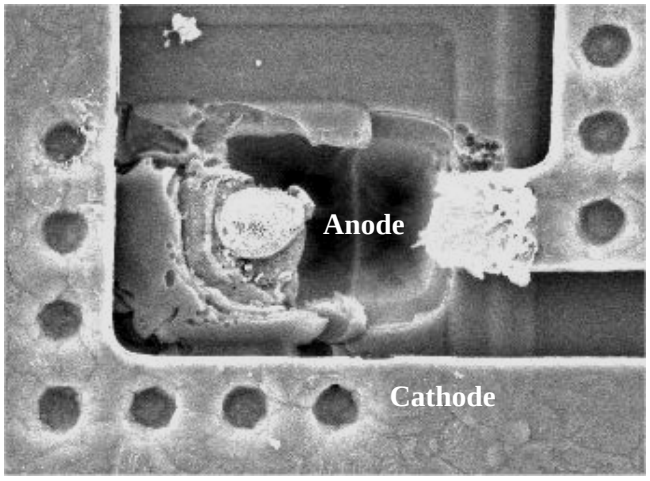


Figure 4: SEM image of the catastrophic damage (fused open AlCu and melted Si) at the same site as shown in Figures 1 and 3. This sample was stressed on an Evaluation Board at -625V FICBM. Note: The sample was deprocessed to the METAL1 layer.

5. Effect of Smaller PCB Power Planes

To investigate the effect of the area of PCB power planes on CBM simulation results, the 3" x 3" Dual Op Amp Evaluation Board shown in Figure 2 was physically cut-down to 1.5" x 3". As expected, this reduced the EB capacitance measured between the ground plane and the field charging plate to ~0.8 nF, or half the value measured before the ground plane area was reduced by 50%.

For three samples that were FICBM tested as per Section III.A.3 using the half-size EB, the Dual Op Amps showed no degradation after ±375V stressing, leakage after -500V stressing, and a resistive short of <100Ω between test pads 2 and 4 after -625V stressing. FA of these CBM failures once again revealed silicon damage and melted / reflowed AlCu at the anode of the EOS/ESD protection diode between pins 2 (-IN A) and 4 (V-).

6. Elimination of Real-World Failures

Investigation of the customer's board assembly process showed that a plastic CPU socket immediately adjacent to Dual Op Amp Position #5 (the failing position) was charged to as high as 1400V prior to infrared (IR) solder reflow. This induced a relatively large charge on adjacent board components, including the Dual Op Amp. Subsequent IR reflow caused these components to discharge, resulting in the CBM damage shown in Figure 1. As corrective action, the customer added an ionizer to their production line between the automatic component insertion and IR reflow process steps to safely dissipate charges on the PCB. No ESD-related Dual Op Amp failures have occurred subsequently, thus proving the effectiveness of this corrective action.

7. Discussion of Results

Figure 5 shows a comparison of the 375V discharge waveforms at pin 2 on a stand-alone Dual Op Amp (i.e., a FICDM discharge) versus test pad 2 when the Dual Op Amp was on the full-size Evaluation Board (i.e., a FICBM discharge). For a given charge voltage, the peak current during a CBM discharge was much higher than a CDM discharge. Also, the FICBM discharge waveform in Figure 5 has a faster rise time than the device (FICDM) discharge waveform due to the lower inductance and resistance of the board discharge path.

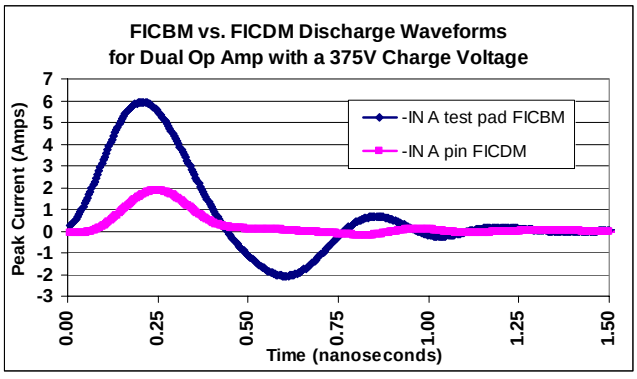


Figure 5: Comparison of FICBM vs. FICDM discharge waveforms at Dual Op Amp pad / pin 2 showing the higher energy in the CBM event for the Evaluation Board shown in Figure 2.

This difference in the discharge waveform peak currents is due primarily to the larger effective capacitances at the board-level in comparison to the

device-level. Figure 6 and Table 1 show the schematic and corresponding details of the DUT (C_x) and board (C_{BDx}) capacitances for the Dual Op Amps.

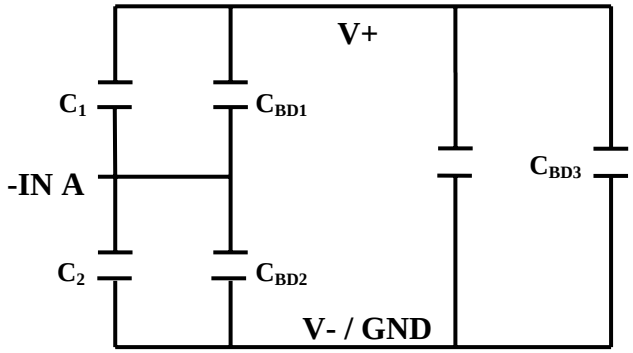


Figure 6: Schematic of the FICDM (C_x) and FICBM (C_{BDx}) capacitive elements contributing to the waveforms in Figure 5.

Table 1: Description and measured values for the capacitive elements shown in the Figure 6 schematic

Label	Description	Value
C_1	DUT diode to V+ capacitance	1.3 pF
C_{BD1}	-IN A pad & trace to V+ cap.	17 pF
C_2	DUT diode to V- capacitance	1.3 pF
C_{BD2}	-IN A pad & trace to V- cap.	9.9 pF
C_3	DUT V+ to V- capacitance	43 pF
C_{BD3}	Eval. Board V+ to V- cap.	164 pF

During CBM testing, the capacitance, C_{BD3}, between the V- / ground and V+ power planes (excluding the DUT) also contributes to the discharge current. C_{BD3} measured 164 pF on the full-size EB and 82 pF on the half-size EB. For a negative CBM charge voltage (which induces positive charge on the V- plane), the V+ plane has negative charge and thus the discharge of C_3 and C_{BD3} occurs through both EOS/ESD protection diodes on pin 2 in forward bias. The peak currents during CDM (pin 2) and CBM (pad 2) discharges reflect the capacitive contributions from C_3 and (C_3 + C_{BD3}), respectively.

When the charging plate was negative during FICBM testing and then the –IN A test pad on the EB was discharged (i.e., grounded), the positive charge stored on the ground plane produced a current spike that was almost instantaneously funneled through the single forward-biased –IN A EOS/ESD protection diode. (Note: The anode of this diode is tied directly to –V / ground and the cathode is tied directly to –IN A.) As expected, larger ground planes store more charge and thus the Dual Op Amp CBM ESD withstand voltage for the full-size EB (±250V) was less than that for the half-size EB (±375V). Because PCBs typically have large power planes, real-world peak CBM currents can be far higher than real-world peak HBM or CDM currents. Consequently, the diode between V- / ground and –IN A was severely damaged by real-world (Figure 1) and simulation (Figures 3 & 4) CBM discharges, while it was robust to component-level HBM and CDM events.

B. Case Study 2 (DSP IC)

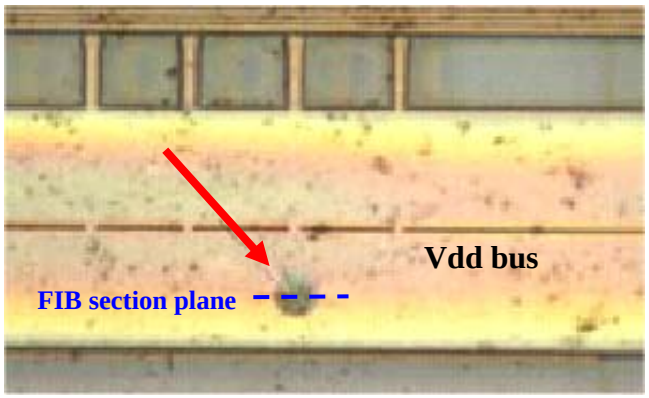
1. Overview

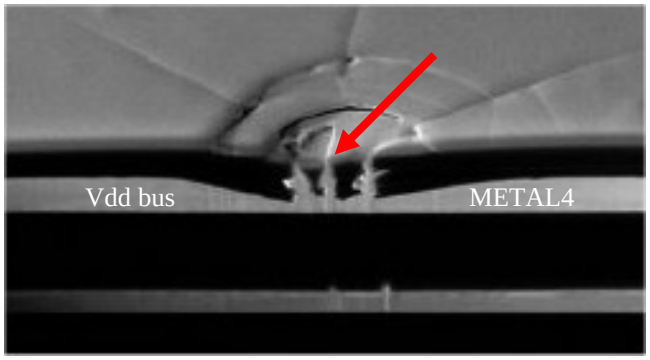
During system-level production testing and field application, a customer had a several hundred PPM failure rate on a four-level-metal, deep-submicron CMOS DSP packaged in a 28 mm x 28 mm, 208-lead Plastic Quad Flat Pack (MQFP). The failure modes varied, but typically involved functional failures within a small block of circuitry within the DSP.

The DSP was located near a corner of the PCB above relatively large copper ground planes in both the top and bottom layers of the PCB. All the components were on one side of the customer's four-layer PCB. The top and bottom ground planes were interconnected by numerous plated through-holes. The 35 GND pins on the DSP package were tied to the interconnected copper ground planes, while the 33 Vdd pins were tied to an internal copper Vdd power plane. The other internal PCB layer was used for routing I/O signals.

2. Failure Analysis Results

FA of samples of the DSP board failures revealed damage at Vdd buses in the form of ~10 μm diameter circular areas of melted / reflowed AlCu with cracked / ruptured overlying passivation (Figures 7a & 7b). Banerjee *et al.* [15] have attributed damage similar to that in Figures 7a & 7b to extreme current densities (typically ~5 x 10^7 A/cm^2 for AlCu METAL4) during short pulses (~100 ns) such as ESD that heat AlCu to ~1000°C, well above its melting point. At this temperature, the thermo-mechanical stress exceeds the fracture strength of the overlying oxide-nitride passivation layer, causing it to rupture. As shown in Figure 7b, the passivation ruptured in a spider-web-like pattern, and parts of the passivation "caved-in" as the AlCu metal melted and reflowed as vertical "fingers." However, the damage shown in Figures 7a & 7b did not result in the observed electrical failure modes since the Vdd buses were not fused open.





Figures 7a & 7b: Optical (upper photo) and corresponding Focused Ion Beam (FIB) cross-section image (lower photo) of the melted / reflowed METAL4 AlCu "fingers" (see arrow) and overlying cracked glassivation on a customer DSP board failure.

Further FA of the DSPs that failed in customer PCBs showed that the functional failures were due to CMOS transistor "stuck at" faults caused by excessive trapped negative charges in the gate oxide of one or more CMOS transistors. This was validated by using a Focused Ion Beam (FIB) to scan the gate oxide of stuck transistors with gallium ions (Ga^{+}). These positive ions neutralized the negative trapped charges, resulting in full recovery of the failing transistors. The charge trap sites were generated when the ~12V tunneling voltage of the gate oxides of these transistors was exceeded. This occurred when the product of the Vdd interconnect resistance for these transistors ($R_{INTERCONNECT}$) and the high current ESD transients (I_{PEAK}) in these Vdd interconnects was >12V. Depending on the density of the trap sites generated in the gate oxide and their fill rate during subsequent PCB operation, the DSP time-to-failure ranged from days to months after the ESD events.

Neither HBM nor CDM testing could replicate the relatively severe damage seen on the customer board failures. At the component level, the Vdd pins on this DSP in a 208-lead MQFP are extremely robust to ESD events, passing at least 7000V HBM and 2500V FICDM testing. (Note: Testing was not conducted above these high voltage levels.) Decapsulation of samples subjected to these extreme device-level ESD events showed no visible damage.

3. Production Board CBM Simulation

As in Case Study 1, FICBM testing was conducted using a KeyTek Verifier Robotic CDM test system. To assist simulating the failures shown in Figures 7a & 7b, the customer provided numerous PCBs. Since the complete customer PCB was larger than the 127 mm (5") field charging plate, the PCBs were cut-down in size. However, the ground plane under the DSP was kept fully intact. (Note: More complete details on the customer's PCB design are not provided since this information is proprietary.) Since full electrical testing of the cut-down PCBs was not feasible, the DSP on each PCB was decapsulated to expose the die for visual inspection purposes. Initial high-magnification die inspection of the DSPs on the PCBs revealed no anomalies like those shown in Figure 7a.

The FICBM test method for each customer PCB was as follows:

1. The cut-down PCB was centered on the charging plate (see Figure 8). Fortunately, the PCB had no components on the bottom side, so it rested flat on the charging plate. In this configuration, the capacitance measured between the PCB ground planes and the charging plate was ~420 pF, while the capacitance between the PCB Vdd plane and the charging plate was ~460 pF.
2. The charging plate was raised to +125V and then the ground plane was discharged at a test pad close to the edge of the PCB. Consistent with the methodology in ESDA STM5.3.1-1999, this was repeated two more times.
3. High magnification optical die inspection was conducted to look for the onset of damage.
4. The charging plate was brought to –125V and then the ground plane was discharged at the same PCB location. This was repeated two more times.
5. High magnification die inspection was again conducted to look for the onset of damage.
6. Consistent with the procedure in Steps 2-5, the ground plane on the same PCB was subjected to FICBM testing in 125V charge voltage increments until high-magnification optical inspection revealed damage.

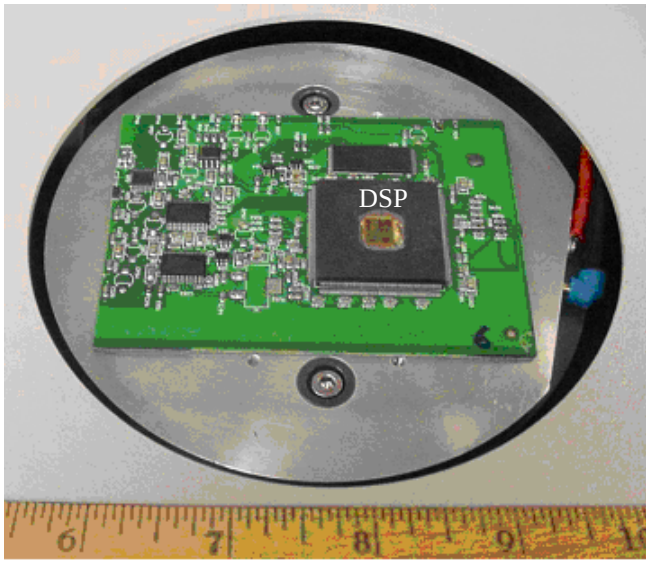


Figure 8: FICBM test method setup for the cut-down customer production board with the decapsulated DSP. The cuts were made along the top and left side of the PCB. Note that the DSP is located near the original corner of the PCB.

4. Production Board CBM Simulation Results

For three PCBs that were CBM tested as per the previous section (III.B.3), the DSPs showed Vdd bus damage similar to that in Figure 7a after -250V stressing. FIB analysis of these CBM failures consistently showed ~10 µm diameter circular areas of melted / reflowed AlCu with cracked / ruptured overlying passivation (see Figure 9). Thus, FICBM testing successfully replicated the real-world board failures (reference Figure 7b).

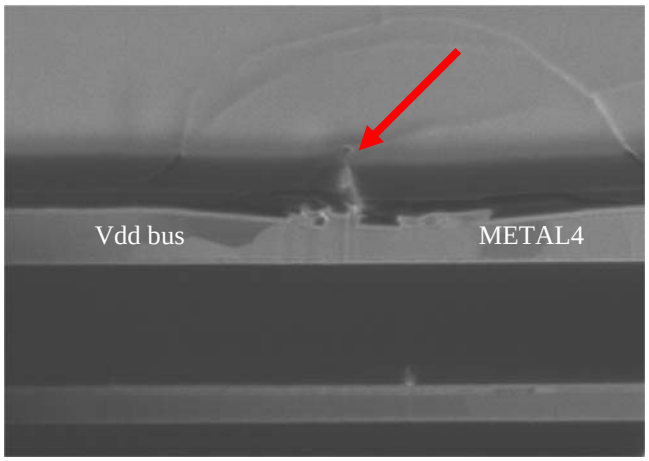


Figure 9: FIB cross-section image of the melted / reflowed MET4 AlCu (see arrow) and cracked glassivation on a DSP IC stressed at -250V CBM using the setup in Figure 8.

5. Effect of Multiple IC Supply Pins Soldered to PCB Power Planes

In Case Study 2, the DSP's 35 GND pins and 33 Vdd pins soldered to the PCB provided very low inductance and very low resistance connections between the DSP and the PCB ground and Vdd planes. To qualitatively determine how much this affected the CBM ESD results, CBM testing was conducted on two sets of cut-down PCBs:

1. **Controls:** Two PCBs with all 208 pins on the DSPs soldered to the board, including all 35 GND pins and 33 Vdd pins.
2. **Single Supply Pins:** Two PCBs as above, except all but one GND pin and one Vdd pin were mechanically cut away so that they no longer contacted the PCB power planes.

CBM testing was conducted as detailed in Section III.B.3 starting at ±125V in 125V increments. To minimize the time required to inspect the DSP die after PCB stressing at each voltage level, the inspection failure criteria was revised to be catastrophic damage readily visible during low magnification optical inspection as shown in Figure 10. Results of this testing are provided in Table 2.

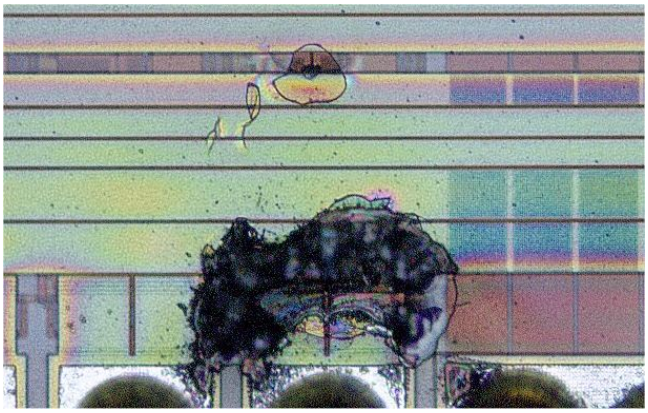


Figure 10: Typical catastrophic DSP damage observed along the supply buses and adjacent bond pads after stressing the cut-down customer boards at the CBM fail voltages listed in Table 2. Note the large areas of melted / reflowed AlCu and missing passivation above this damage.

Table 2: CBM results based on catastrophic damage as a function of the number of supply pins connected to the PCB

Pins Soldered to PCB	Pass	Fail
35 GND's + 33 Vdd's	875V	1000V
1 GND + 1 Vdd	1125	1250

6. Elimination of Real-World Failures

Investigation of the customer's board assembly process showed that the DSP on the PCB was sometimes charged to at least ±300V prior to wave soldering. Much of this charging was caused by the prior manufacturing step in which large plastic edge connectors were attached, resulting in inductive charging of the PCBs. Subsequent wave soldering instantaneously discharged the DSP and all other components on the PCB. As corrective action, the customer added an ionizer to their production line just prior to wave soldering to safely dissipate charges on the PCB. No ESD-related DSP failures have occurred subsequently, thus proving the effectiveness of this corrective action.

7. Discussion of Results

During component-level CDM testing of the DSP in a 208-lead MQFP package, the capacitance measured between a Vdd pin and the charging plate was ~25 pF. However, during CBM testing of this IC on the cut-down customer production board shown in Figure 8, the capacitance between the Vdd plane and the charging plate was ~460 pF. Thus, for a given charge voltage, the peak current during a CBM discharge was much higher than a CDM discharge. This can be seen in Figure 11 which shows a comparison of the 250V discharge waveforms at a ground pin on a stand-alone DSP (i.e., a FICDM discharge) versus a GND test pad when the DSP was on the cut-down board (i.e., a FICBM discharge) with all 35 GND and 33 Vdd pins connected to the PCB power planes. As with the Case Study 1 waveforms in Figure 5, note that the Case Study 2 board discharge waveform has a faster rise time than the device discharge waveform due to the lower inductance and resistance of the board discharge path.

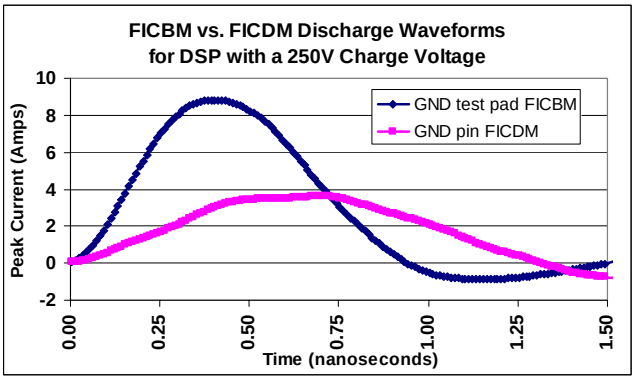


Figure 11: Comparison of FICBM vs. FICDM discharge waveforms at a DSP ground pad / pin showing the higher energy in the CBM event for the cut-down PCB shown in Figure 8.

Based on the design of the production board PCB, when the charging plate was charged negatively during FICBM testing, a positive charge was induced on the ground plane on the bottom of the production board and a negative charge was induced on the internal Vdd plane above this ground plane. When the ground plane was discharged (i.e., grounded), much of the negative charge stored by the Vdd plane on the PCB was channeled through the DSP since it provided such a low impedance path to the ground plane. During this specific discharge event, this low impedance was due to the combination of the following factors:

- The 33 parallel Vdd pins on the DSP package that were connected to the Vdd plane provided a much lower resistance / inductance discharge path between the Vdd plane and the DSP than any other IC on the PCB. (Other ICs on the PCB had only one Vdd pin tied to the Vdd plane.)
- The DSP has a large die with $>10^5$ parallel forward-biased diodes formed between the N-Wells tied to Vdd and the large P-substrate tied to GND. These $>10^5$ parallel diodes provide a far lower "on" resistance (only ~0.2Ω) during high-current, forward-biased operation than any other diode paths on the PCB.
- The 35 parallel GND pins on the DSP package that were connected to the ground plane provided a much lower resistance / inductance discharge path between the DSP and the ground plane than any other IC on the PCB. (Other ICs on the PCB had only one GND pin tied to the ground plane.)

The combination of the above factors caused the DSP to be the primary CBM discharge path between the negatively-charged PCB Vdd plane and the PCB ground plane when it was grounded during the CBM event. Thus, the charge voltage required to damage the DSP's Vdd buses at the board-level (i.e., -250V) was <10% of that required to cause such damage at the component-level (i.e., >2500V).

As expected, the CBM ESD withstand voltage of the DSP was higher when only one GND and one Vdd pin was connected to the PCB (reference Table 2). This is because single supply connections increase the resistance / inductance of the discharge path through the DSP, and consequently more of the CBM ESD current flows through other components on the PCB.

IV. Conclusions

Key findings / conclusions from this work are as follows:

1. Using a commercial CDM test system, a CBM test method was developed that successfully simulates real-world CBM failures.
2. Since PCB capacitance is much higher than IC package capacitance, a CBM discharge has much higher energy than a CDM discharge for a given charge voltage. In addition, CBM discharges generally have faster rise times than CDM discharges. Thus, ICs that are effectively immune to ESD damage at the device-level may be susceptible to ESD damage at the board-level. For example, as shown in Case Study 2, a DSP IC had a CBM withstand voltage that was <10% of its CDM withstand voltage.
3. Due to the high energy associated with real-world CBM discharges, CBM ESD damage can be far more severe than typical device-level ESD damage. Consequently, CBM ESD damage can be easily mistaken for EOS damage. For example, Figures 4 and 10 show CBM damage that might incorrectly be attributed to EOS damage.
4. Before attributing IC failures to EOS, the possibility of CBM ESD damage should be explored. This is particularly important since an FA report that incorrectly concludes that an IC failed due to EOS damage can trigger investigations that will not result in effective corrective actions. For example, likely sources of board-level EOS include: power supply transients; improper power supply sequencing; inductive load dumps; improper orientation of the IC on the PCB; and applications errors. Investigating these and other possible sources of EOS may be highly time-consuming and will not identify the root cause of failure if the IC damage was caused by a CBM ESD discharge rather than an EOS event.
5. For a given PCB design that uses the same IC in multiple board positions, an unusually high failure rate of this IC for a given board position should trigger an investigation into the possibility of CBM ESD damage.
6. ICs that are adjacent to large insulators such as plastic sockets or plastic connectors and ICs that are close to PCB edges (especially PCB corners, edge connectors, mounting holes, and test points) are particularly susceptible to CBM ESD damage.
7. For a given IC, CBM susceptibility depends on the overall area and layout of the PCB power planes. Larger power planes typically result in larger capacitance, thus resulting in lower overall IC CBM withstand voltages than smaller power planes.
8. For a given IC, CBM susceptibility depends on the number of power supply pins connected to the PCB power planes. Multiple IC connections to power planes result in lower resistances and inductances for CBM discharge currents, thus resulting in lower overall IC CBM withstand voltages.
9. Large PCB power planes and/or numerous IC connections to power planes may be required for electrical performance reasons. Therefore, the key to eliminating real-world CBM failures is to implement manufacturing controls to ensure that rapid PCB discharging does not occur [16]. PCBs are most susceptible to CBM ESD damage during the processing steps from when they are first populated with components until they are finally inserted into a case or other enclosure that provides adequate ESD protection. As shown in these two case studies, precautions should especially be taken to ensure PCBs are not charged prior to convection / IR reflow or wave soldering, since these process steps are common sources of CBM discharges.
10. The ESDA should consider developing a formal CBM ESD standard test method.

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