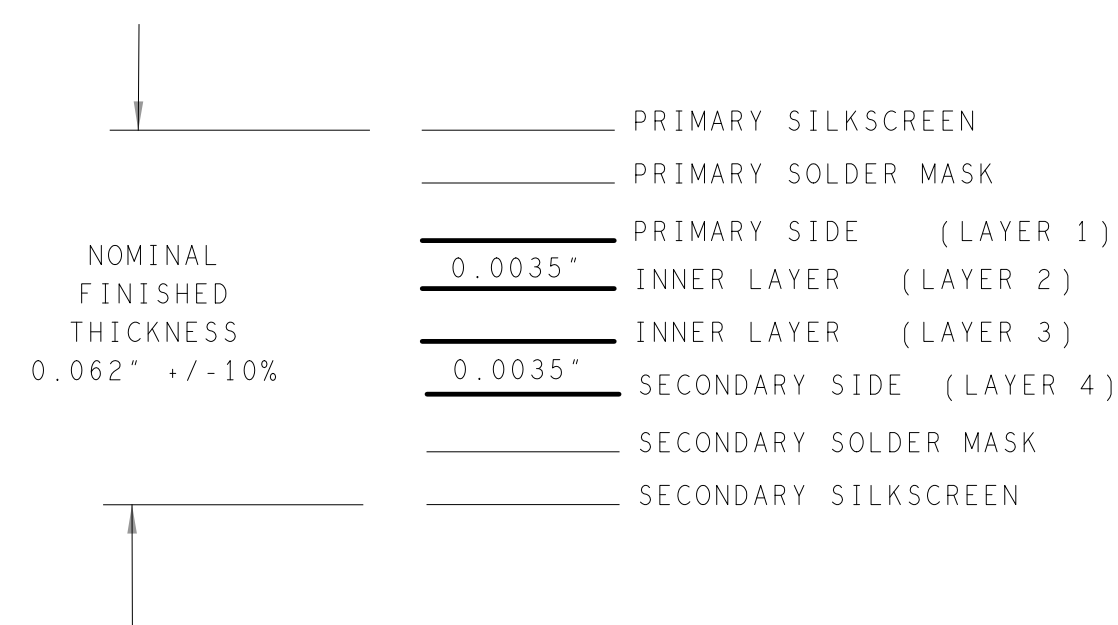


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE	10-03-2022	X
B	ECR-112470	1-17-2023	X

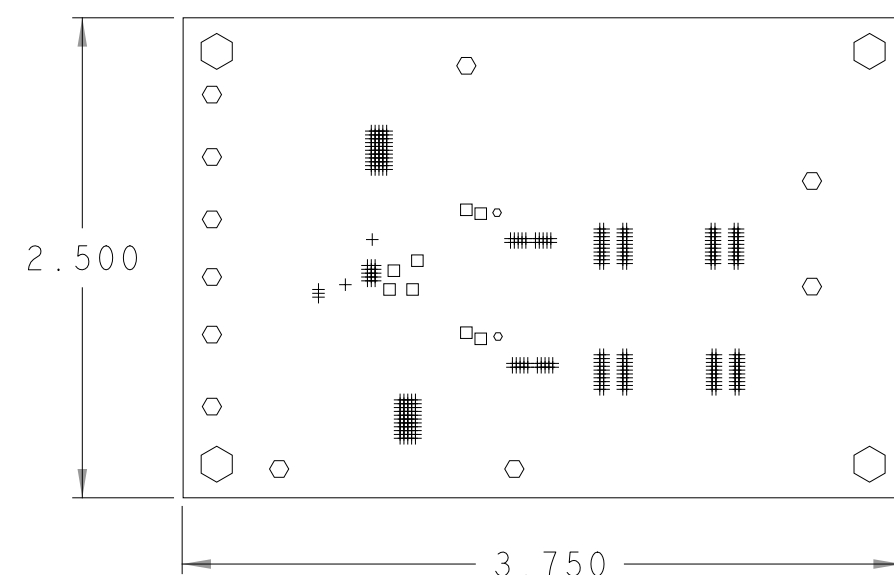
4 LAYER STACKUP



HOLE TOLERANCE

UNLESS SPECIFIED
PLATED: $\pm .003$
NON PLATED: $+.002 / -.001$

FINISHED HOLES IN MILS				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	PLATED	QTY	TOLERANCE/NOTES
+	10.0	PLATED	1469	
□	12.0	PLATED	8	
○	45.0	PLATED	2	
○	100.0	PLATED	11	
⬡	187.0	NON-PLATED	4	



SPECIFICATIONS:

MATERIALS; ALL LAMINATES AND BONDING MATERIALS SHOULD BE SELECTED FROM
IPC-4101 OR IPC-4103, MINIMUM Tg>170degC, Td>300degC,
U.L. RATING OF 94 V-0

MATERIAL FAMILY; FR4

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CLADDING;          EXTERNAL LAYERS 2 OZ. COPPER.
                   INTERNAL LAYERS 1 OZ. COPPER.
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NOTE: IF THE LAYER STACKUP CONFLICTS WITH THE ABOVE
CLADDING SPECIFICATIONS THEN THE LAYER STACKUP SHALL
TAKE PRECEDENCE.

SOLDER MASK; SHALL BE LIQUID PHOTOIMAGEABLE (LPI) APPLIED ON BOTH SIDES
OVER BARE COPPER OR GOLD AND SHALL MEET IPC-SM-840
(LATEST REV.) CLASS 3. COLOR BLUE.

SILK SCREEN; SHALL BE PERMANENT NON-CONDUCTIVE EPOXY INK, COLOR: WHITE
SYNTHETIC INKJET PRINTING ALLOWED FOR DENSE BOARDS,
COLOR: WHITE

SURFACE FINISH; ENIG (Electroless Nickel/Immersion Gold)
PER IPC-4552 LATEST REVISION

INTENTIONAL SHORTS; IF SUPPLIED DATA INCLUDES A FILE "READ_ME.2", THEN
INTENTIONAL NET SHORTS EXIST. CUSTOMER REVIEW AND APPROVAL
IS REQUIRED IF SUPPLIED DATA REPORTS ANY CONDITION THAT
DOES NOT MATCH "READ_ME.2" FILE PROVIDED.

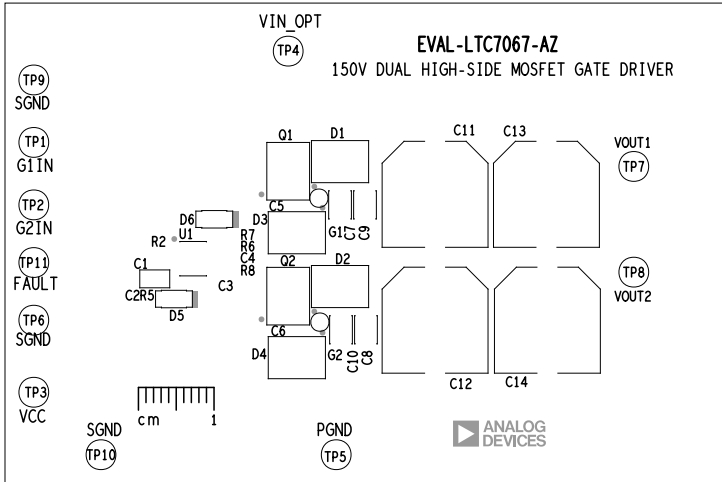
TEST REQUIREMENTS:	100% NETLIST ELECTRICAL VERIFICATION USING CUSTOMER SUPPLIED IPC-D-356 NETLIST FOR OPENS AND SHORTS WHEN "GERBER DATA" IS PROVIDED. THIS VERIFICATION ALSO REQUIRED FOR "ODB++" DATA PER EMBEDDED NETLIST.
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REQUIREMENTS:

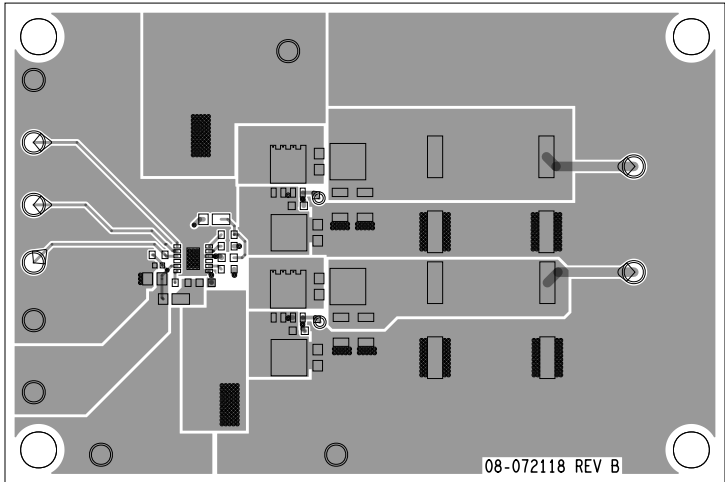
1. REFER TO IPC-6010 SERIES (LATEST REV.), CLASS 2 FOR FABRICATION UNLESS OTHERWISE SPECIFIED.
2. ACCEPTABILITY PER ANALOG DEVICES, INC. SPECIFICATION TST00115, (LATEST REVISION.)
3. MODIFICATIONS TO THE ARTWORK ARE NOT ALLOWED WITHOUT WRITTEN AUTHORIZATION.
4. HOLE PATTERN TOLERANCES FOR UNDIMENSIONED HOLES SHALL BE A DIAMETER OF 0.005 INCHES FROM THEIR TRUE POSITION.
5. PLATED HOLE WALL THICKNESS SHALL NOT BE LESS THAN 0.001 INCH MINIMUM AVERAGE, WITH NO READING LESS THAN .0008 BY CROSS SECTION.
6. HOLE DIAMETERS APPLY AFTER PLATING.
7. FINISHED CONDUCTOR WIDTHS SHALL NOT BE REDUCED FROM THE NOMINAL INDICATED ON THE MASTER PATTERN, BY MORE THAN THE CONDUCTOR THICKNESS.
8. MINIMUM DESIGN LINE WIDTH IS .XXX INCH.
9. MINIMUM DESIGN SPACING IS .XXX INCH.
10. NON-FUNCTIONAL PAD REMOVAL FROM INNER SIGNAL LAYERS MAY BE PERFORMED AFTER CUSTOMER APPROVAL.
11. IF PAD SIZES PROVIDED ARE NOT LARGE ENOUGH TO MAINTAIN ANNULAR RING REQUIREMENT, MFRG. MAY REQUEST APPROVAL TO TEAR DROP PADS TO MAINTAIN ANNULAR RING. (AT PAD TO TRACE INTERSECTION ONLY AND ELECTRICAL INTEGRITY MUST BE MAINTAINED.)
12. THEIVING MAY BE ADDED TO COMPENSATE FOR LOW COPPER DENSITY AREAS ON THIS DESIGN ONLY AFTER REVIEW AND APPROVAL FROM THE CUSTOMER:
 - A. THEIVING TO CARD EDGE, FIDUCIALS, NON-PLATED THROUGH HOLES, ALL OTHER FEATURES TO BE 0.200 INCH MINIMUM.
 - B. THERE SHALL BE NO THEIVING IN ANY AREAS FREE OF SOLDER MASK OR INTERNAL COPPER PLANES.
13. MFRG. TO LEGIBLY ETCH OR STAMP/SCREEN WITH PERMANENT NON-CONDUCTIVE INK ON SECONDARY SIDE IN A CLEAR AREA UNLESS OTHERWISE INDICATED;
 - A. U.L. CODE-FLAMMABILITY RATING
 - D. MFRG LOGO
 - B. DATE CODE (STAMP).
 - E. SUCCESSFUL ELECTRICAL TEST
 - C. LOT NUMBER
14. REPAIRS PER IPC-7711/21 (LATEST REV.) ARE ALLOWED. REPAIRS ARE NOT ALLOWED IN ANY AREA DEFINED ON GOLD_PRM AND/OR GOLD_SEC ARTWORK LAYERS WHEN PROVIDED IN GERBER OR ODB++, DATA

PRIMARY SIDE

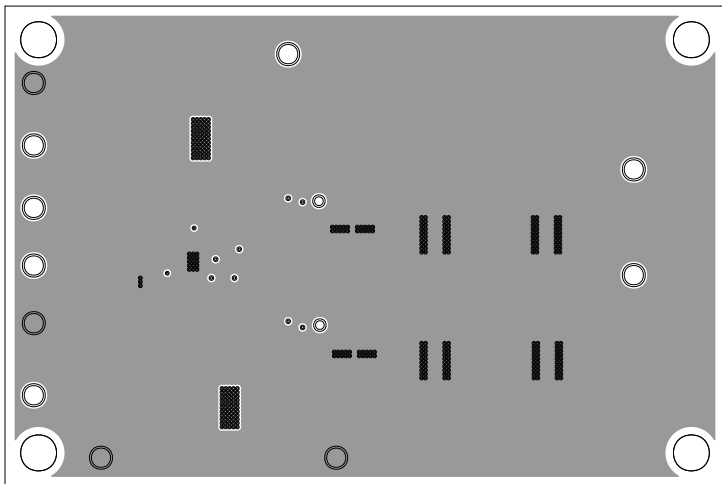
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		APPROVAL		DATE			
TOLERANCES		TEMPLATE DESIGNER BILLY PHILLIPS		01SEP20			
DECIMALS	FRACTIONS	HARDWARE SERVICES BOB MC DONALD		01SEP20			
.XX --.010	--1/32	HARDWARE SYSTEMS DAVE WILLIAMS		01SEP20			
.XXX --.000		COMPONENT DESIGNER ADGT LIBRARY		01SEP20			
.XXXX --.0000	--.2						
MATERIAL						TITLE FABRICATION EVAL-LTC7076-AZ	
		HARDWARE RELEASE X		6999yy			
FINISH		PCB DESIGNER X		6999yy		SIZE	
		PTD DESIGNER X		6999yy		FSOM NO	
		CHECKER X		6999yy		DRAWING NUMBER	
						REV	
DO NOT SCALE DWG						D 24355 09-072118 X B	
						SCALE 1 / 1	
						SHEET 1 of 1	



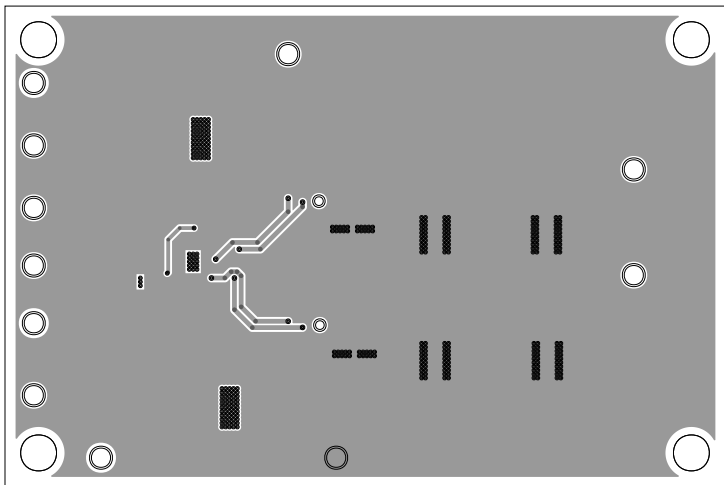
SILKSCREEN PRIMARY
08-072118 -03 DATE: 2-1-2023
EVAL-LTC7067-AZ REV B



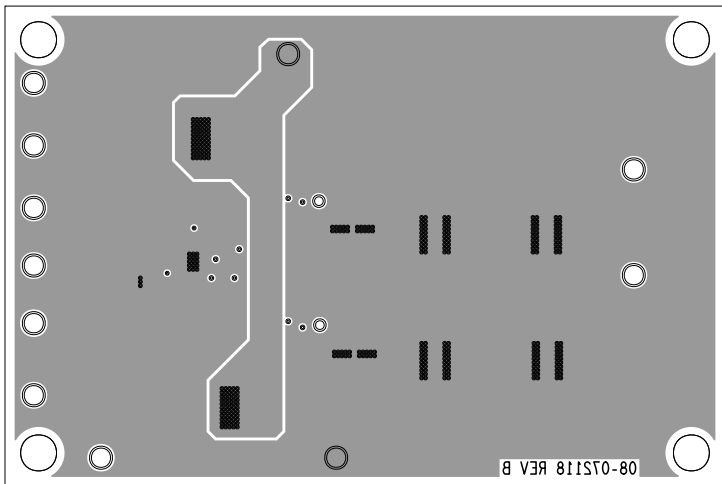
L1 PRIMARY
08-072118 -01 DATE: 2-1-2023
EVAL-LTC7067-AZ REV B



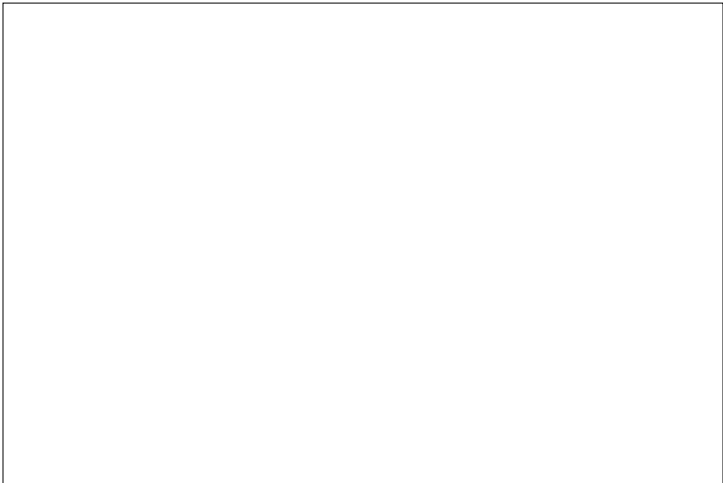
L2
08-072118 -08 DATE: 2-1-2023
EVAL-LTC7067-AZ REV B



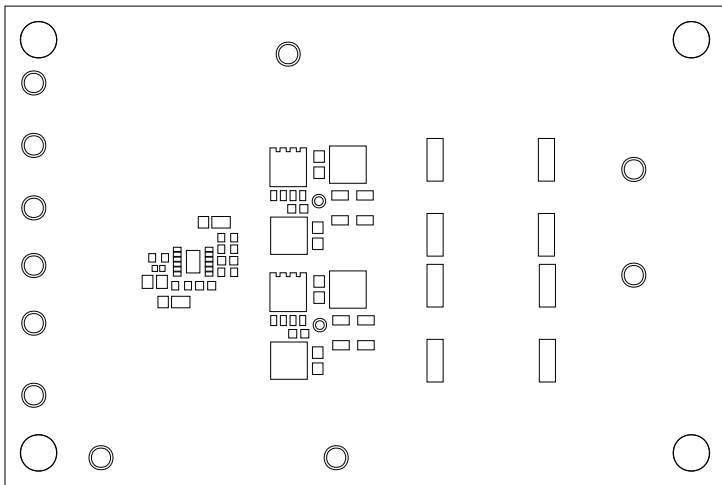
L3
08-072118 -09 DATE: 2-1-2023
EVAL-LTC7067-AZ REV B



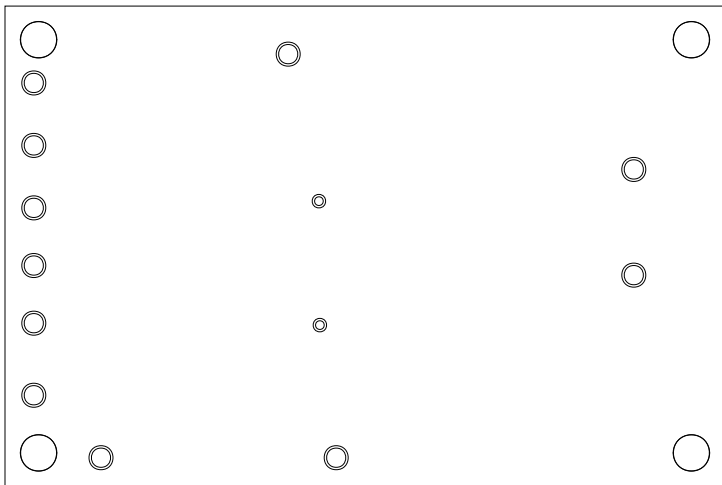
L4 SECONDARY
08-072118 -10 DATE: 2-1-2023
EVAL-LTC7067-AZ REV B



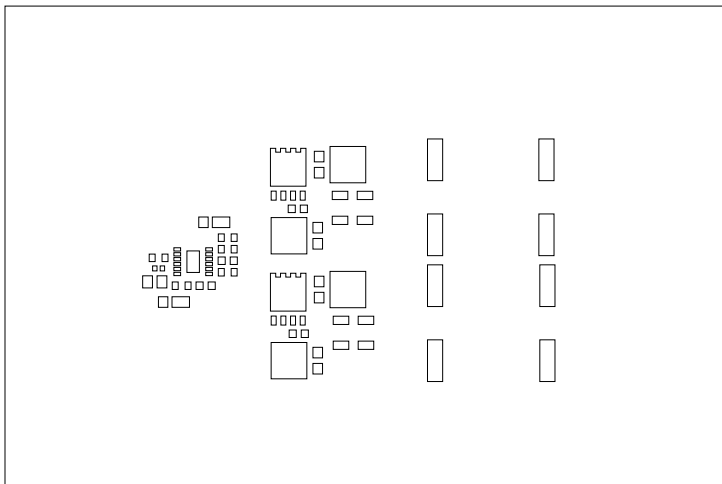
SILKSCREEN SECONDARY
08-072118 -05 DATE: 2-1-2023
EVAL-LTC7067-AZ REV B



SOLDERMASK PRIMARY
08-072118 -04 DATE: 2-1-2023
EVAL-LTC7067-AZ REV B



SOLDERMASK SECONDARY
08-072118 -06 DATE: 2-1-2023
EVAL-LTC7067-AZ REV B



PASTEMASK PRIMARY
08-072118-13 DATE: 2-1-2023
EVAL-LTC7067-AZ REV B