

8

7

6

5

4

3

2

1

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RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

JUMPER TABLE		
JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

TEMPLATE ENGINEER
-

HARDWARE SERVICES
-

HARDWARE SYSTEMS
-

TEST ENGINEER
-

COMPONENT ENGINEER
-

TEST PROCESS
-

HARDWARE RELEASE
-

DESIGNER
-

PTD ENGINEER
DEREK SAM

CHECKER
-

DATE

SCHEMATIC

EVAL-ADIN3310EBZ
Product(s): ADIN3310
<PRODUCT_1>
Customer Evaluation
-
<User Define>
<User Define>
<User Define>

MASTER PROJECT TEMPLATE
TBD

TESTER TEMPLATE
067706_a

DRAWING NO.
02-068019

REV.
B

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES

DECIMALS
X.XX +0.010
X.XXX +0.005

FRACTIONS
+1/32

ANGLES
+2

SIZE
D

SCALE
1:1

CODE ID NO.
CodeID

SHEET 1 OF 10

ANALOG
DEVICES

8

7

6

5

4

3

2

1

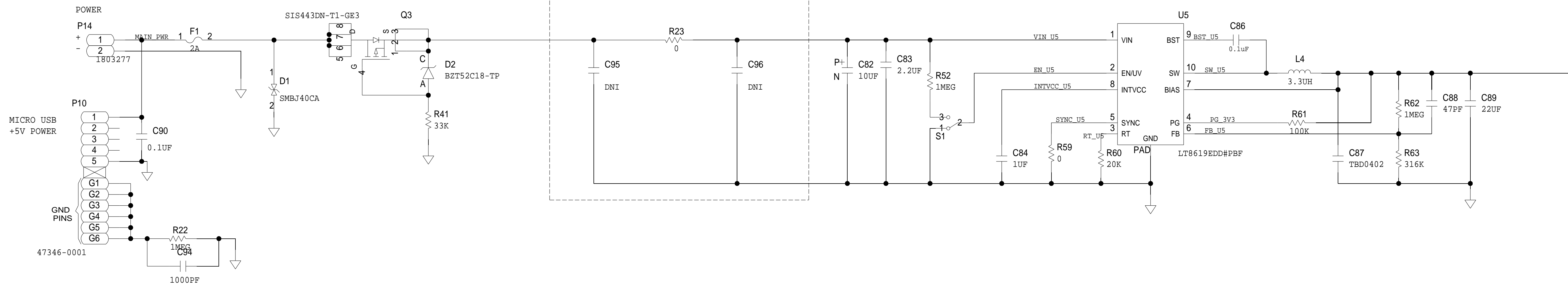
DRAFT

BOARD POWER & GLOBAL RESET

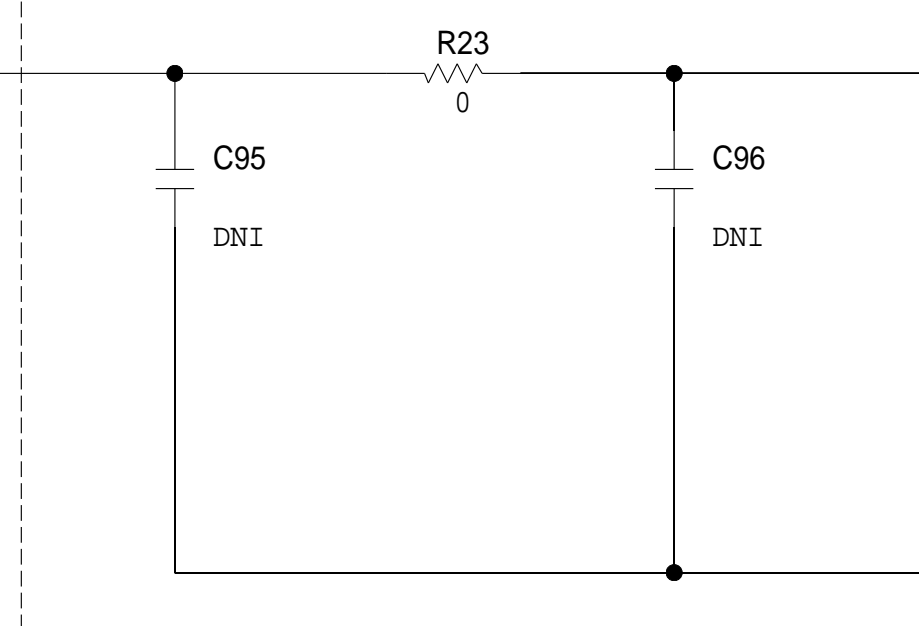
REVISIONS

REV	DESCRIPTION	DATE	APPROVED

BOARD PWR

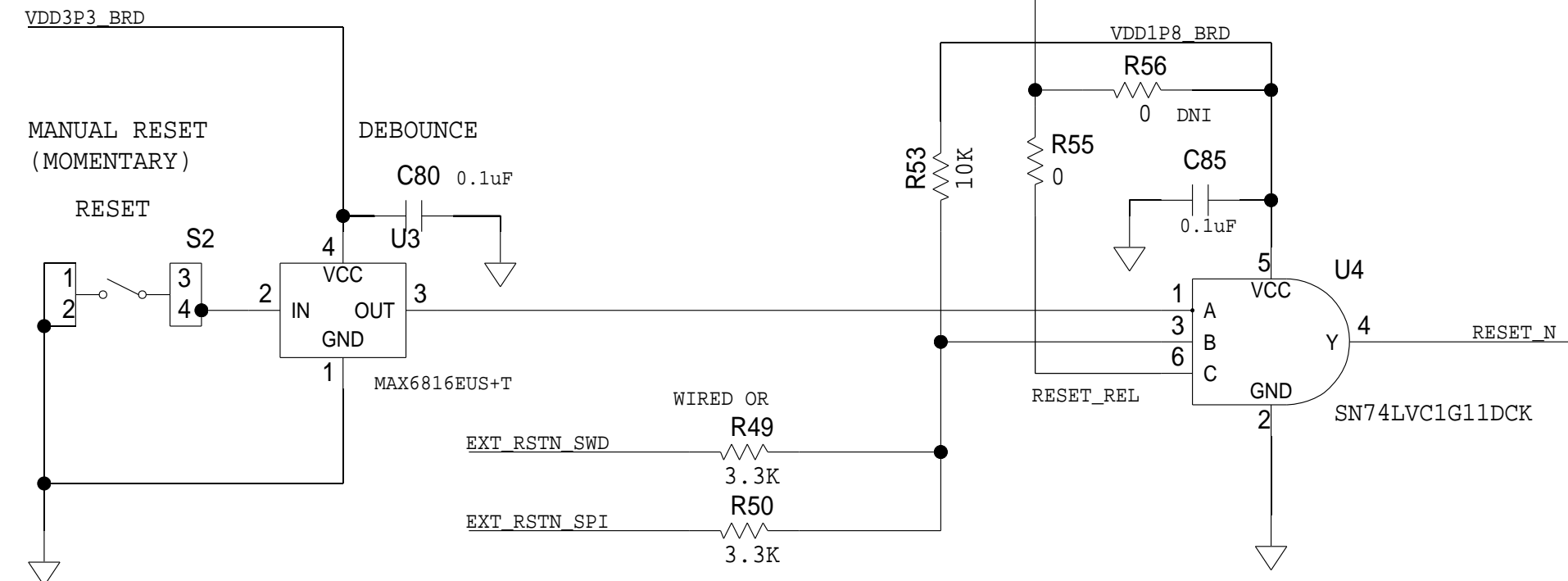


EMI FILTER

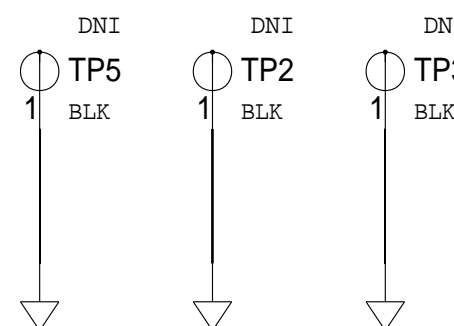


FOR VDDIO=1.8V SHORT 2&3 (DEFAULT)
FOR VDDIO=3.3V SHORT 1&2

RESET CKT



GND HOOKS



SCHEMATIC

EVAL-ADIN3310EBZ
Product(s): ADIN3310
<PRODUCT_1>

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
DEREK SAM

DRAWING NO.
02-068019

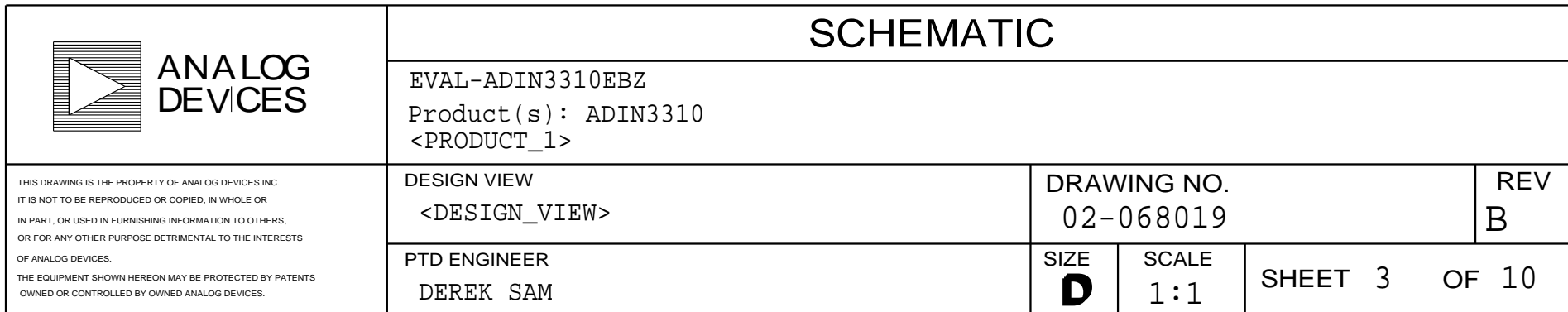
REV
B

SIZE
D

SCALE
1:1

SHEET 2 OF 10

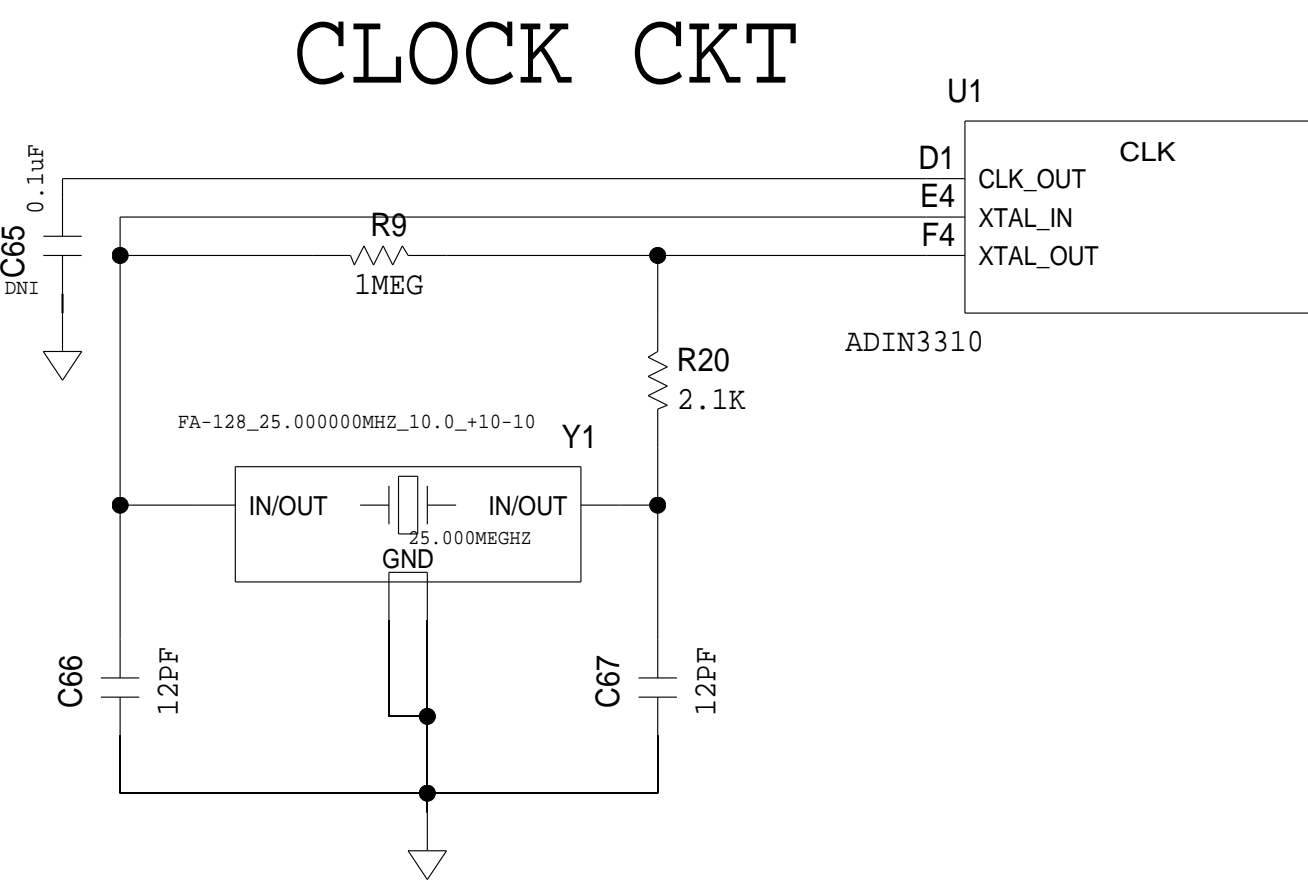
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



OTHER ADIN3310 CONNECTIONS - CLK, SWD, MDIO & LEDS

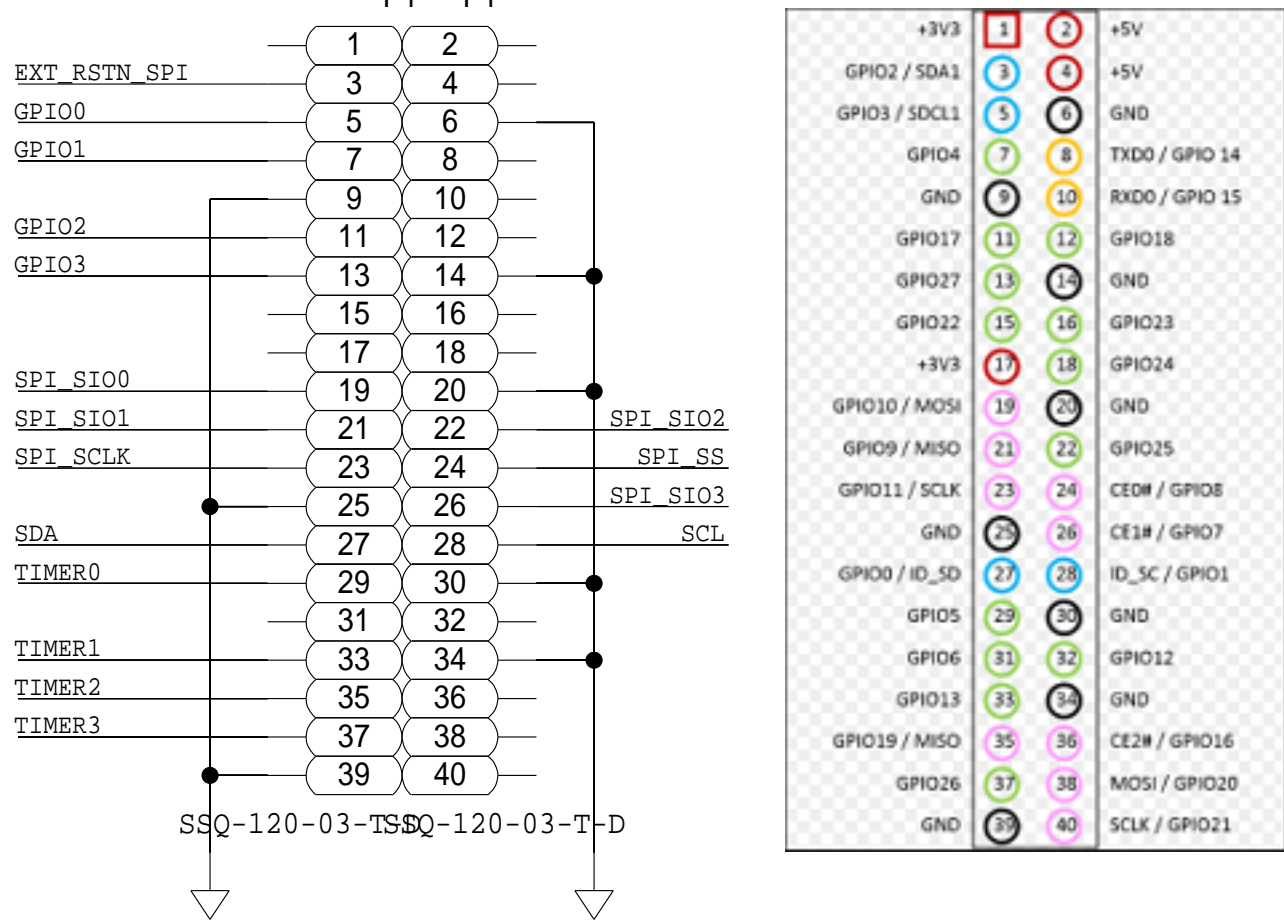
U1	A13	RESET_N
	H14	SPI_SCLK
	L12	SPI_SIO0
	K12	SPI_SIO2
	J13	SPI_SIO1
	J12	SPI_SIO3
	H12	SPI_SS
	H13	GPIO0
	G14	GPIO2
	G13	GPIO3
	G12	GPIO1
	B13	MDC
	B12	MDIO
	D13	SWCLK
	D12	SWDIO
	A11	SWV
	F14	TIMER0
	F13	TIMER1
	E14	TIMER2
	D14	TIMER3

ADIN3310



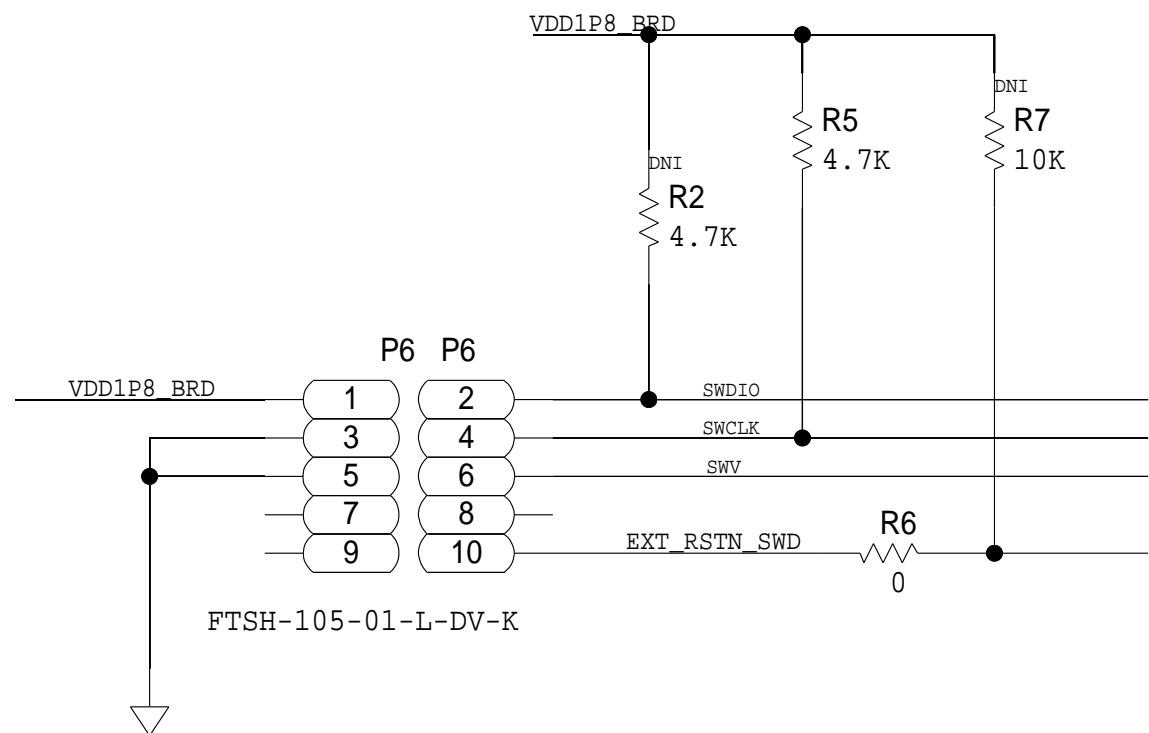
Layout: all clks should be routed with 500hm trace char impedance

Q\D\S SPI INTERFACE & PI HAT CONN.
PI IS INSERTED ON BOTTOM LAYER

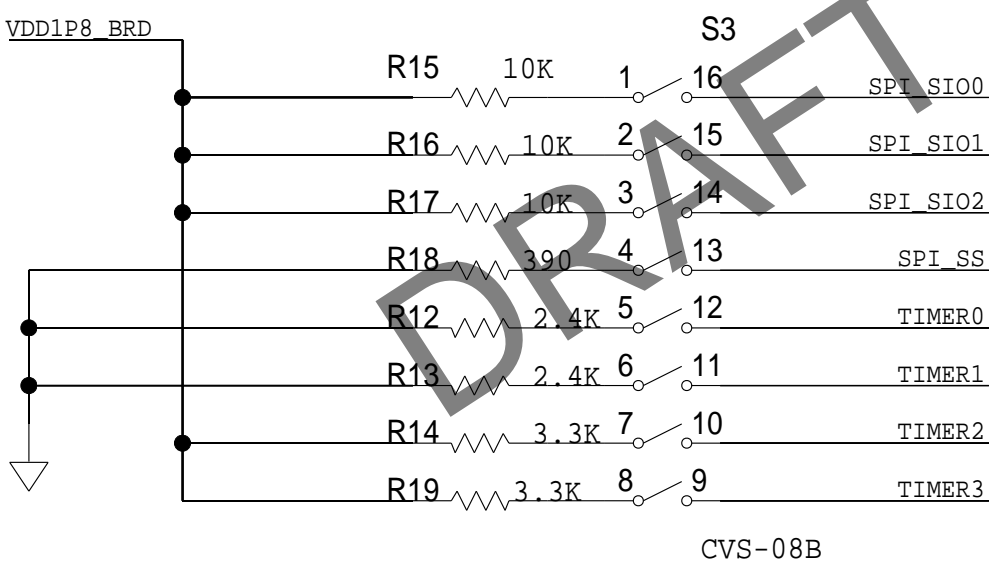


+3V3	1	2	+5V
GPIO2 / SDA1	3	4	+5V
GPIO3 / SDC1	5	6	GND
GPIO4	7	8	TXD0 / GPIO14
GND	9	10	RXD0 / GPIO15
GPIO17	11	12	GPIO18
GPIO27	13	14	GND
GPIO22	15	16	GPIO23
+3V3	17	18	GPIO24
GPIO10 / MOSI	19	20	GND
GPIO9 / MISO	21	22	GPIO25
GPIO11 / SCLK	23	24	CEM / GPIO6
GND	25	26	CE1A / GPIO7
GPIO0 / ID_0	27	28	ID_3C / GPIO1
GPIO5	29	30	GND
GPIO6	31	32	GPIO12
GPIO13	33	34	GND
GPIO19 / MISO	35	36	CE2A / GPIO16
GPIO26	37	38	MOSI / GPIO20
GND	39	40	SCLK / GPIO21

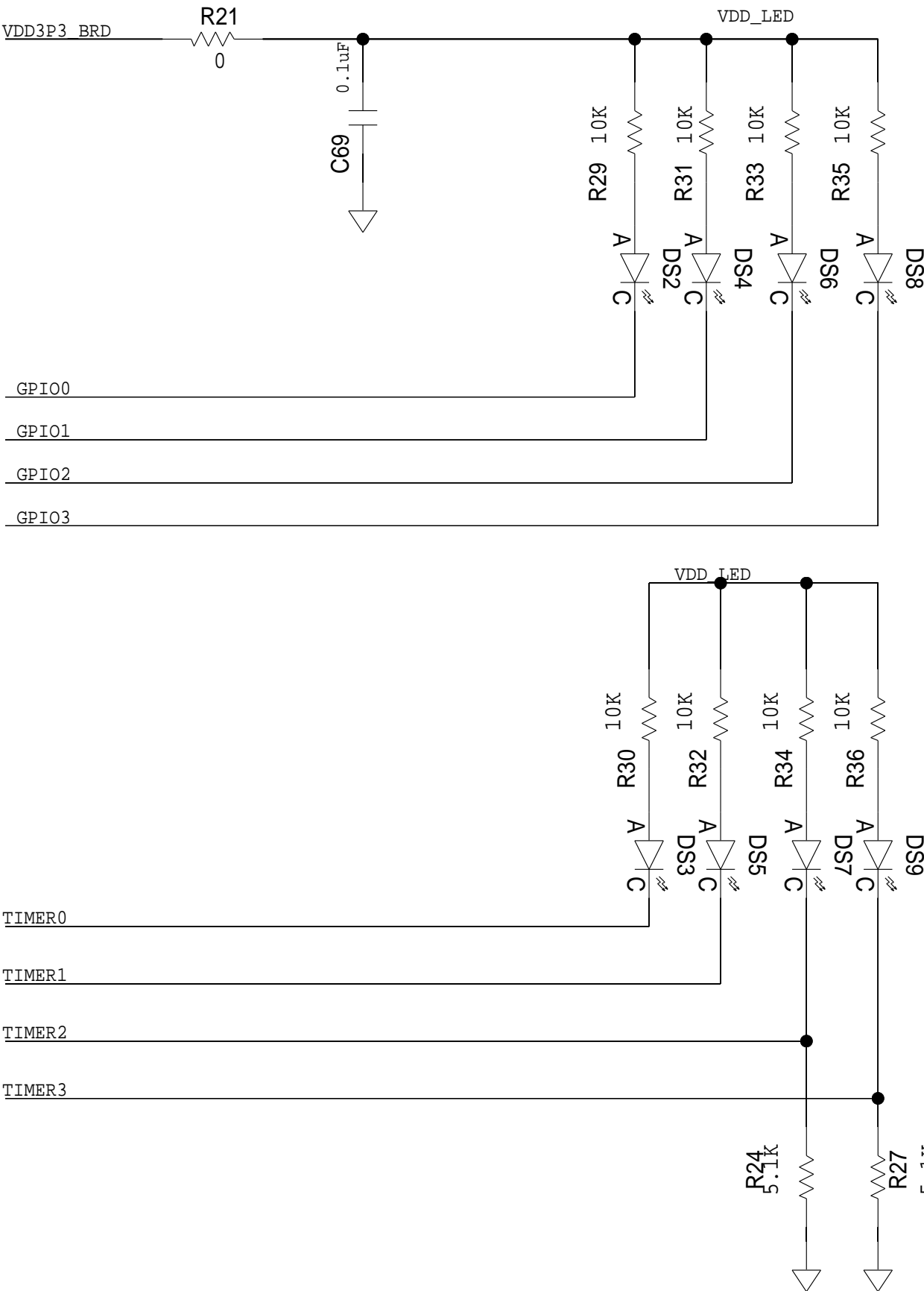
SWD INTERFACE
(INTERNAL DEBUG ONLY)



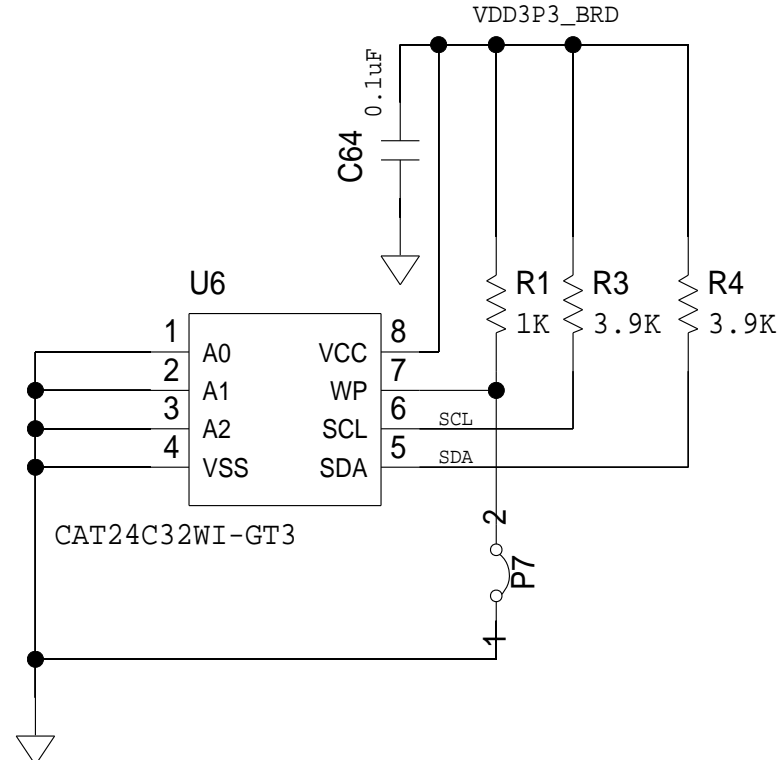
STRAPPING & HOST PORT SEL.



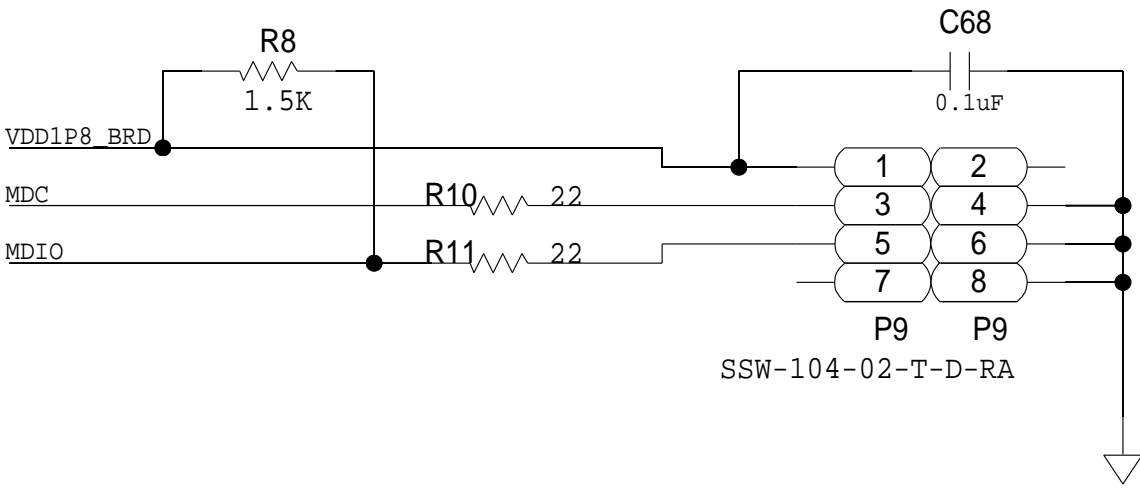
LEDS



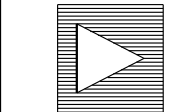
EEPROM
(PI HAT REQUIREMENT)



MDIO EXT INTERFACE CONNECTOR
(INTERNAL DEBUG ONLY)



<https://github.com/raspberrypi/hats/blob/master/designguide.md>



ANALOG
DEVICES

SCHEMATIC

EVAL-ADIN3310EBZ
Product(s): ADIN3310
<PRODUCT_1>

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
DEREK SAM

DRAWING NO.
02-068019

SIZE
D

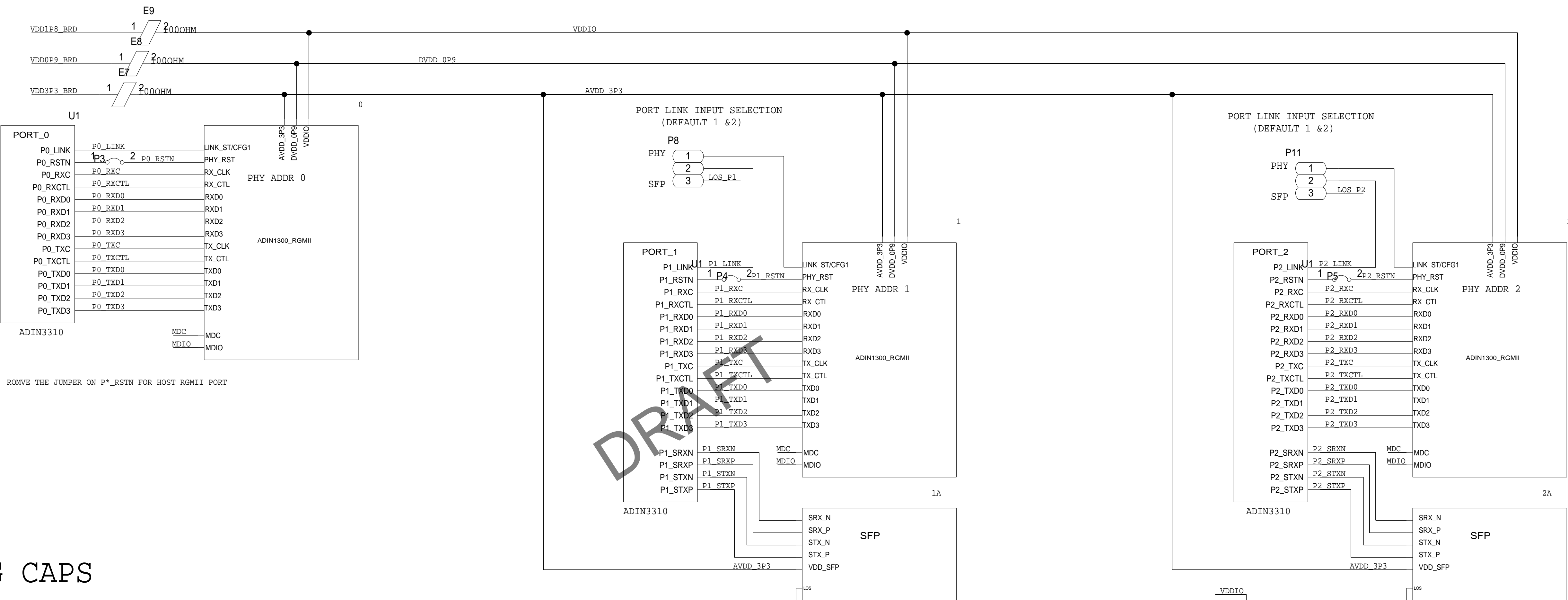
SCALE
1:1

SHEET 4 OF 10

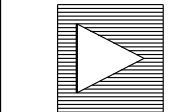
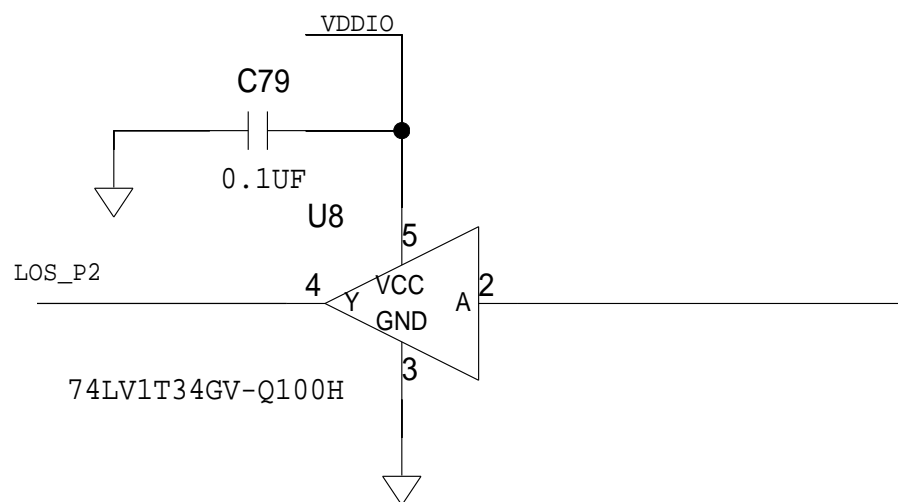
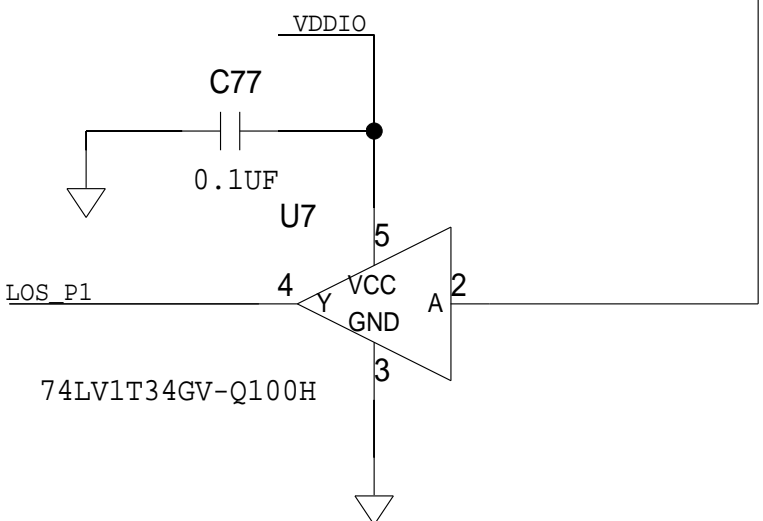
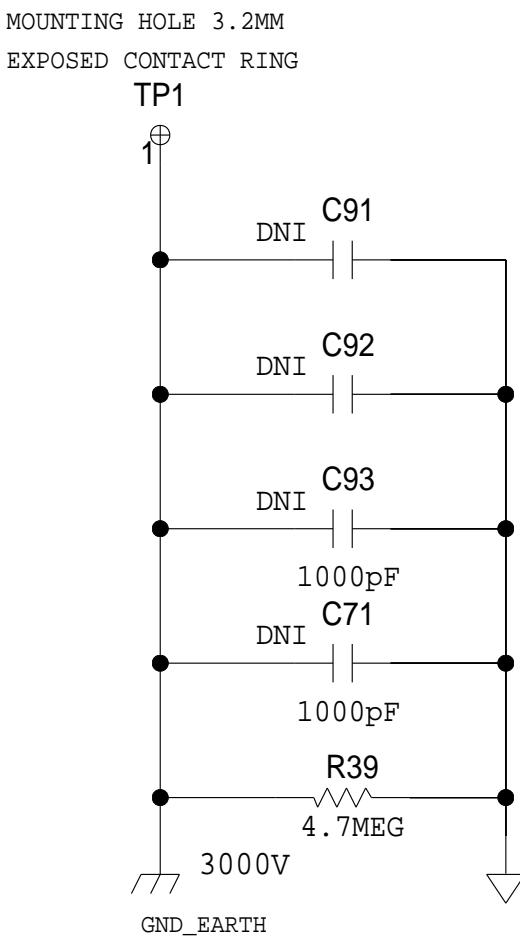
REV
B

PHYS: (ADIN1300 & SFP)

ADIN1300 - RGMII
SFP - SGMII



STITCHING CAPS



ANALOG
DEVICES

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SCHEMATIC				
EVAL-ADIN3310EBZ Product(s): ADIN3310 <PRODUCT_1>				
DESIGN VIEW <DESIGN_VIEW>			DRAWING NO. 02-068019	REV B
PTD ENGINEER DEREK SAM	SIZE D	SCALE 1:1	SHEET 5 OF 10	

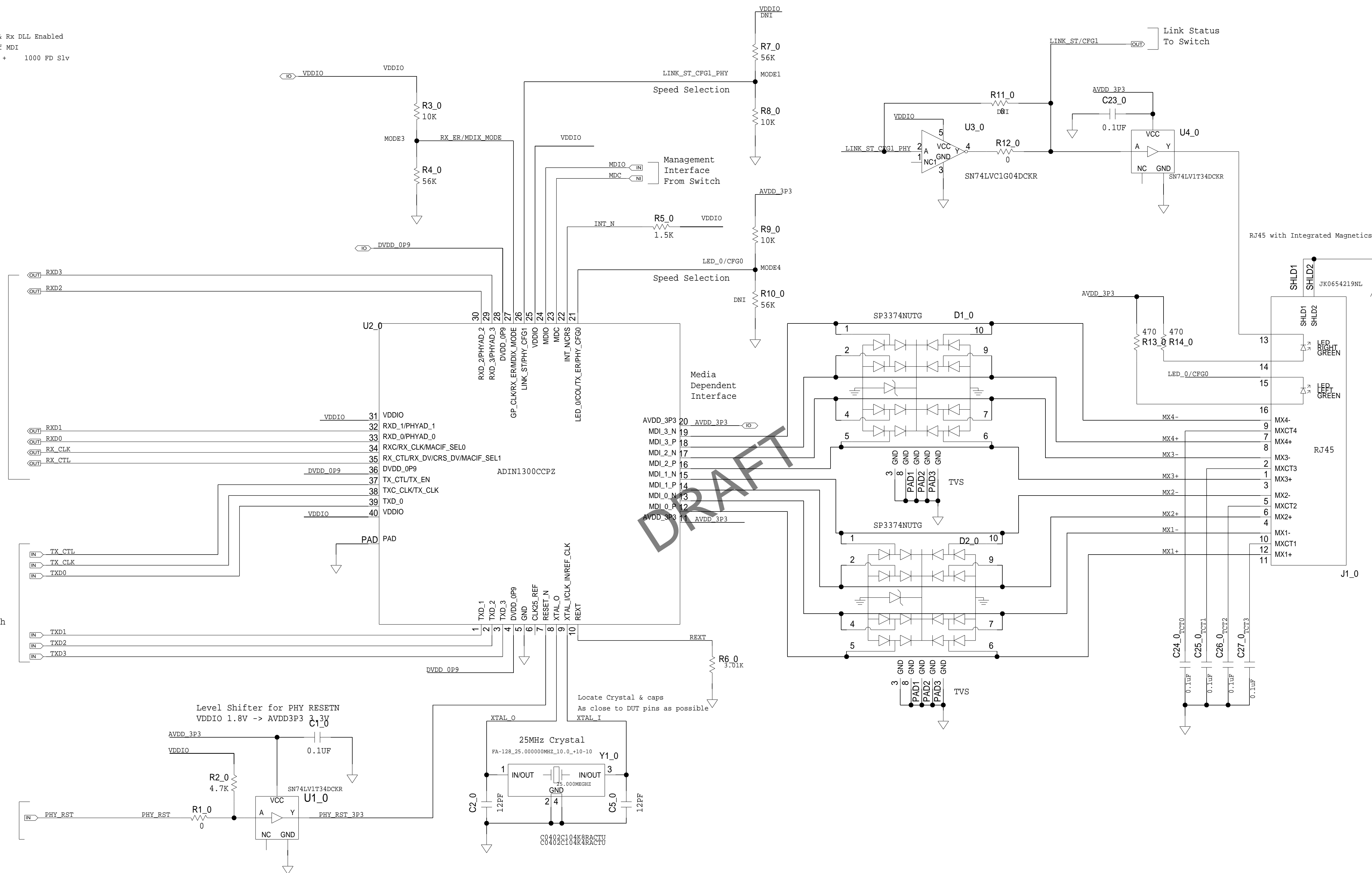
Gb Ethernet PHY with ADIN1300

PHY Strapping:

MAC INTERFACE: RGMII with Tx & Rx DLL Enabled
MDI MODE SEL AutoMDI+ Pref MDI
SPEED CONFIG: 10/100 HD/PD + 1000 PD Slv

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

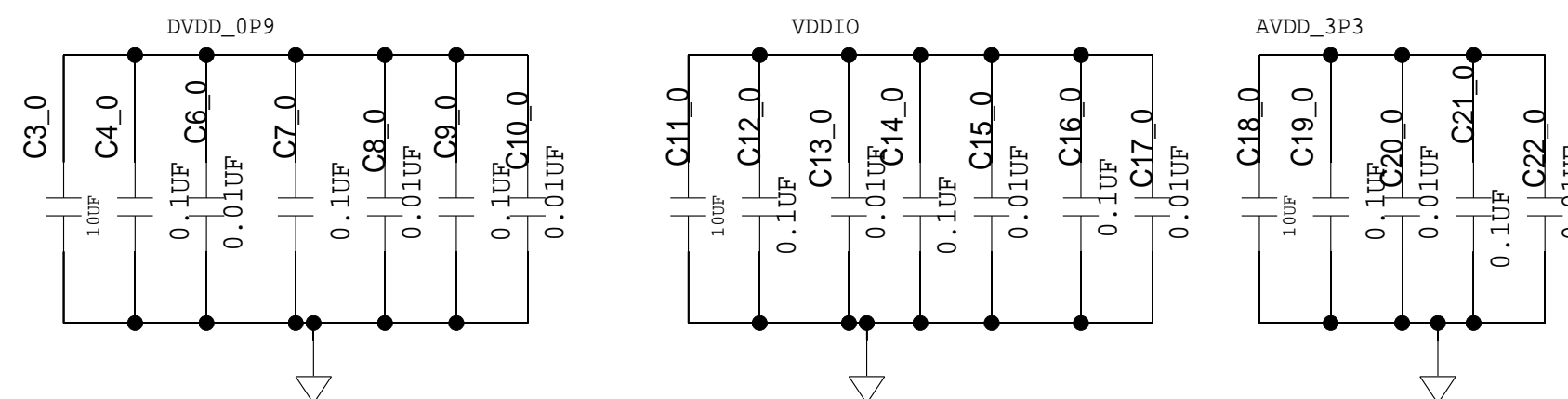


LAYOUT NOTES:

- 2.3.2. RGMII/RMII (125MHz)
- Plan components on RGMII ports 1 & 4 towards top edge and all others towards the bottom edge.
- Route P*_Tx/P*_Rx signals with 500ohm Char Impedance.
- All signals within Tx group (P*_TXCL, P*_TXD<0:3>, P*_TXCTL) should be length matched.
- All signals within Rx group (P*_RXCL, P*_RXD<0:3>, P*_RXCTL) should be length matched
- No length matching required between signals of different ports
- No length matching required between Tx & Rx groups
- Route All RGMII signals in Top layer . Keep routing lengths as small possible
- All clocks should be routed with 500ohm char impedance

DECOUPLING CAPS:

0.1uF & 0.01uF caps per pin

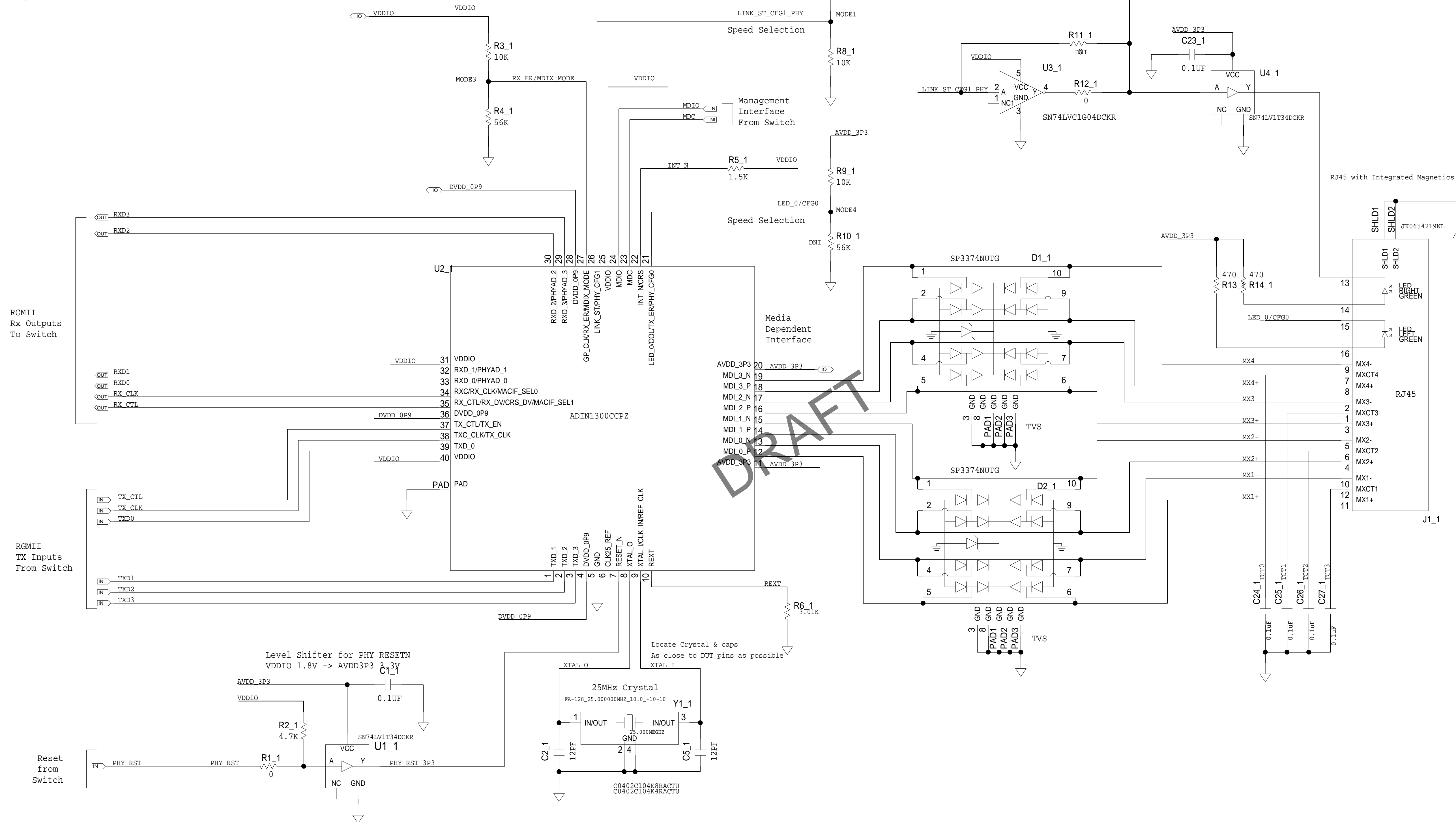


SCHEMATIC			
ANALOG DEVICES		EVAL-ADIN3310EBZ Product(s): ADIN3310 <PRODUCT_1>	
DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02-068019	REV B
PTD ENGINEER DEREK SAM		SIZE D	SCALE 1:1
		SHEET 6	OF 10

Gb Ethernet PHY with ADIN1300

PHY Strapping:

MAC INTERFACE: RGMII with Tx & Rx DLL Enabled
MDI MODE SEL AutoMDI+ Pref MDI
SPEED CONFIG: 10/100 HD/FD + 1000 FD Slv

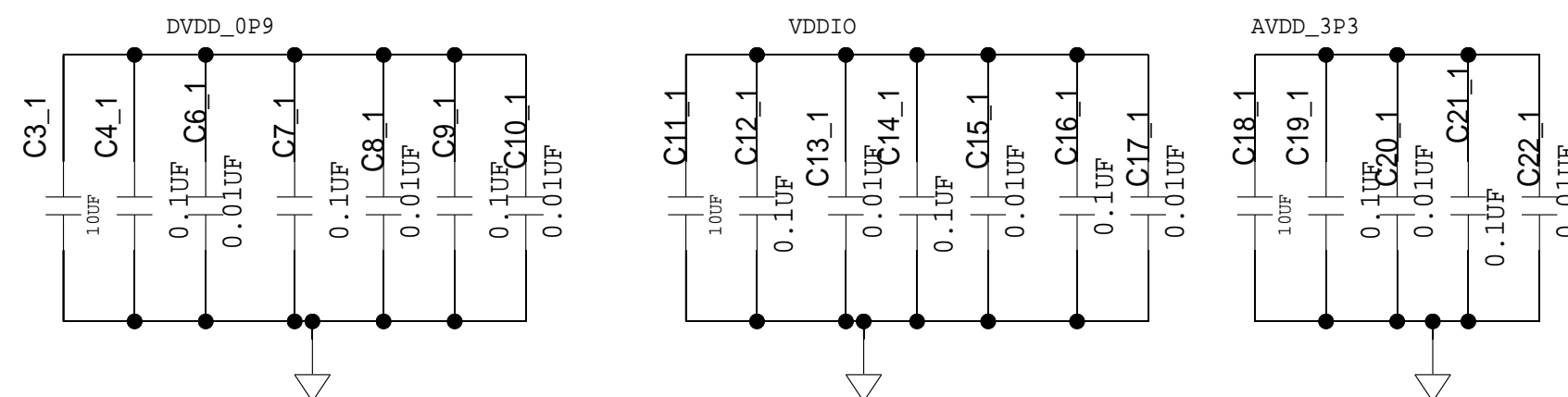


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- No length matching required between signals of different ports
- No length matching required between Tx & Rx groups
- Route All RGMII signals in Top layer . Keep routing lengths as small possible
- All clocks should be routed with 500nm char impedance

DECOUPLING CAPS:

0.1uF & 0.01uF caps per pin

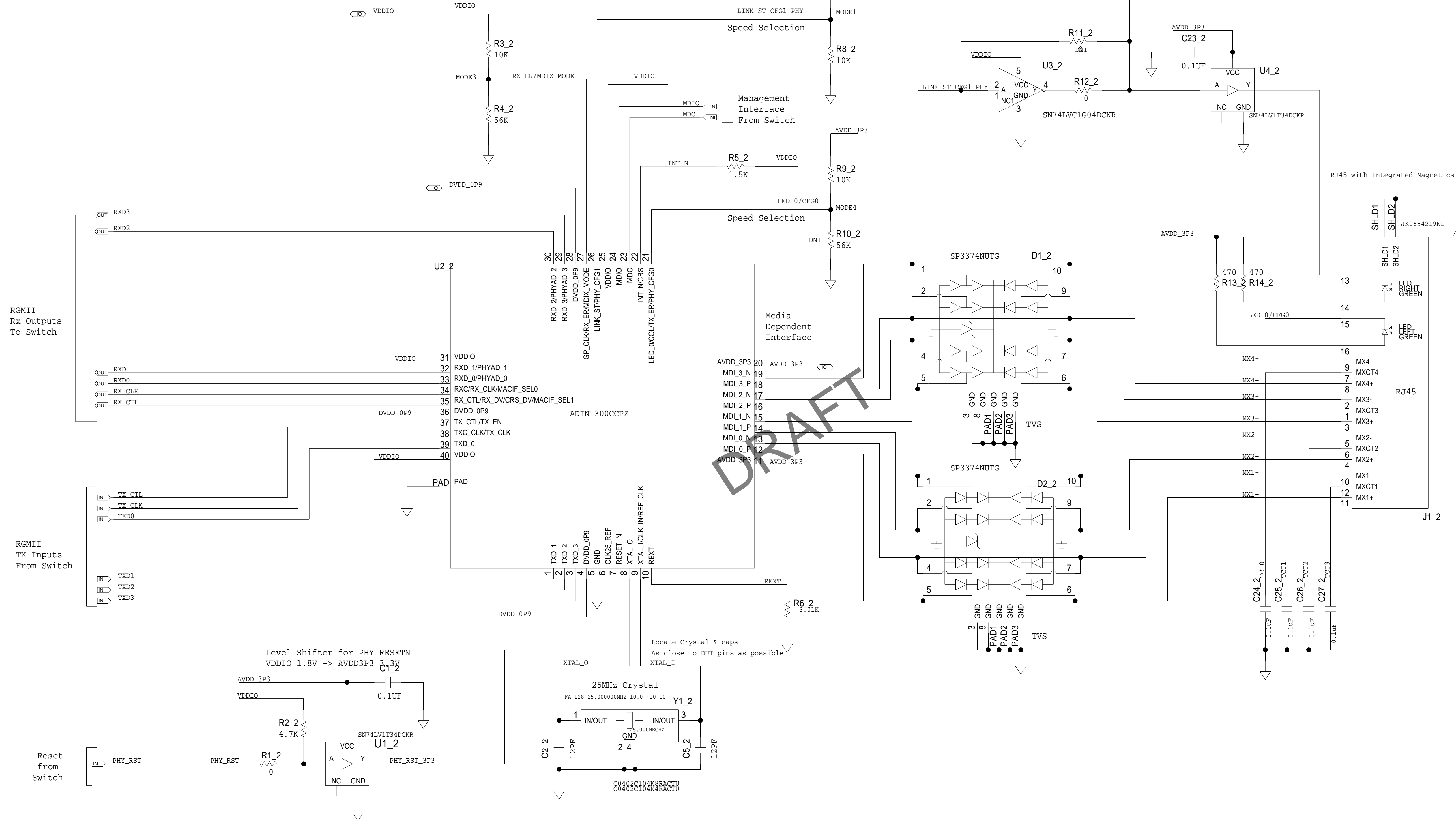


ANALOG DEVICES		SCHEMATIC			
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		DESIGN VIEW <DESIGN_VIEW>		REV B	
		PTD ENGINEER DEREK SAM		SIZE D	SCALE 1:1
		SHEET 7 OF 10			

Gb Ethernet PHY with ADIN1300

PHY Strapping:

MAC INTERFACE: RGMII with Tx & Rx DLL Enabled
MDI MODE SEL AutoMDI+ Pref MDI
SPEED CONFIG: 10/100 HD/FD + 1000 FD Slv

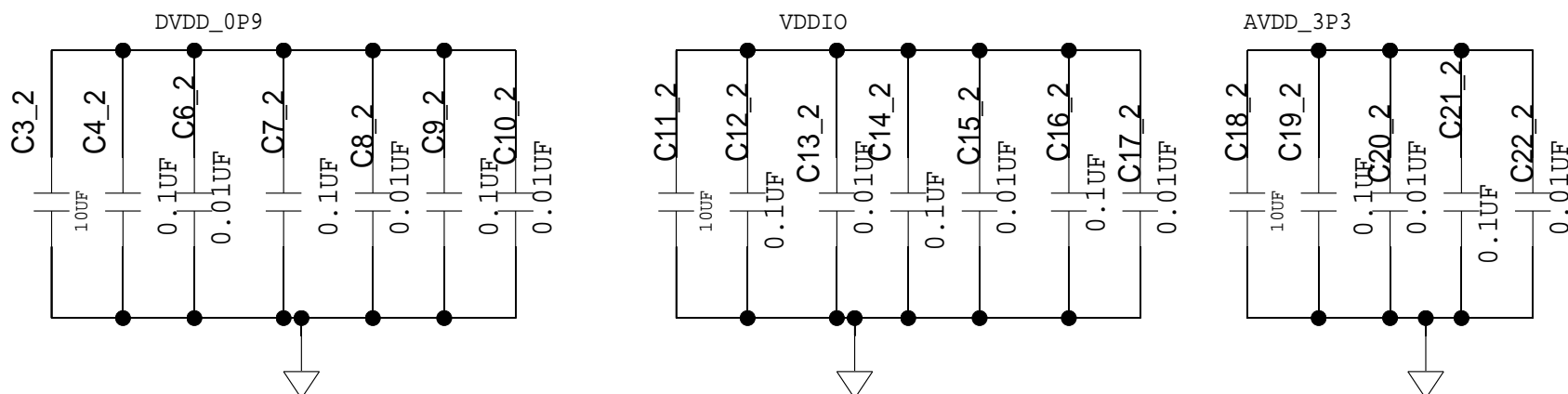


LAYOUT NOTES:

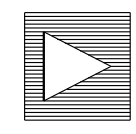
- 2.3.2. RGMII/RMII (125MHz)
- Plan components on RGMII ports 1 & 4 towards top edge and all others towards the bottom edge.
- Route P*_Tx/P*_Rx signals with 500ohm Char Impedance.
- All signals within Tx group (P*_TXCL, P*_TXD<0:3>, P*_TXCTL) should be length matched.
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- All clocks should be routed with 500ohm char impedance

DECOUPLING CAPS:

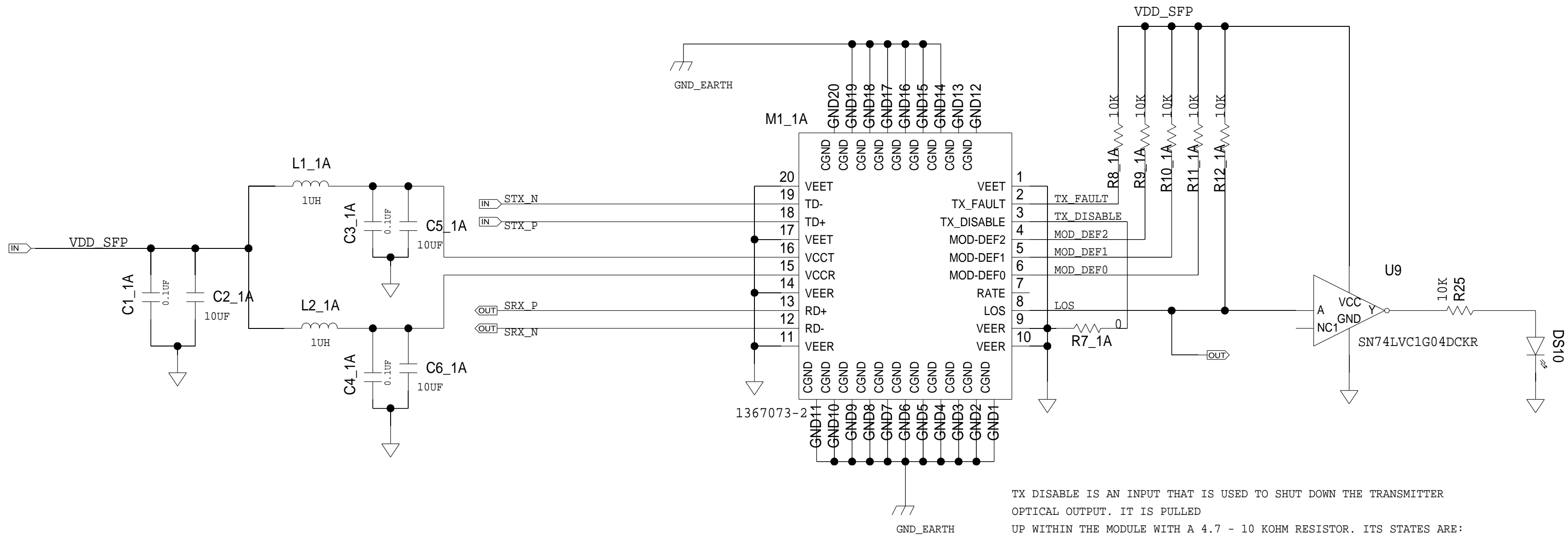
0.1uF & 0.01uF caps per pin



REVISIONS				
REV	DESCRIPTION	DATE	APPROVED	

 ANALOG DEVICES		SCHEMATIC		
		EVAL-ADIN3310EBZ Product(s): ADIN3310 <PRODUCT_1>		
DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02-068019		REV B
PTD ENGINEER DEREK SAM		SIZE D	SCALE 1:1	SHEET 8 OF 10

SFP

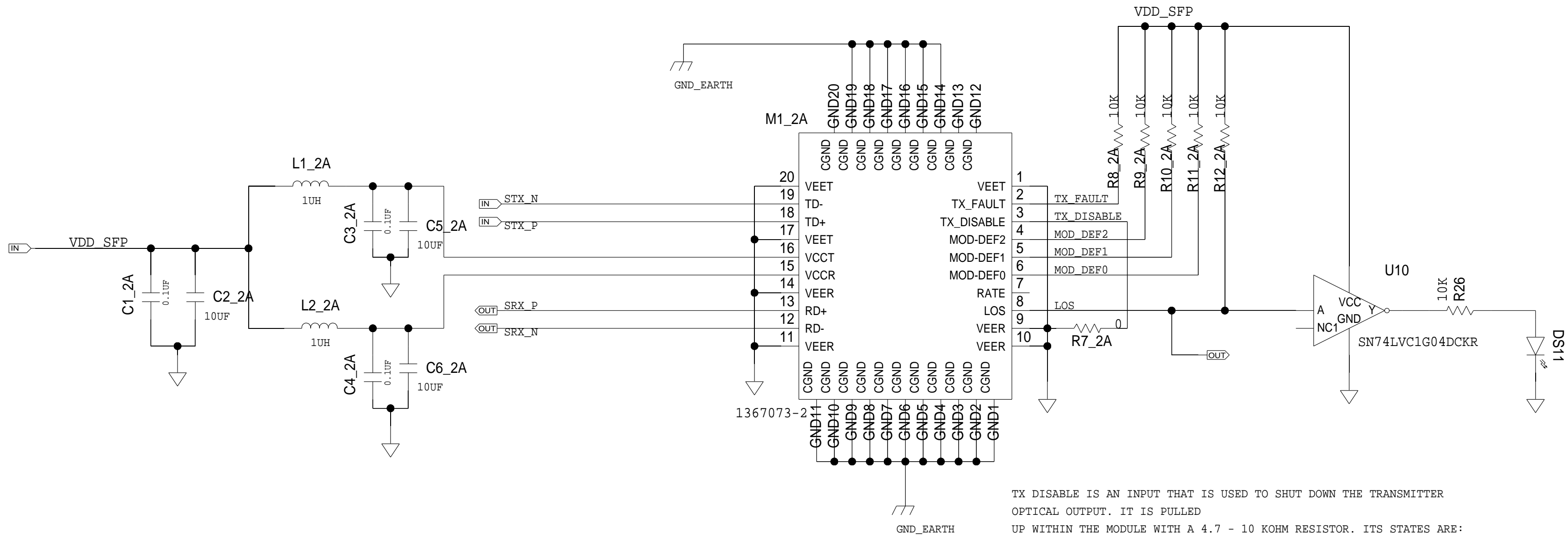


LAYOUT NOTES:

- SGMII (data rate: 1.25Gbps)
- 1.Route P*_STxP/N & P*_SRxP/N signals as 1000hm differential lines
 - 2.Top layer routing recommended
 - 3.Length matching within pair is required.
 - 4.Co-planar routing is recommended - stitch vias on ground shield on both sides of route
 - 5.Keep Routing lengths short . avoid stubs

	SCHEMATIC			
	EVAL-ADIN3310EBZ Product(s): ADIN3310 <PRODUCT_1>			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-068019		REV B
	PTD ENGINEER DEREK SAM	SIZE D	SCALE 1:1	SHEET 9 OF 10

SFP



LAYOUT NOTES:

- SGMII (data rate: 1.25Gbps)
- 1.Route P*_STxP/N & P*_SRxP/N signals as 1000hm differential lines
- 2.Top layer routing recommended
- 3.Length matching within pair is required.
- 4.Co-planar routing is recommended - stitch vias on ground shield on both sides of route
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	SCHEMATIC			
	EVAL-ADIN3310EBZ Product(s): ADIN3310 <PRODUCT_1>			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02-068019		REV B
	PTD ENGINEER DEREK SAM	SIZE D	SCALE 1:1	SHEET 10 OF 10