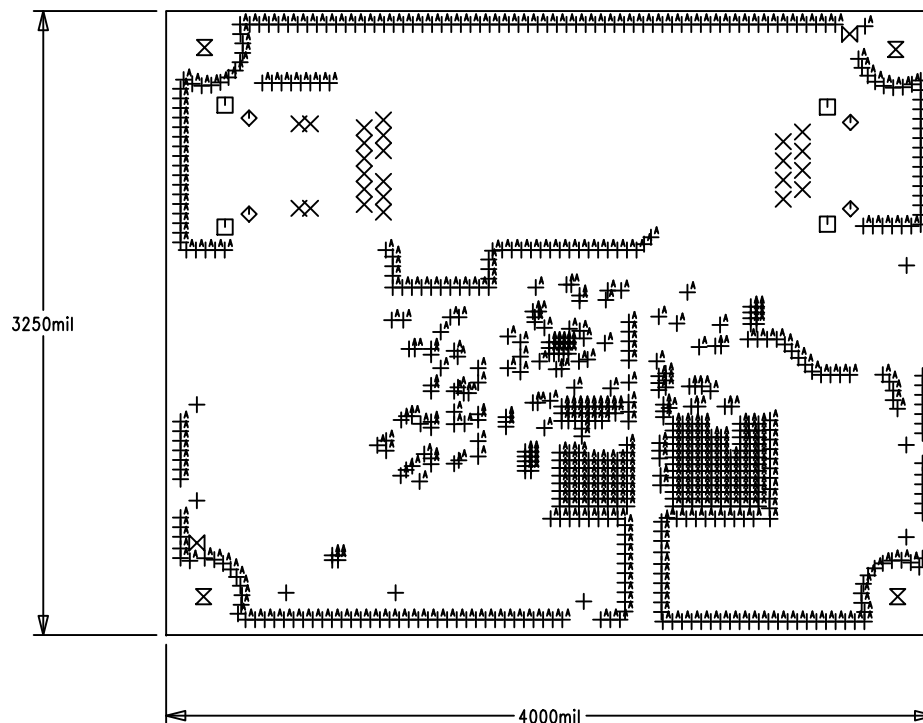


REVISION HISTORY				
ECO	REV	DESCRIPTION	APP. ENG.	DATE
-	2	PRODUCTION	KAUNG H.	2-23-16

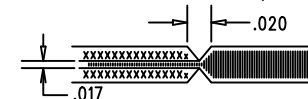
SHOWN FROM TOP SIDE



SIZE	QTY	SYM	PLATED	TOL
94	8	+	YES	+/-0.0
36	24	X	YES	+/-0.0
62	4	□	YES	+/-0.0
128	4	◇	NO	+/-0.0
188	4	⊗	YES	+/-0.0
70	2	⊗	NO	+/-0.0
10	711	+ <sup>A</sup>	YES	+/-0.0

## NOTES: UNLESS OTHERWISE SPECIFIED


- FAB PER IPC-A-600.
- MATERIAL: -LEAD FREE ASSEMBLY COMPLIANT, ISOLA FR-370HR OR EQUIVALENT.  
-FINISHED THICKNESS TO BE 0.062" +/- .005"  
-TOTAL OF 6 LAYERS WITH 2 OZ. CU ON THE OUTER LAYERS AND 1 OZ. CU ON THE INNER LAYERS.  
-FLAMMABILITY RATING: 94 V-0 MINIMUM.
- SIZE: CUT TO DIMENSIONS AND TOLERANCES SHOWN.  
0.00" ARE PRIMARY DATUMS.
- DRILLING: -DRILL HOLES PER SCHEDULE. PLATE THROUGH HOLES WITH COPPER, 0.001" THICK MIN.  
-ALL HOLE SIZES ARE SPECIFIED AFTER PLATING.  
-HOLE LOCATION TOLERANCES ARE +/-0.003" IN RELATION TO CENTER
- FINISH: -SMOBC USING LPI BOTH SIDES, COLOR GREEN.  
-GOLD IMMERSION BOTH SIDES.  
-FOR SILKSCREENS: USE WHITE NON-CONDUCTIVE INK.
- DO NOT ALTER ARTWORK e.g. TO ADD LOGO OR DATE CODE.  
PAD SIZE CAN BE MODIFIED TO MEET END FINISH.
- PCBS ARE TO BE RoHS COMPLIANT.
- SCORING FOR PANELIZED PCB (PRODUCTION FAB ONLY):



9. CONTROLLED DIELECTRIC FOR ALL LAYERS

### LAYER STRUCTURE

.0027"	L1-TOP
.009" +/- 10%"	
.00135"	L2-GND1
.014" +/- 10%"	
.00135"	L3-SIGNAL1
.062" FINISHED 6 LAYERS .009" +/- 10%"	
.00135"	L4-SIGNAL2
.014" +/- 10%"	
.00135"	L5-GND2
.009" +/- 10%"	
.0027"	L6-BOTTOM

UNLESS OTHERWISE SPECIFIED		APPROVALS				1630 MCCARTHY BLVD MILPITAS, CA 95035 PH: (408)432-1900 www.linear.com LTC CONFIDENTIAL- FOR CUSTOMER USE ONLY	
DIMENSIONS ARE IN INCHES TOLERANCES: 0.XX" = ±0.01" 0.XXX" = ±0.005" INTERPRET DIM AND TOL PER ASME Y14.5M-1994 THIRD ANGLE PROJECTION		PCB DES. KAUNG H.				TITLE: FABRICATION DRAWING HIGH EFFICIENCY IEEE 802.3bt PD WITH PoE IDEAL DIODE BRIDGE	
		APP ENG. KAUNG H.		SIZE IC NO. LT4295IUF			
				N/A DEMO CIRCUIT 2475A		2	
		SCALE = NONE		FILENAME: DC2475A-1.PCB		SHT 1 OF 1	