HMC8327LG

v08.0718

E-BAND LOW NOISE DOWNCONVERTER SiP 81 - 86 GHz

Typical Applications

The HMC8327LG is ideal for:

- E-Band Communication Systems
- High Capacity Wireless Backhaul
- Test & Measurement

Features

Conversion Gain: 8.5 dB typical

Image Rejection: 20 dBc typical

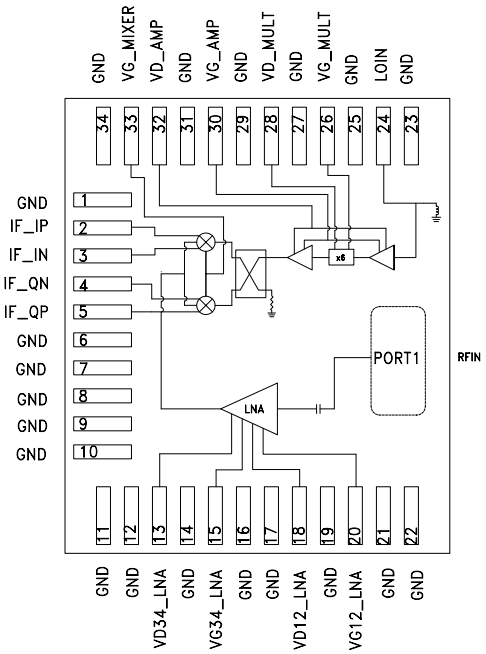
Noise Figure: 6 dB typical

Input Third-Order Intercept (IP3): 2 dBm typical

Input Power for P1dB Compression: -7 dBm typical

Fully Integrated In Surface Mount 34 Lead 13 mm x 11 mm Package

Functional Diagram



General Description

The HMC8327LG is a fully integrated System In Package (SiP) in-phase/quadrature (I/Q) downconverter that operates between an RF input frequency range of 81 GHz to 86 GHz and an IF output frequency range of DC to 2 GHz. This device provides a small signal conversion gain of 8 to 13 dB with 20 dBc of image rejection. The HMC8327LG utilizes a low noise amplifier followed by an image rejection mixer which is driven by a 6x LO multiplier. Differential I and Q mixer outputs are provided for direct conversion applications. Alternatively, the outputs can be combined using an external 90° hybrid and two external 180° hybrids for single-ended applications.

Electrical Specifications, T_A = -40°C to +85°C, IF = 1000 MHz, LO = 4 dBm, VD12_LNA = 2 V, VD34_LNA = 4 V, VD_AMP = 4 V, VD_MULT = 1.5 V, VG_MIXER = -1 V [1]

Parameter	Min.	Typ. (25°C)	Max.	Units
RF Frequency Range	81		86	GHz
LO Frequency Range	13.2		14.6	GHz
IF Frequency Range	0		2	GHz
LO Input Level Range	0		8	dBm
Gain Flatness		2	5	dB
Conversion Gain	6	8.5	17	dB
Image Rejection	15	20		dBc
Input Power for 1 dB Compression (P1dB)	-13	-7		dBm
Input Third-Order Intercept (IP3)	-6	2		dBm
Input Second-Order Intercept (IP2)	15	30		dBm
6x LO Leakage at the RF Input Port (RFIN)		-55	-50	dBm
I/Q Phase Balance [2]			15	degrees
I/Q Amplitude Balance [2]		0.5	3	dB
Noise Figure		6	8	dB

[1] Measurements performed as downconverter with upper sideband selected and two external 180° hybrids followed by one external 90° hybrid at the IF ports, unless otherwise noted.
[2] Measurements performed without external hybrids.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Electrical Specifications, T_A = -40°C to +85°C, IF = 1000 MHz, LO = 4 dBm, VD12_LNA = 2 V, VD34_LNA = 4 V, VD_AMP = 4 V, VD_MULT = 1.5 V, VG_MIXER = -1 V [1]

Parameter	Min.	Typ. (25°C)	Max.	Units
RF Port Return Loss	8	10		dB
DC Power Dissipation		1.0	1.25	W
Input Waveguide port		WR-12		
Baseband Output Port Impedance (differential)		100		Ohm
Baseband Output Port Return Loss [2]	8	10		dB
LO Input Port Impedance		50		Ohm
LO Input Port Return Loss	8	10		dB
VG for the LNA (VG12_LNA, VG34_LNA)	-2		0	V
VD for the LNA (VD34_LNA)	3.8	4	4.2	V
VD for the LNA (VD12_LNA)	1.9	2	2.1	V
VD for the Multiplier (VD_MULT)	1.42	1.5	1.58	V
VG for the Multiplier (VG_MULT)	-2		0	V
VG for the Mixer (VG_MIXER)	-2		0	V
Supply Current (ID12_LNA + ID34_LNA) [3]		66		mA
Supply Current (ID _AMP) [4]		175		mA
Supply Current (ID_MULT) [5]		80		mA

[1] Measurements performed as downconverter with upper sideband selected and two external 180° hybrids followed by one external 90° hybrid at the IF ports, unless otherwise noted.
[2] Measurements performed without external hybrids.
[3] Adjust VG12_LNA between -2 V and 0 V to achieve typical quiescent current ID12_LNA = 22 mA. Adjust VG34_LNA between -2 V and 0 V to achieve typical quiescent current ID34_LNA = 44 mA.
[4] Adjust VG_AMP between -2 V and 0 V to achieve typical quiescent current (ID_AMP) = 175 mA.
[5] Adjust VG_MULT between -2 V and 0 V to achieve typical current (ID_MULT) = 80 mA under RF drive.

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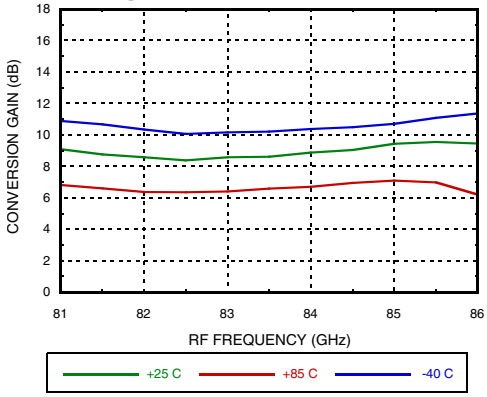
Upper Sideband Selected, IF = 1000 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Conversion Gain vs. RF Frequency over Temperature



Conversion Gain vs. RF Frequency over LO Power

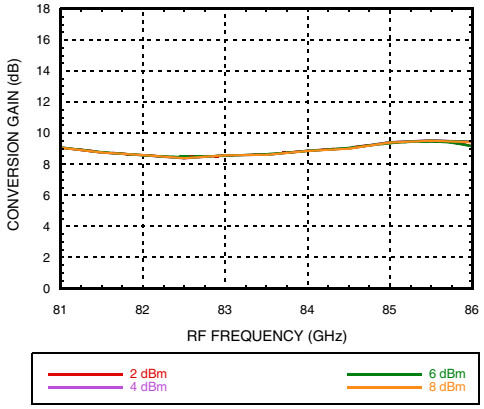


Image Rejection vs. RF Frequency over Temperature

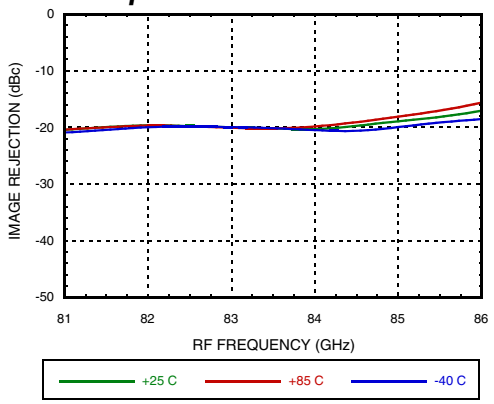
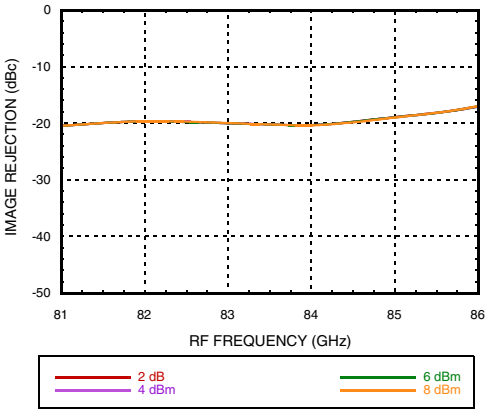
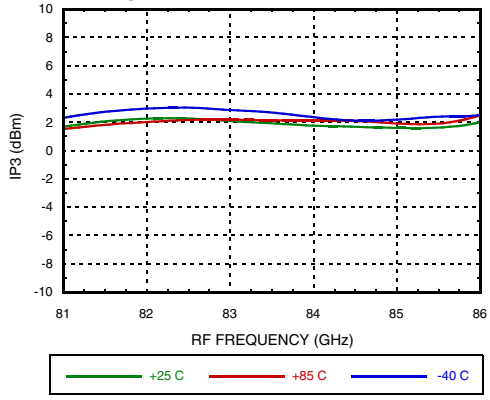


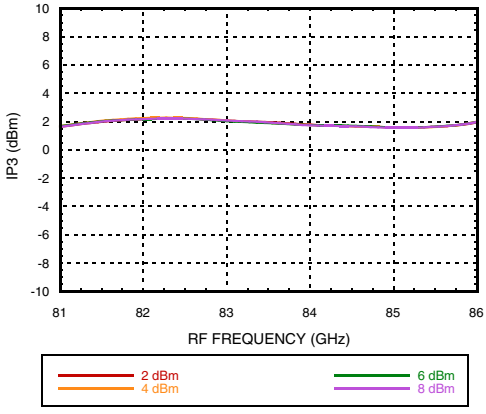
Image Rejection vs. RF Frequency over LO Power



Input IP3 vs. RF Frequency over Temperature

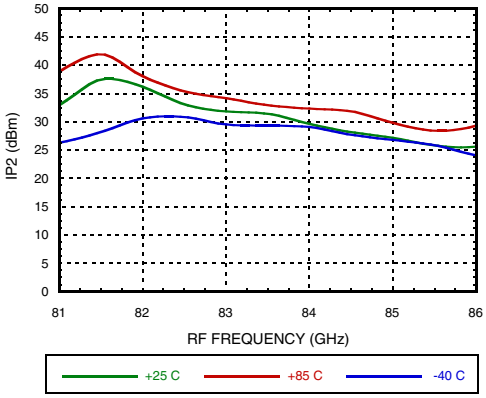


Input IP3 vs. RF Frequency over LO Power

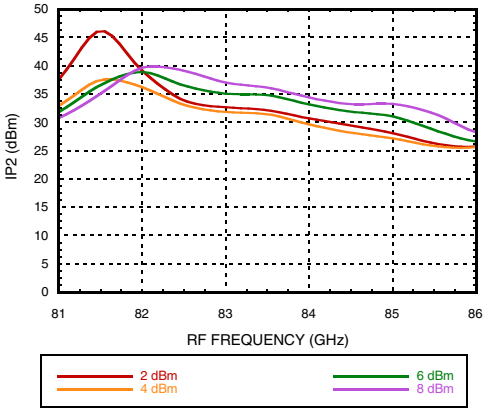


Upper Sideband Selected, IF = 1000 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

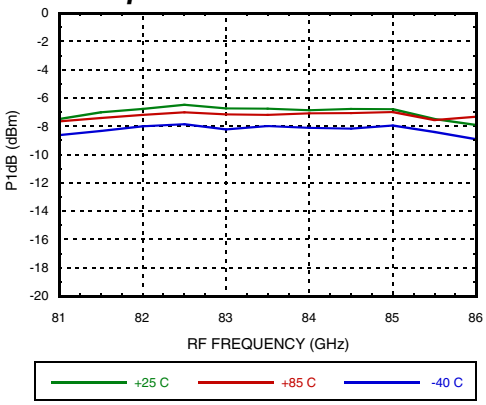
Input IP2 vs. RF Frequency over Temperature



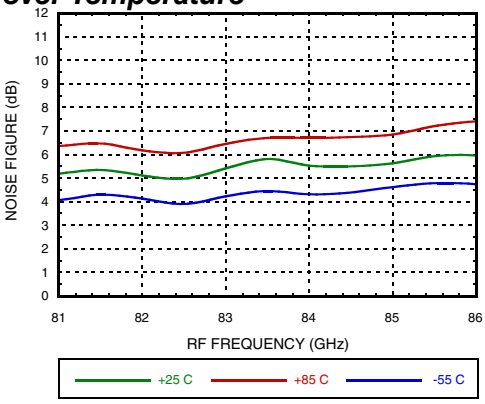
Input IP2 vs. RF Frequency over LO Power



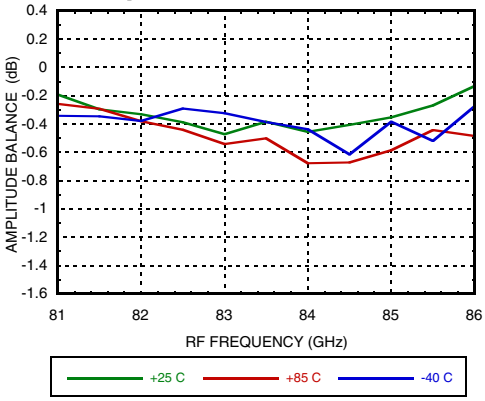
Input P1dB vs. RF Frequency over Temperature



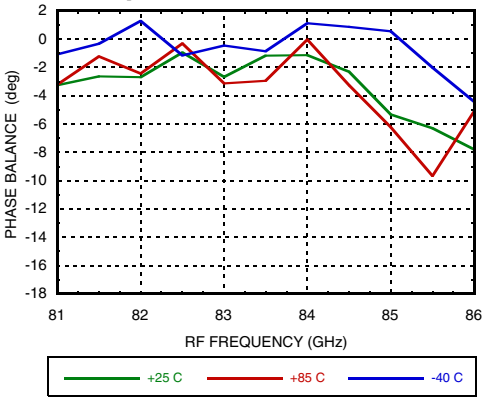
Noise Figure vs. RF Frequency over Temperature



Amplitude Balance vs. RF Frequency over Temperature



Phase Balance vs. RF Frequency over Temperature



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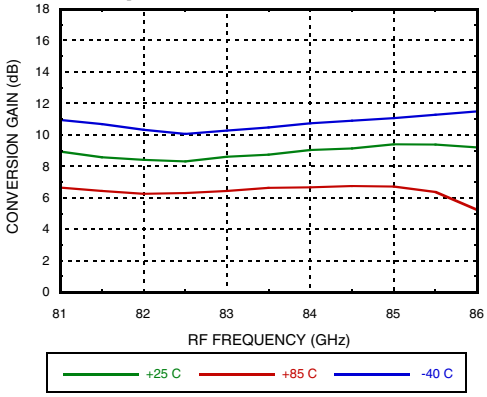
Lower Sideband Selected, IF = 1000 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Conversion Gain vs. RF Frequency over Temperature



Conversion Gain vs. RF Frequency over LO Power

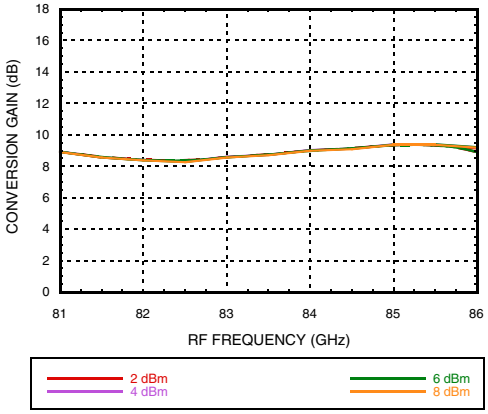


Image Rejection vs. RF Frequency over Temperature

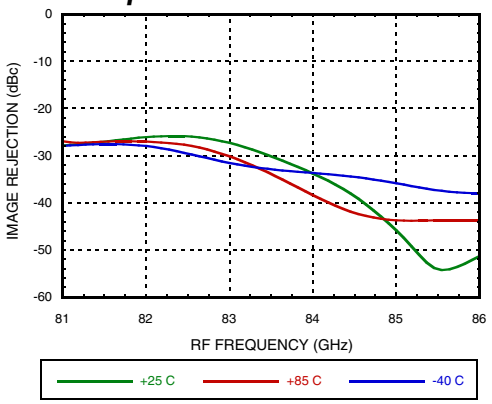
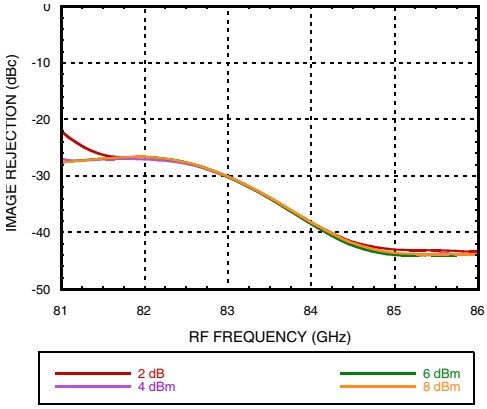
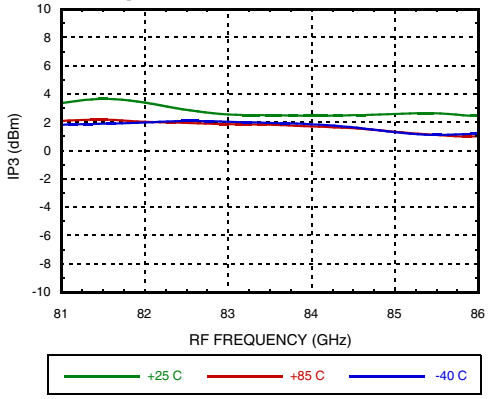


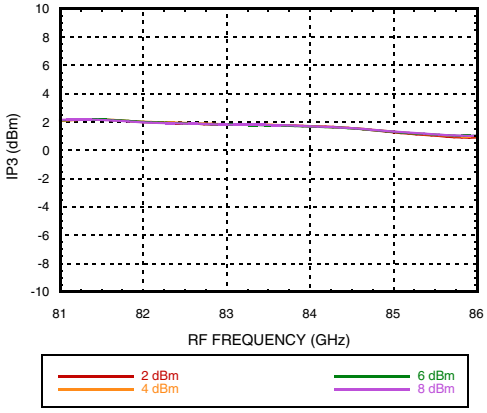
Image Rejection vs. RF Frequency over LO Power



Input IP3 vs. RF Frequency over Temperature

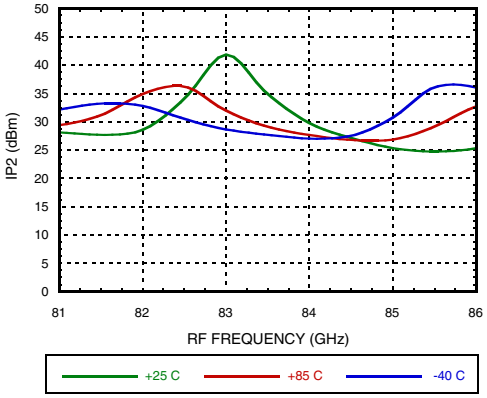


Input IP3 vs. RF Frequency over LO Power

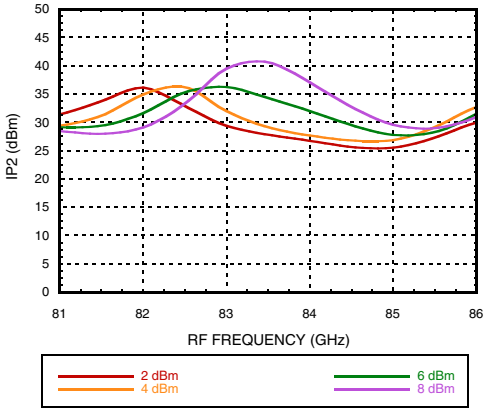


Lower Sideband Selected, IF = 1000 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

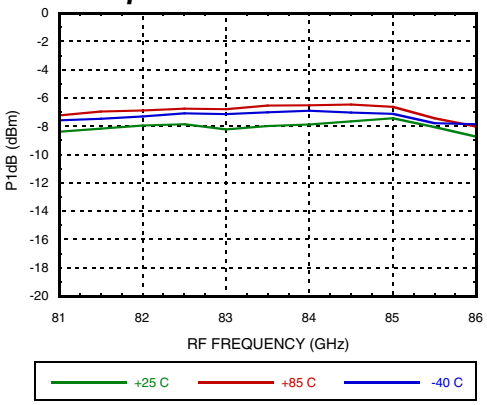
Input IP2 vs. RF Frequency over Temperature



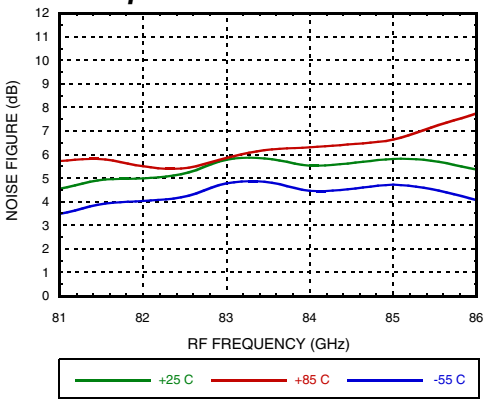
Input IP2 vs. RF Frequency over LO Power



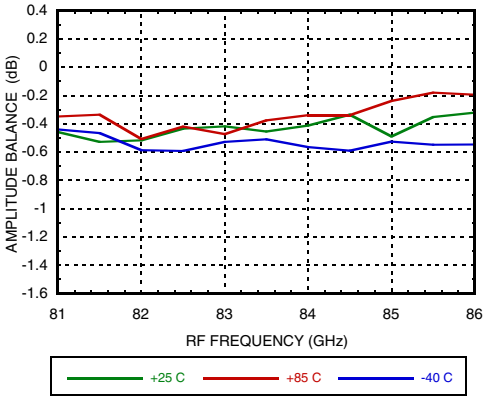
Input P1dB vs. RF Frequency over Temperature



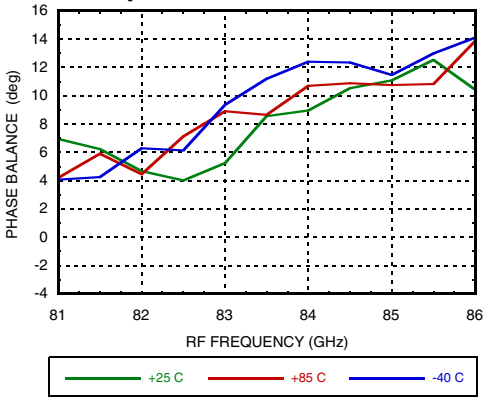
Noise Figure vs. RF Frequency over Temperature



Amplitude Balance vs. RF Frequency over Temperature

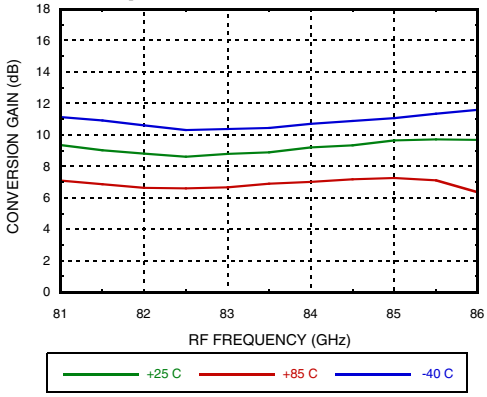


Phase Balance vs. RF Frequency over Temperature



Upper Sideband Selected, IF = 100 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Conversion Gain vs. RF Frequency over Temperature



Noise Figure vs. RF Frequency over Temperature

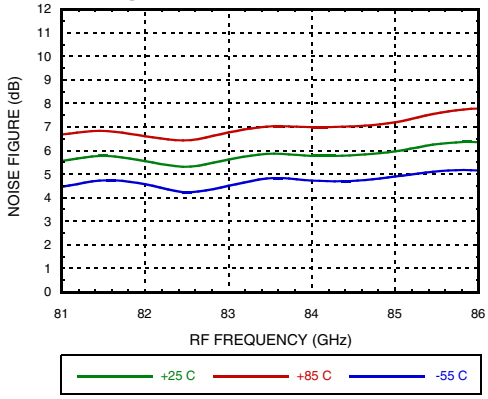
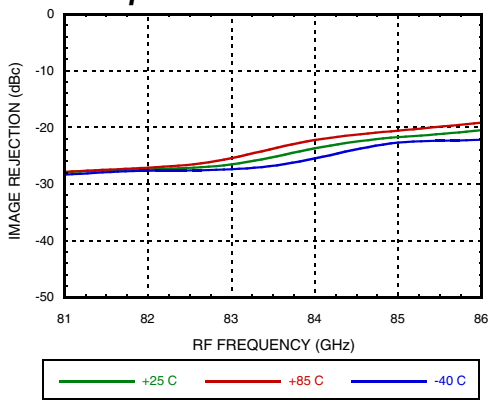
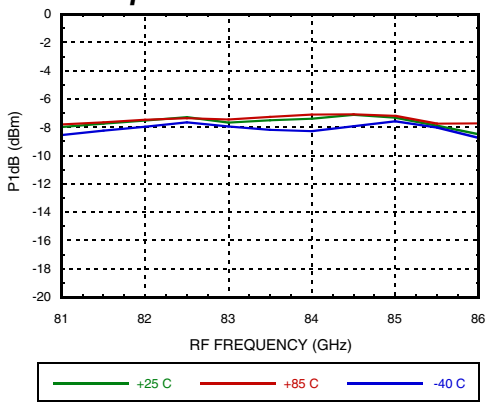


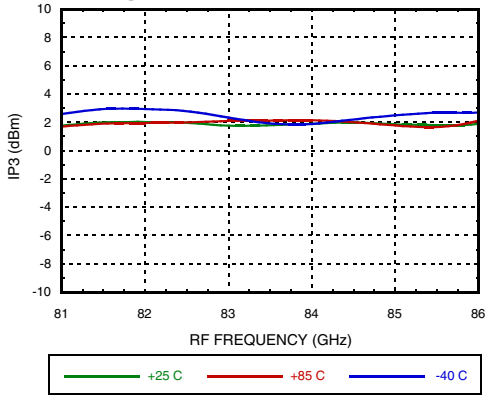
Image Rejection vs. RF Frequency over Temperature



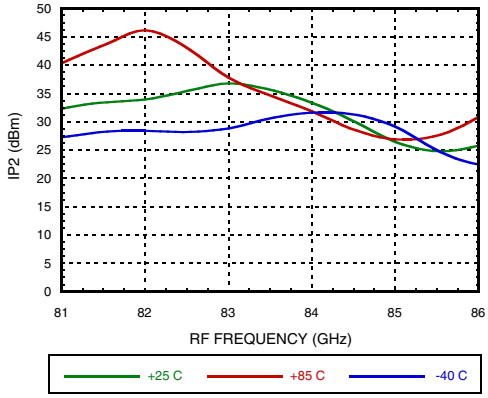
Input P1dB vs. RF Frequency over Temperature



Input IP3 vs. RF Frequency over Temperature

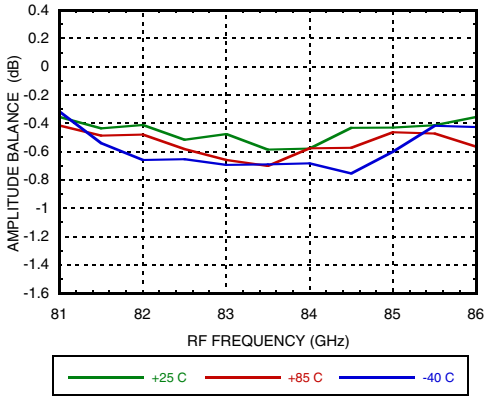


Input IP2 vs. RF Frequency over Temperature

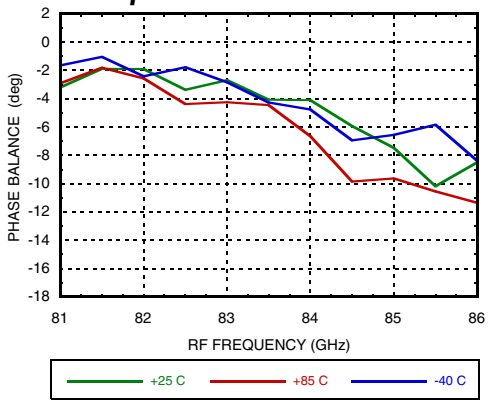


Upper Sideband Selected, IF = 100 MHz, RFIN = -20 dBm per Tone per Tone, LO = 4 dBm, Unless otherwise Noted

Amplitude Balance vs. RF Frequency over Temperature

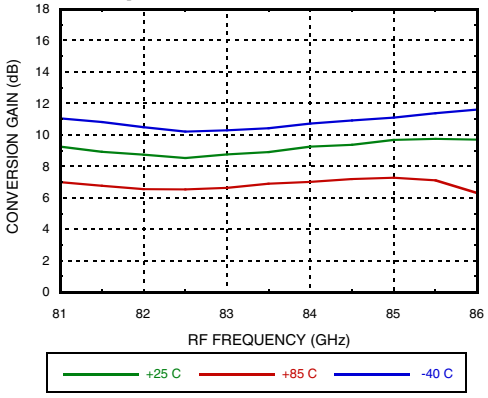


Phase Balance vs. RF Frequency over Temperature



Lower Sideband Selected, IF = 100 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Conversion Gain vs. RF Frequency over Temperature



Noise Figure vs. RF Frequency over Temperature

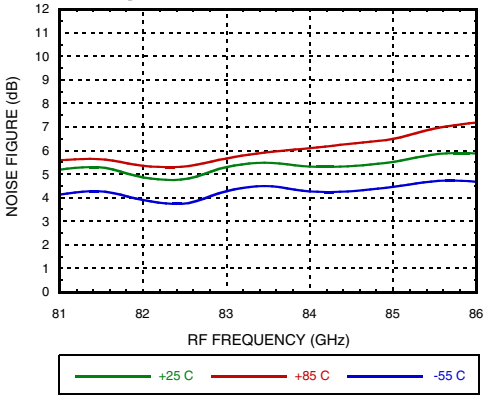
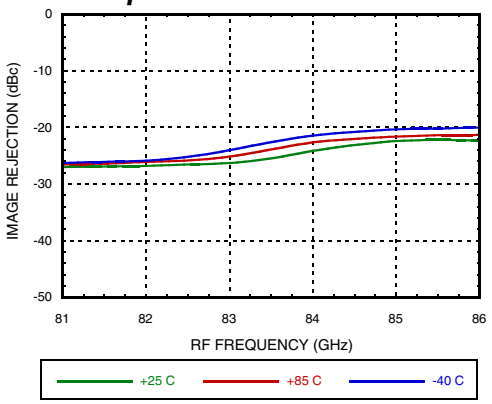
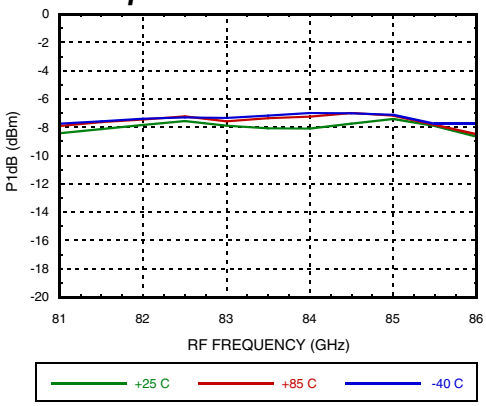


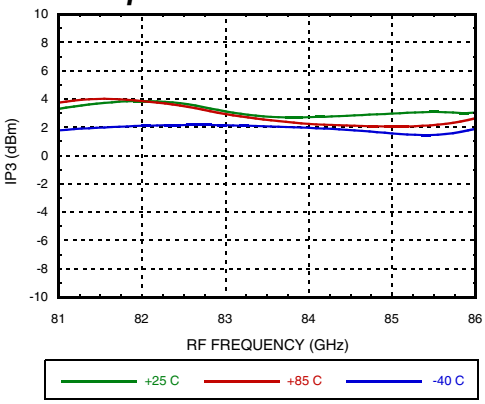
Image Rejection vs. RF Frequency over Temperature



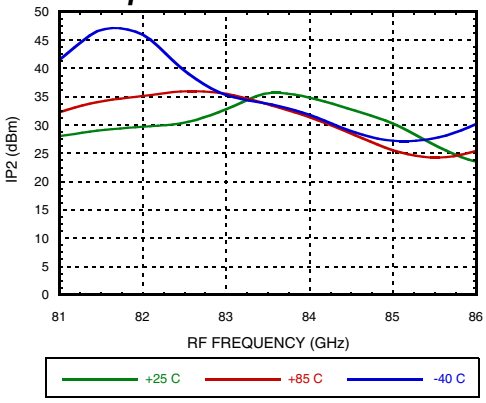
Input P1dB vs. RF Frequency over Temperature



Input IP3 vs. RF Frequency over Temperature

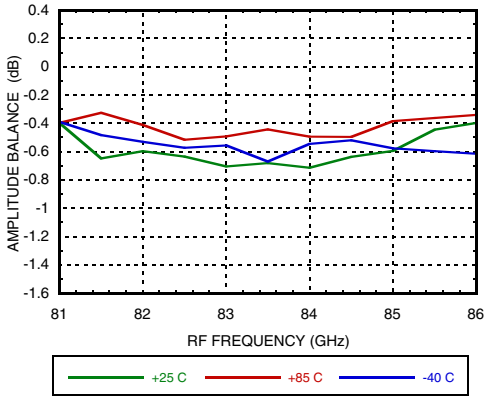


Input IP2 vs. RF Frequency over Temperature

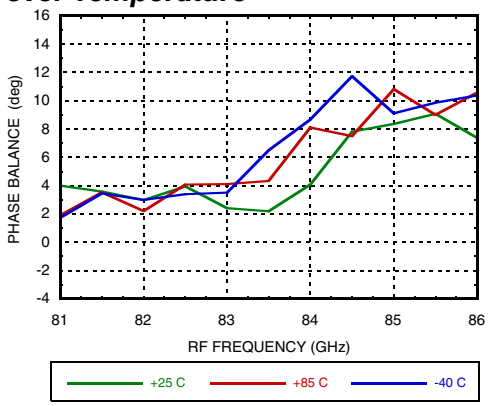


Lower Sideband Selected, IF = 100 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Amplitude Balance vs. RF Frequency over Temperature

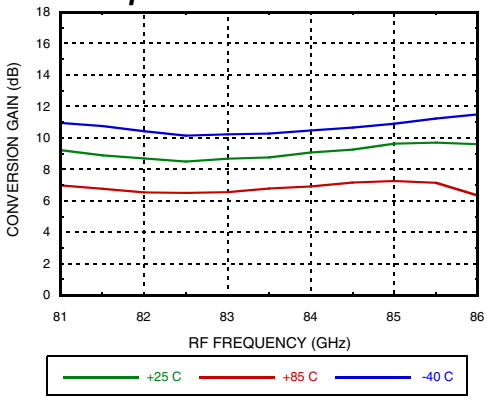


Phase Balance vs. RF Frequency over Temperature



Upper Sideband Selected, IF = 500 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Conversion Gain vs. RF Frequency over Temperature



Noise Figure vs. RF Frequency over Temperature

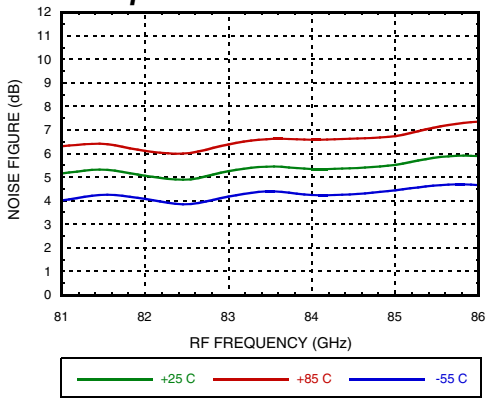
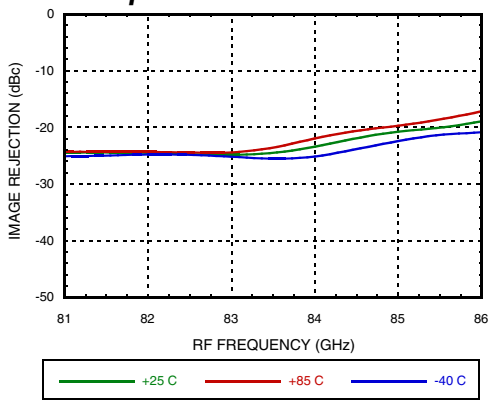
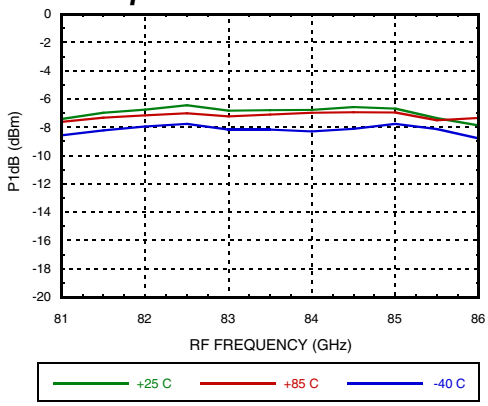


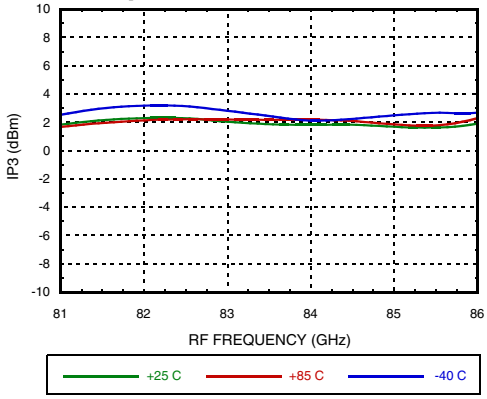
Image Rejection vs. RF Frequency over Temperature



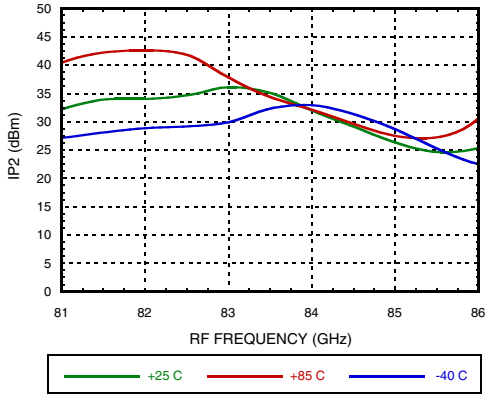
Input P1dB vs. RF Frequency over Temperature



Input IP3 vs. RF Frequency over Temperature

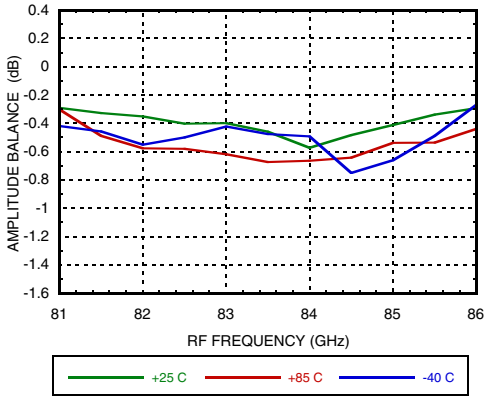


Input IP2 vs. RF Frequency over Temperature

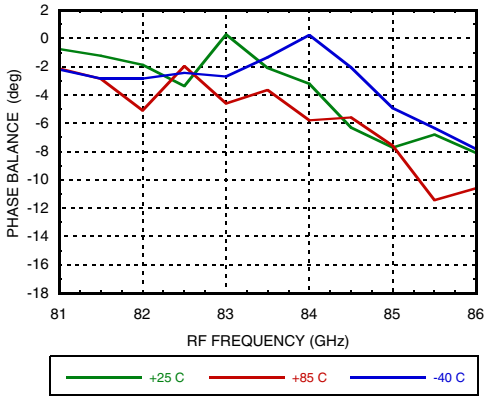


Upper Sideband Selected, IF = 500 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Amplitude Balance vs. RF Frequency over Temperature

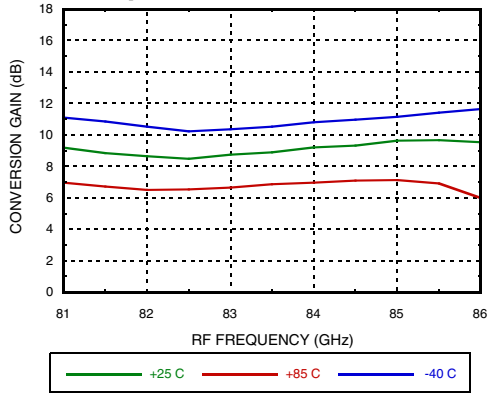


Phase Balance vs. RF Frequency over Temperature



Lower Sideband Selected, IF = 500 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Conversion Gain vs. RF Frequency over Temperature



Noise Figure vs. RF Frequency over Temperature

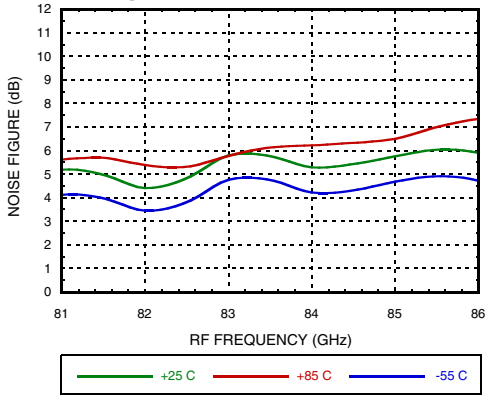
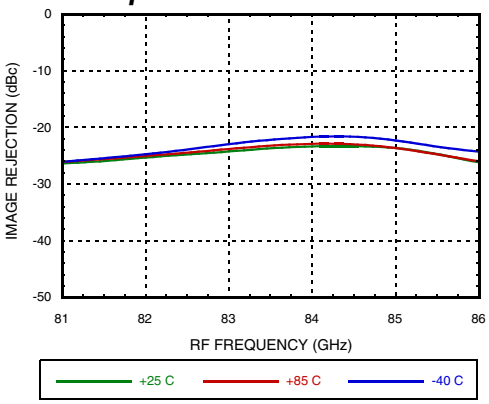
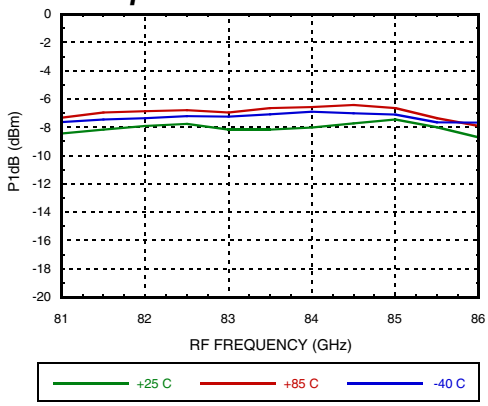


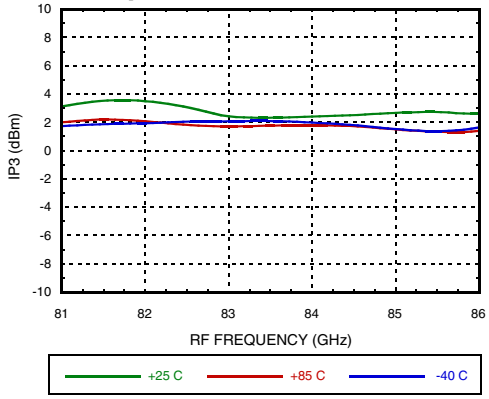
Image Rejection vs. RF Frequency over Temperature



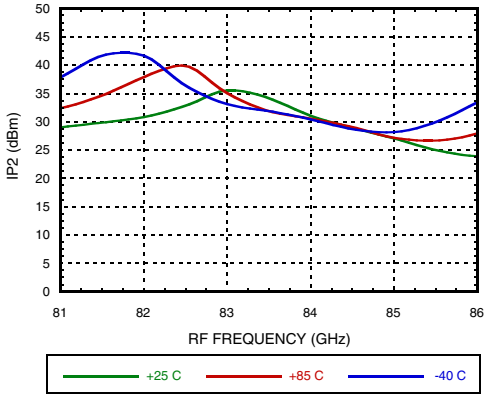
Input P1dB vs. RF Frequency over Temperature



Input IP3 vs. RF Frequency over Temperature



Input IP2 vs. RF Frequency over Temperature



For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
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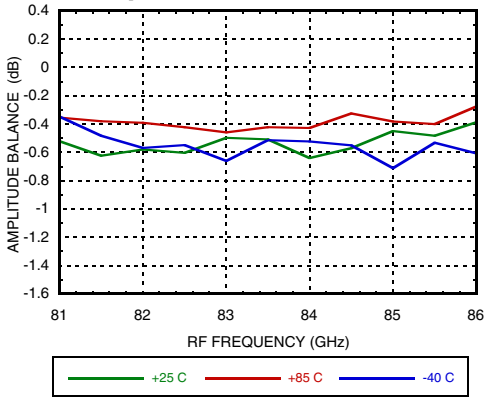
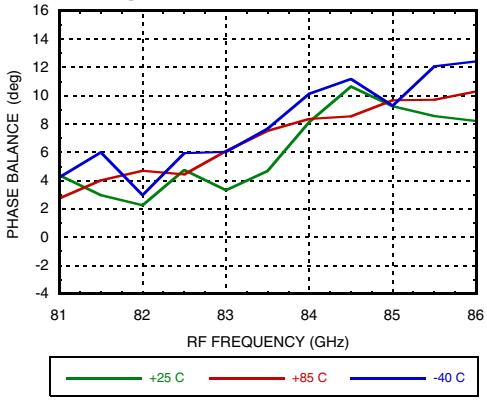
Lower Sideband Selected, IF = 500 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Amplitude Balance vs. RF Frequency over Temperature

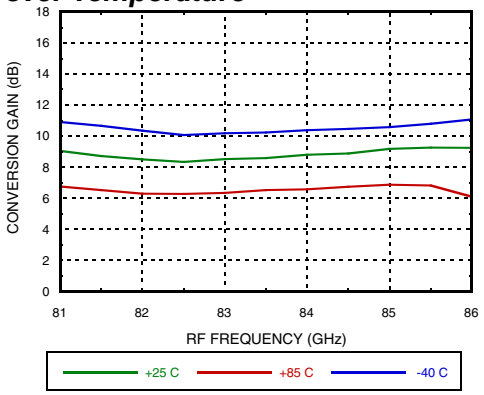


Phase Balance vs. RF Frequency over Temperature



Upper Sideband Selected, IF = 2000 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Conversion Gain vs. RF Frequency over Temperature



Noise Figure vs. RF Frequency over Temperature

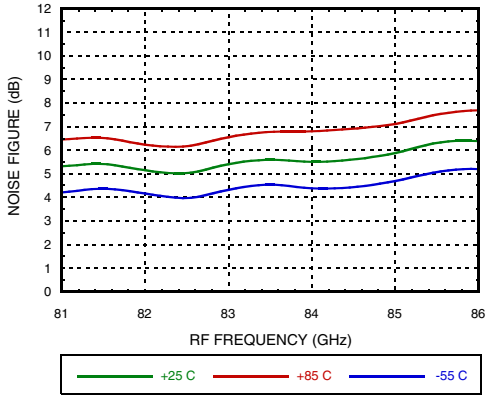
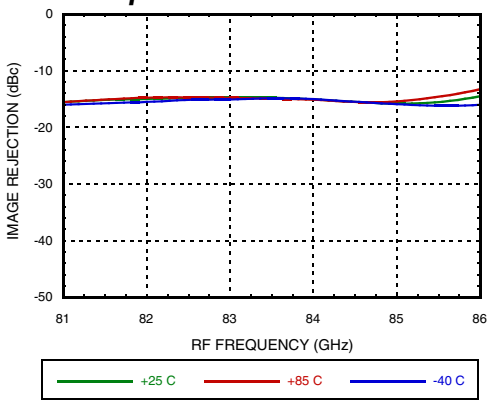
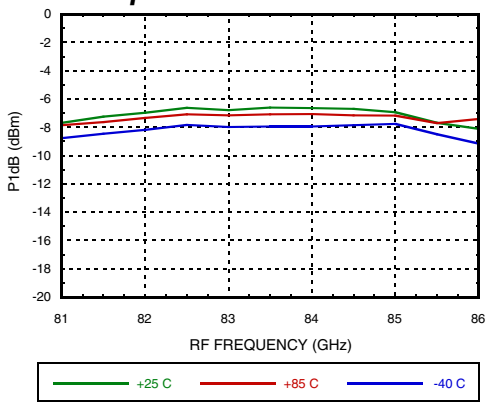


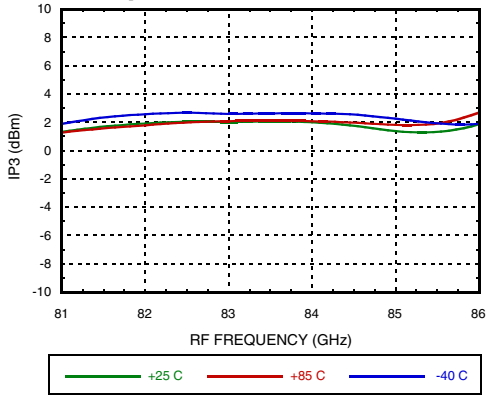
Image Rejection vs. RF Frequency over Temperature



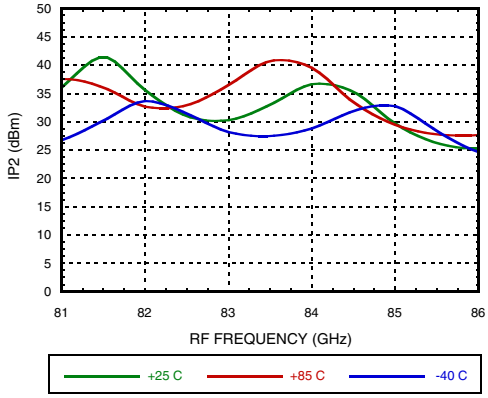
Input P1dB vs. RF Frequency over Temperature



Input IP3 vs. RF Frequency over Temperature

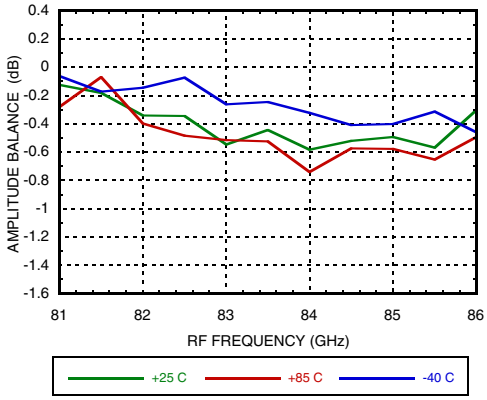


Input IP2 vs. RF Frequency over Temperature

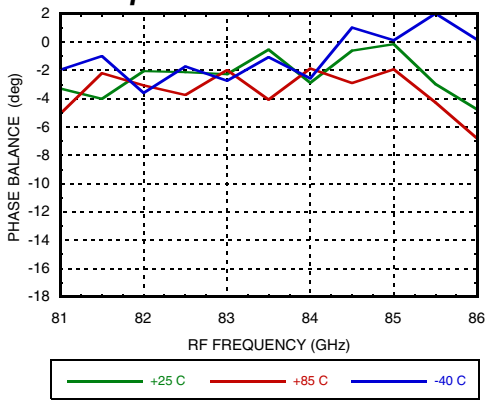


Upper Sideband Selected, IF = 2000 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Amplitude Balance vs. RF Frequency over Temperature



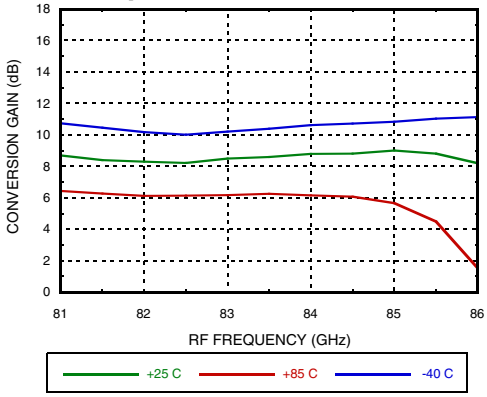
Phase Balance vs. RF Frequency over Temperature



E-BAND LOW NOISE DOWNCONVERTER SiP 81 - 86 GHz

Lower Sideband Selected, IF = 2000 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Conversion Gain vs. RF Frequency over Temperature



Noise Figure vs. RF Frequency over Temperature

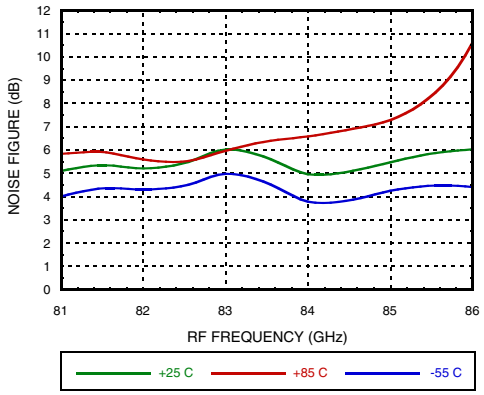
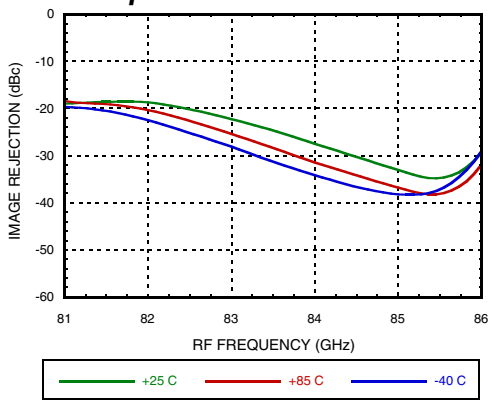
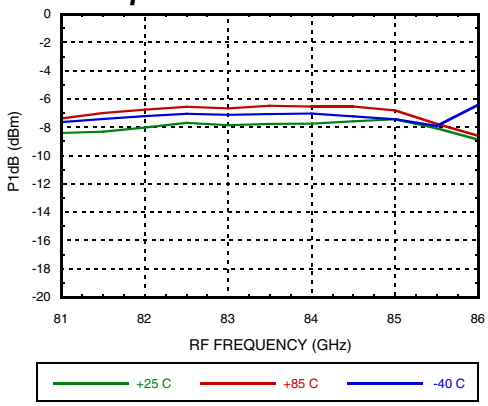


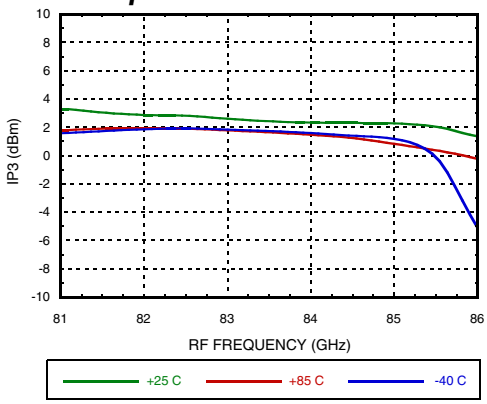
Image Rejection vs. RF Frequency over Temperature



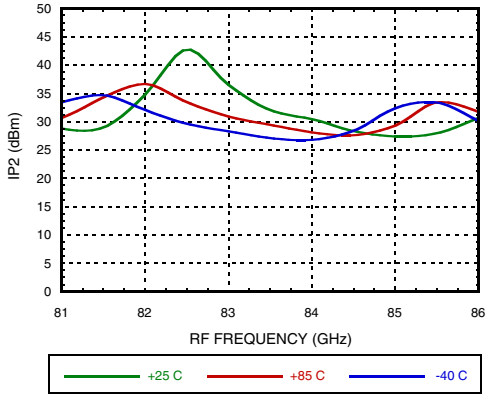
Input P1dB vs. RF Frequency over Temperature



Input IP3 vs. RF Frequency over Temperature

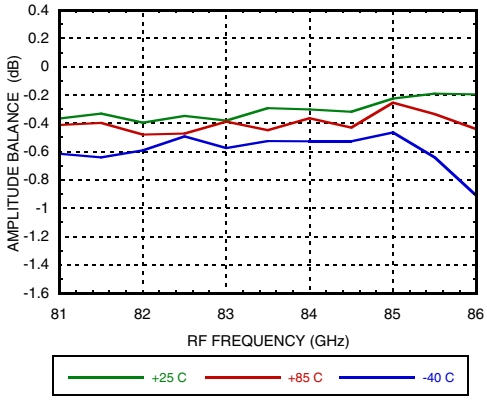


Input IP2 vs. RF Frequency over Temperature

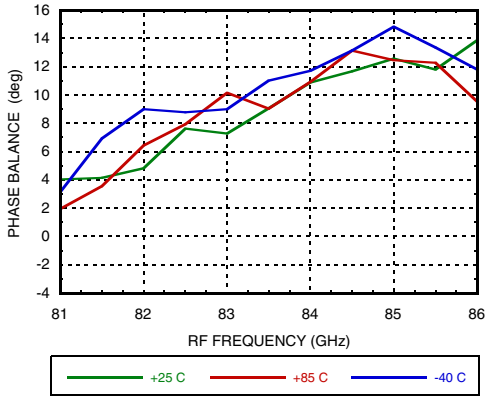


Lower Sideband Selected, IF = 2000 MHz, RFIN = -20 dBm per Tone, LO = 4 dBm, Unless otherwise Noted

Amplitude Balance vs. RF Frequency over Temperature

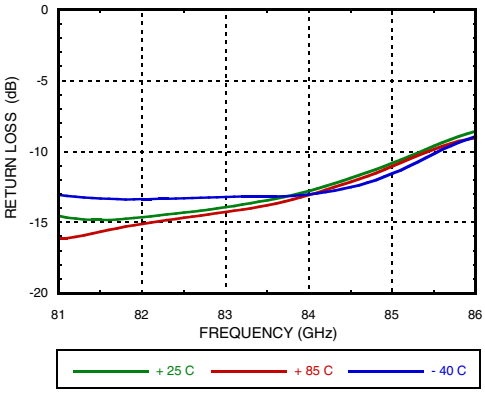


Phase Balance vs. RF Frequency over Temperature

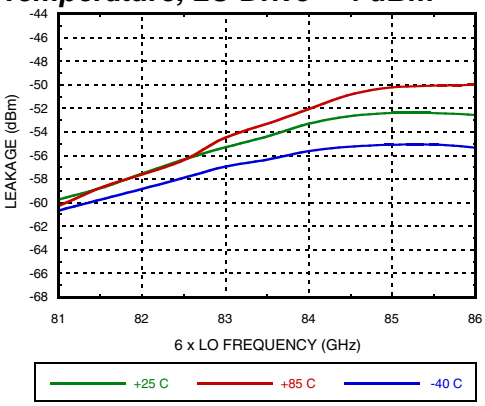


Return Loss Measured on Evaluation PCB and 6 x LO Leakage at RF Port

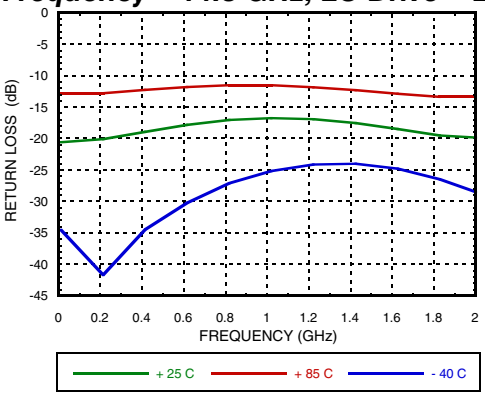
RF Return Loss over Temperature



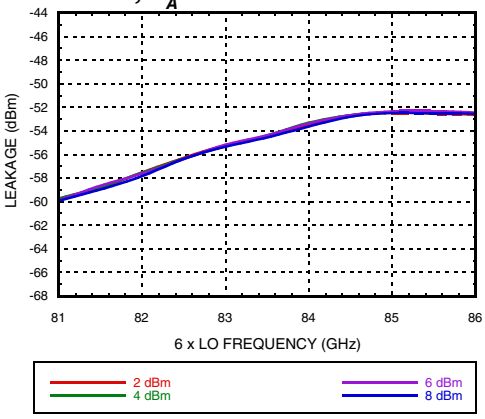
6 x LO Leakage at RF Ports over Temperature, LO Drive = 4 dBm



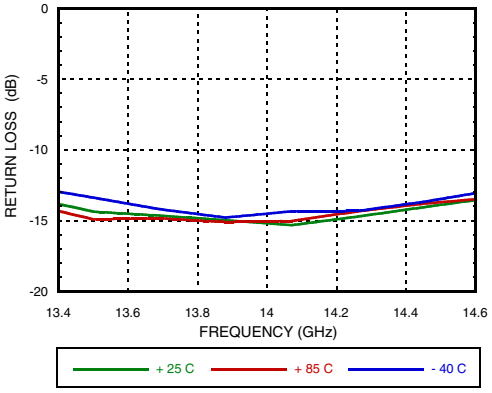
IF Return Loss over Temperature, LO Frequency = 14.3 GHz, LO Drive = 2dBm



6 x LO Leakage at RF Ports over LO Power, T_A = 25 °C



LO Return Loss over Temperature



Spurious Performance, Lower Sideband Selected

T_A = 25°C, IF = 1 GHz, RFIN = -20 dBm , LO = 4 dBm. Mixer spurious products are measured in dBc from the IF output power level single-ended for frequencies below 50 GHz, with all other IF ports terminated. Spur values are (M × IF) + (N × LO). N/A means not applicable.

RF = 81 GHz, LO = 13.667 GHz

	nLO							
mIF	0	1	2	3	4	5	6	7
-5	N/A	<-65	<-65	<-65	-61	N/A	N/A	N/A
-4	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-3	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-2	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-1	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
0	N/A	-23	<-65	<-65	N/A	N/A	N/A	N/A
1	0	<-65	<-65	<-65	N/A	N/A	N/A	N/A
2	-36	<-65	<-65	<-65	N/A	N/A	N/A	N/A
3	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A
4	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A
5	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A

RF = 83.5 GHz, LO = 14.083 GHz

	nLO							
mIF	0	1	2	3	4	5	6	7
-5	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-4	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-3	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-2	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-1	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
0	N/A	-23	<-65	<-65	N/A	N/A	N/A	N/A
1	0	<-65	<-65	<-65	N/A	N/A	N/A	N/A
2	-36	<-65	<-65	<-65	N/A	N/A	N/A	N/A
3	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A
4	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A
5	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A

RF = 86 GHz, LO = 14.5 GHz

	nLO							
mIF	0	1	2	3	4	5	6	7
-5	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-4	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-3	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-2	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-1	N/A	-33	-56	-63	N/A	N/A	N/A	N/A
0	N/A	-27	-42	-35	N/A	N/A	N/A	N/A
1	0	-35	-56	-60	N/A	N/A	N/A	N/A
2	-35	<-65	<-65	<-65	N/A	N/A	N/A	N/A
3	-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A
4	<-65	<-65	<-65	-64	N/A	N/A	N/A	N/A
5	<-65	<-65	<-65	-63	N/A	N/A	N/A	N/A

Spurious Performance, Upper Sideband Selected

T_A = 25°C, IF = 1 GHz, RFIN = -20 dBm , LO = 4 dBm. Mixer spurious products are measured in dBc from the IF output power level single-ended for frequencies below 50 GHz, with all other IF ports terminated. Spur values are (M × IF) + (N × LO). N/A means not applicable.

RF = 81 GHz, LO = 13.333 GHz

	nLO							
mIF	0	1	2	3	4	5	6	7
-5	N/A	<-65	<-65	<-65	-65	N/A	N/A	N/A
-4	N/A	<-65	<-65	<-65	-59	N/A	N/A	N/A
-3	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-2	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-1	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
0	N/A	-30	<-65	<-65	N/A	N/A	N/A	N/A
1	0	<-65	<-65	<-65	N/A	N/A	N/A	N/A
2	-38	<-65	<-65	<-65	N/A	N/A	N/A	N/A
3	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A
4	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A
5	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A

RF = 83.5 GHz, LO = 13.75 GHz

	nLO							
mIF	0	1	2	3	4	5	6	7
-5	N/A	<-65	<-65	<-65	-56	N/A	N/A	N/A
-4	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-3	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-2	N/A	-64	<-65	<-65	N/A	N/A	N/A	N/A
-1	N/A	-42	<-65	<-65	N/A	N/A	N/A	N/A
0	N/A	-22	-55	-40	N/A	N/A	N/A	N/A
1	0	-42	<-65	<-65	N/A	N/A	N/A	N/A
2	-34	<-65	<-65	<-65	N/A	N/A	N/A	N/A
3	-59	<-65	<-65	<-65	N/A	N/A	N/A	N/A
4	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A
5	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A

RF = 86 GHz, LO = 14.166 GHz

	nLO							
mIF	0	1	2	3	4	5	6	7
-5	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-4	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-3	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-2	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
-1	N/A	<-65	<-65	<-65	N/A	N/A	N/A	N/A
0	N/A	-23	<-65	<-65	N/A	N/A	N/A	N/A
1	0	<-65	<-65	<-65	N/A	N/A	N/A	N/A
2	-39	<-65	<-65	<-65	N/A	N/A	N/A	N/A
3	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A
4	<-65	<-65	<-65	<-65	N/A	N/A	N/A	N/A
5	<-65	<-65	<-65	-63	N/A	N/A	N/A	N/A

Table 5. Absolute Maximum Ratings

VD_AMP	4.5 V
VD_MULT	3 V
VD12_LNA, VD34_LNA	4.5 V
VG_AMP	-3 V to 0.2 V
VG_MULT	-3 V to 0.2 V
VG12_LNA, VG34_LNA	-3 V to 0.2 V
LO Drive	10 dBm
Storage Temperature	-55°C to 150°C
Peak Reflow Temperature	260°C
ESD Sensitivity, Human Body Model (HBM)	Class 0 (100 V)
ESD Sensitivity, Field-induced Charged Device Model (FICDM)	Class C0b (200 V)

Table 6. Reliability Information

Maximum Junction Temperature (to Maintain 3 Million Hours (MTTF))	175°C
Nominal Junction Temperature (TA = 85°C)	147°C
Thermal Resistance (R_{TH}) (junction to ground paddle)	51.1°C/W
Operating Temperature	-40°C to +85°C
Temperature Humidity Bias (THB) [1] [2] [3]	JESD22-A101
Temperature Humidity Storage (THS) [1] [3]	JESD22-A101

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing

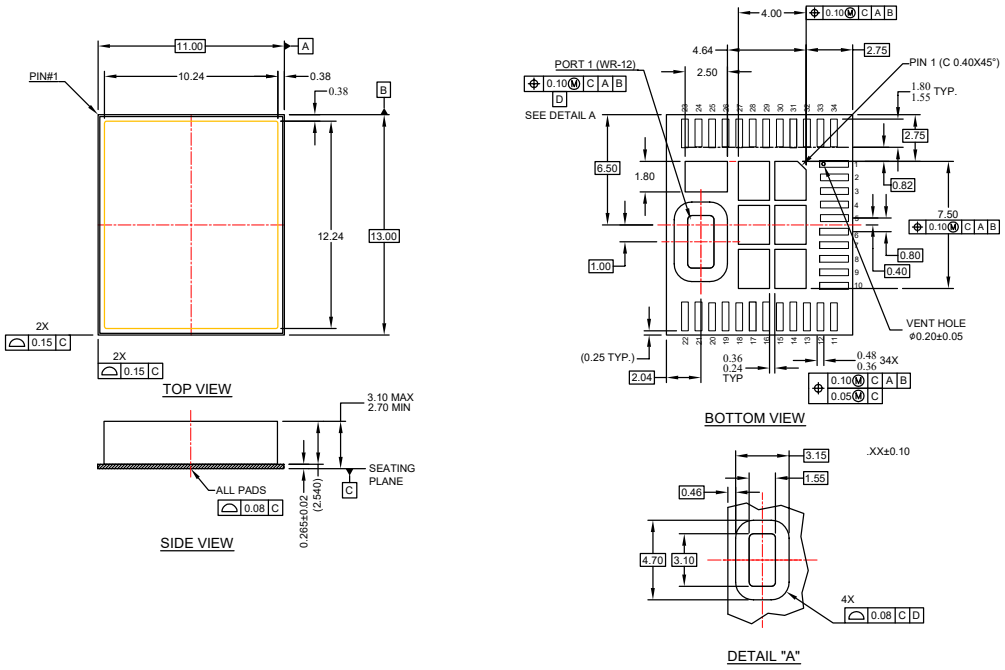


Table 7. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating [6]	Package Marking [4] [5]
HMC8327LG	Nickel Plated Copper Lid, Laminate Substrate	ENEPIG	MSL3	HMC8327LG YYWW XXXXXXX Country of Origin

[1] Samples subject to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake 24 hours at 125°C, Unbiased Soak: 192 hours at 30°C, 60% RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.
[2] Results valid for 50% of nominal DC power dissipation up to 100% of nominal power dissipation for all active devices. Analog Devices Inc. recommends that customers perform their own THB test for all other bias conditions.
[3] Valid for package vent hole solder sealed or unsealed during test.
[4] Year and week number, YYWW.
[5] Assembly lot number, XXXXXXX.
[6] Max peak reflow temperature of 260°C.

Table 8. Pin Descriptions

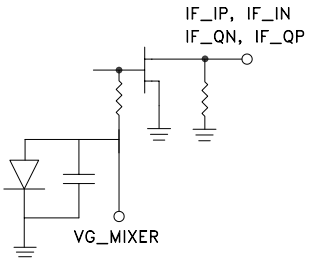
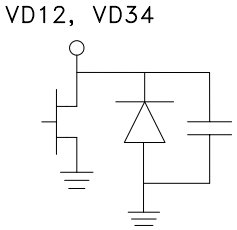
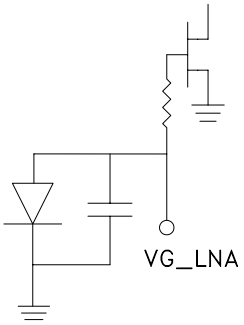
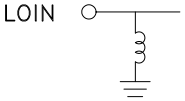
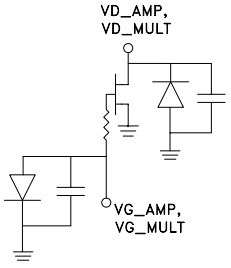
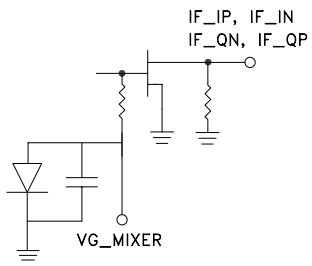
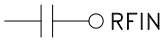
Pin Number	Function	Description	Pin Schematic
1, 6-12, 14, 16, 17, 19, 21-23, 25, 27, 29, 31, 34, G1-G8	GND	Ground connections. These pins and exposed ground paddle must be connected to RF/DC ground.	
2, 3	IF_IP, IF_IN	Positive and Negative IF I outputs. These pins are dc-coupled. When operation to dc is not required, block these pins externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, these pins must not source or sink more than 3 mA of current or part malfunction and part failure may result.	
4, 5	IF_QN, IF_QP	Negative and Positive IF Q outputs. These pins are dc-coupled. When operation to dc is not required, block these pins externally using a series capacitor with a value chosen to pass the necessary frequency range. For operation to dc, these pins must not source or sink more than 3 mA of current or die malfunction and part failure may result.	
13, 18	VD34_LNA, VD12_LNA	Drain voltage for the low noise amplifier. External bypass capacitor of 4.7 µF is recommended.	
15, 20	VG34_LNA, VG12_LNA	Gate voltage for the low noise amplifier. External bypass capacitor of 4.7 µF is recommended.	
24	LOIN	Local oscillator input. This pin is DC coupled and matched to 50 Ohm.	
26	VG_MULT	Gate voltage for the LO multiplier. External bypass capacitor of 4.7 µF is recommended.	
28	VD_MULT	Drain voltage for the LO multiplier. External bypass capacitor of 4.7 µF is recommended.	
30	VG_AMP	Gate voltage for the LO amplifier. External bypass capacitor of 4.7 µF is recommended.	
32	VD_AMP	Drain voltage for the LO amplifier. External bypass capacitor of 4.7 µF is recommended.	

Table 8. Pin Descriptions

Pin Number	Function	Description	Pin Schematic
33	VG_MIXER	Gate voltage for the FET mixer. External bypass capacitor of 4.7 µF is recommended.	
Port1	RFIN	WR12 waveguide port. This port is AC coupled and matched to 50 ohm.	

Theory of Operation

The HMC8327LG is fully integrated System in Package (SiP) in phase/quadrature (I/Q) low noise downconverter that is made up of 2 functional blocks.

The RFIN port of the HMC8327LG is connected to the GaAs low noise amplifier that is made up of four stages of low noise amplification that feeds into the second block.

The second block is a GaAs I/Q downconverter with an integrated LO buffer and 6× multiplier. The 6× multiplier allows the use of a lower frequency range LO input signal,typically between 13.4 GHz and 14.6 GHz. The 6× multiplier is implemented using a cascade of 3× and 2× multipliers. The LO buffer amplifiers are included on chip to allow a typical LO drive level of only +4 dBm for full performance. The LO path feeds a quadrature splitter followed by on-chip baluns that drive the I and Q mixer cores. The mixer cores comprise singly balanced passive mixers. The RF input of the I and Q mixers are then driven through an on-chip Wilkinson power splitter, which is then fed by the first block of the HMC8327LG.

Bias Procedure

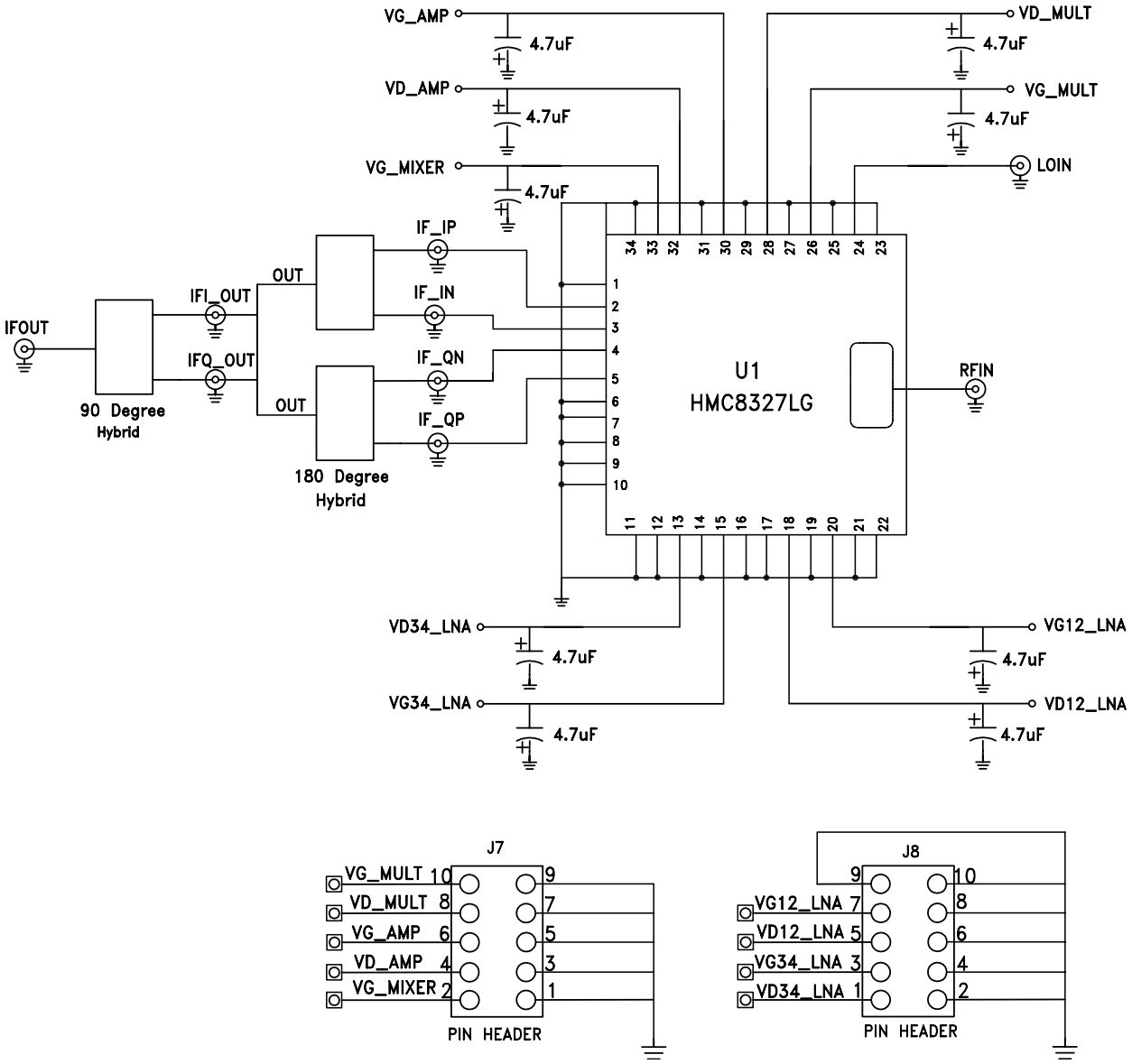
The HMC8327LG functional blocks uses multiple amplifier and multiplier stages, which are actve stages that all use depletion mode pseudomorphic high electron mobility transistors (pHEMTs). To ensure transistor damage does not occur, use the following power-up bias sequence and do not apply RF power to the device on the LO or IF ports unless otherwise noted:

1. Apply a -2 V bias to VG_MULT, VG_AMP, VG12_LNA and VG34_LNA.
2. Apply a -1 V bias to VG_MIXER.
3. Apply a 2 V bias to VD12_LNA.
4. Apply a 1.5 V bias to VD_MULT.
5. Apply a 4 V bias to VD_AMP and VD34_LNA.
6. Adjust VG_AMP between -2 V to 0 V to achieve a total quiescent ID_AMP current of 175 mA.
7. Adjust VG12_LNA between -2 V to 0 V to achieve a total quiescent ID12_LNA current of 22 mA.
8. Adjust VG34_LNA between -2 V to 0 V to achieve a total quiescent ID34_LNA current of 44 mA.
9. Apply a LO input signal on the LO port and adjust VG_MULT between -2 V and 0 V to achieve a total ID_MULT current of 80 mA.

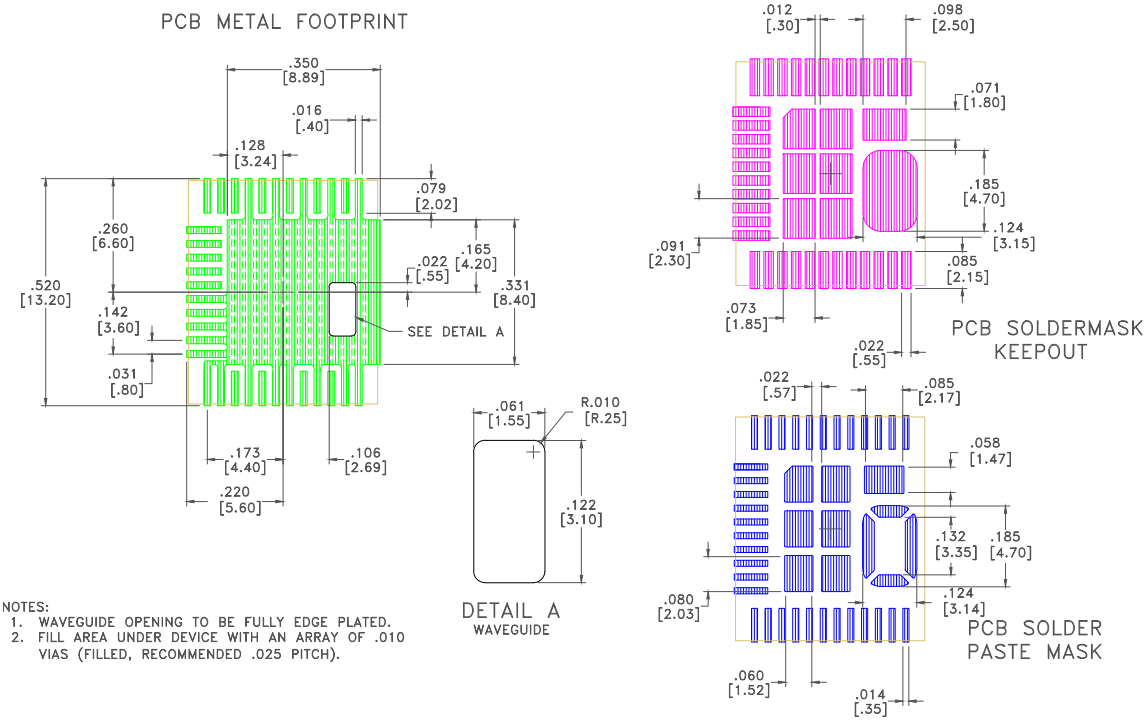
To ensure transistor damage does not occur, use the following power-down bias sequence:

1. Apply a 0 V bias to VD_MULT, VD_AMP, VGA_VD12 and VD34_LNA.
2. Apply a 0 V bias to VG_MIXER.
3. Apply a 0 V bias to VG_MULT, VG_AMP, VG12_LNA and VG34_LNA.

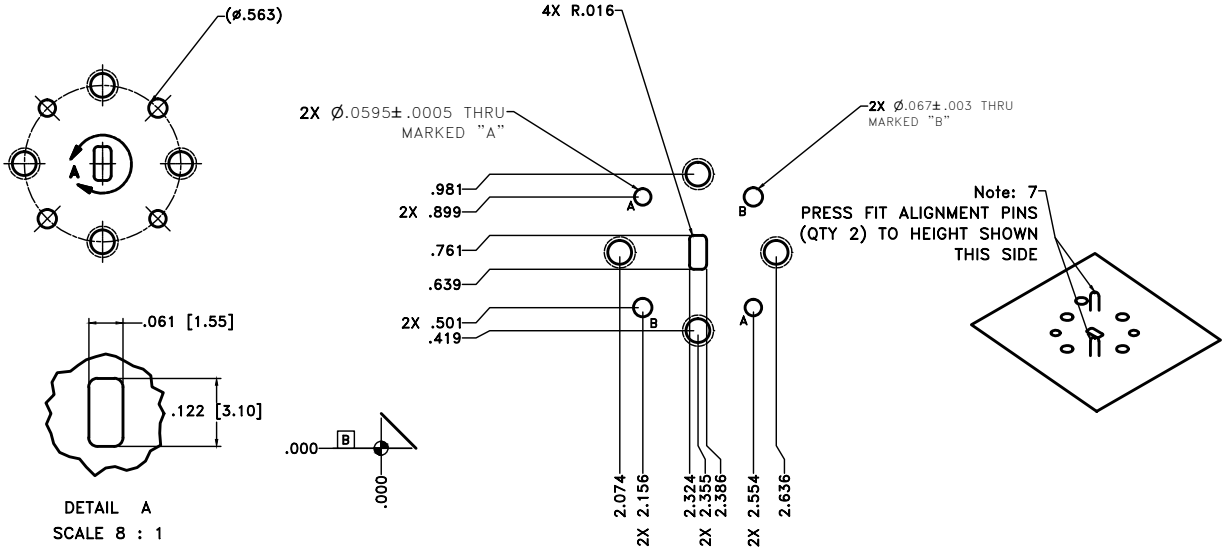
Application Circuit



Recommended PCB Land Pattern and Solder Mask Keep-out



Recommended Standard WR-12 Footprint for Backplate

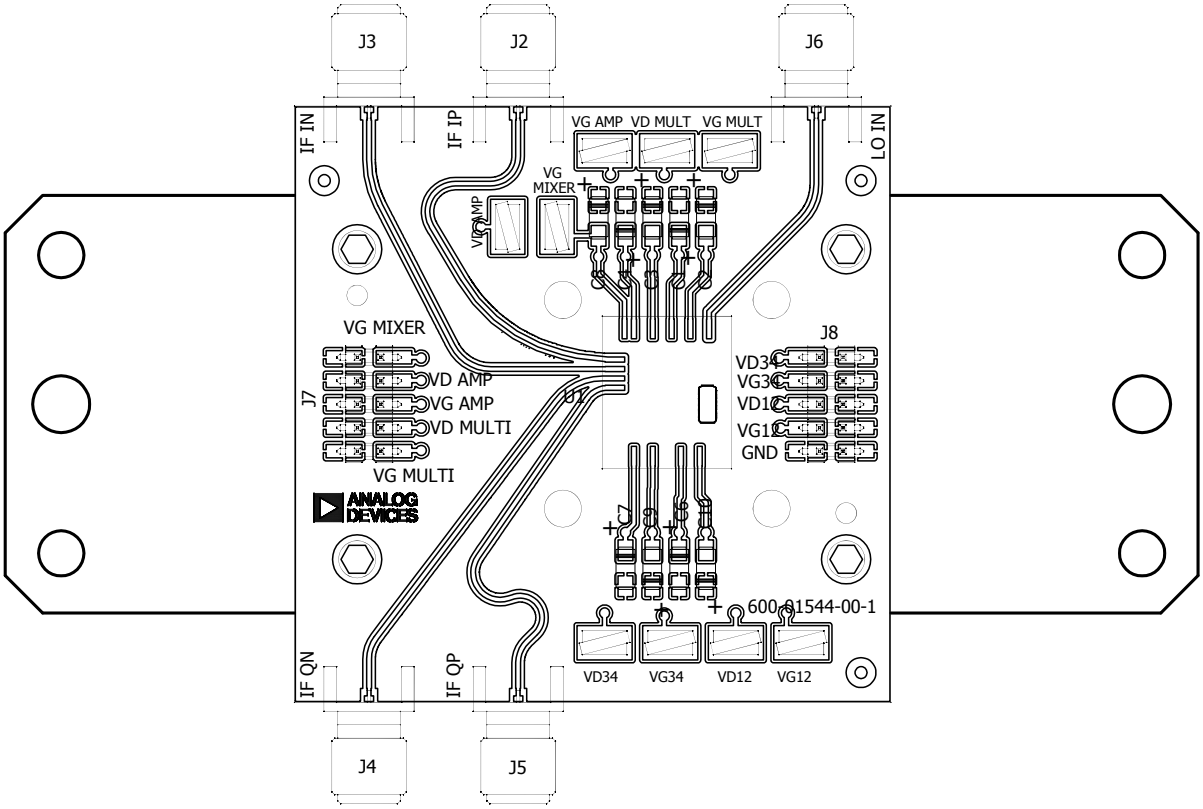


Part List				
ITEM	QTY	VENDOR	STOCK NUMBER	DESCRIPTION
1	2	VARIOUS	VARIOUS	PIN, ALIGNMENT, FLANGE, .0615 DIA

NOTES:

1.0 REMOVE BURRS AND BREAK SHARP EDGES.
2.0 ALL INTERNAL RADII SHALL BE .090 UNLESS OTHERWISE NOTED
3.0 SURFACE FINISH 32 RMS UNLESS OTHERWISE SPECIFIED
4.0 DIMENSIONS APPLY AFTER PLATING
5.0 MATERIAL: ALUMINUM 6061-T6 PER QQ-A-250/11
6.0 FINISH: NONE.
7.0 INSTALL DOWEL PINS.
8.0 USE ELECTRONIC DATA FOR ALL GEOMETRY THAT IS NOT DIMENSIONED.

Evaluation PCB



List of Materials for Evaluation PCB

Item	Description
J2, J6	SMA CONNECTOR, SRI
J7 - J8	CONNECTOR HEADER 10 POS, SMT
C1 - C4, C8 - C10	4.7 µF CAPACITOR, SMD 3216
U1	HMC8327LG
605-01131-00	MCH, PIN PLATE, E-BAND FIXTURE
620-00229-00	EPOXY PREFORM
SCREW	SOCKET HEAD CAP,4-40 UNC 3/16
PCB [1]	600-01236-00 Evaluation Board

[1] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices upon request.

Table 20. Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC8327LG Evaluation PCB	EV1HMC8327LG [1]

[1] Reference this number when ordering Evaluation PCB

Notes: