19-3441; Rev 0; 10/04

MAXIM

双闪存引脚电子测量/高压开关矩阵

概述

MAX9960双路闪存引脚电子/高压开关矩阵可替代闪存或SOC ATE系统 (图1)中用来连接系统信号源与两个引脚的继电器和开关。器件每通道可提供7个开关，最多选择4个独立源：引脚电子 (PE)、两路参数测量单元 (PMU) 或其它开尔文模拟信号源、一路闪存编程高压 ($FV_{HH\_}$)。PMU加载和感应开关可独立控制，用于连接两路非开尔文源，替代PMU或开尔文源。MAX9960两个通道中的每一通道均包括可完全独立控制的7路开关。

MAX9960信号通道中的开关在通用引脚电子测量IC的整个电压范围内具有600MHz带宽、低至3Ω的串联电阻和低至8pF的并联电容。片内1倍或2倍增益可选的缓冲器产生闪存高压，由 6.5V DAC基准输入产生最大13V的闪存编程电压。

当从$FV_{HH_}$切换至PE_或者从PE_切换至$FV_{HH_}$时，被测器件 (DUT_) 电压具有单调性。PE_和$FV_{HH_}$输入切换时间通常小于350ns。

MAX9960工作在0°C至+70°C商业级温度范围，提供48引脚、薄型QFN封装 (7mm x 7mm x 0.8mm)，封装底部带有裸露焊盘，有助于散热。

应用

闪存存储器自动测试设备

SOC自动测试设备

特性

- ◆ 双路高压开关矩阵
- ◆ 3Ω、8pF、600MHz带宽的引脚电子测量通道
- ◆ 13V闪存编程通道
- ◆ 内部选择1倍或2倍增益
- ◆ 两个开尔文PMU通道
- ◆ 快速切换：350ns (典型值)
- ◆ PE_和$FV_{HH_}$之间切换时具有单调摆率

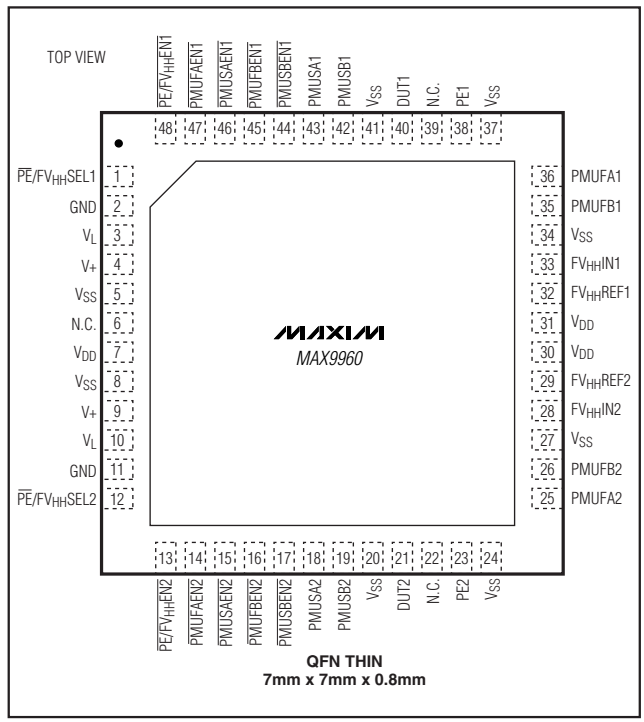
定购信息

PART	TEMP RANGE	PIN-PACKAGE*	PKG CODE
MAX9960BCTM	0°C to +70°C	48 Thin QFN-EP** (7mm x 7mm x 0.8mm)	T4877-6

** 详细的封装信息请参考本数据资料的最后部分。*

*** EP = 裸露焊盘。*

引脚配置



ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +26V
V_{DD} to GND .....-0.3V to +16.5V
V_{SS} to GND .....-6.5V to +0.3V
V_L to GND .....-0.3V to +6V
V+ to V_{SS} .....+32V
Digital Inputs .....(GND - 0.3V) to (V_L + 0.3V)
$FV_{HH}IN\_$ .....(the higher of -4V and (V_{SS} - 0.3V)) to (the lower of +10V and (V_{DD} + 0.3V))
All Other Pins .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Continuous Current, PE_ .....±120mA
Continuous Current, PMUS_ _ .....±10mA
Continuous Current, PMUFA_ + PMUFB_ + (FVHH_ Path) .....±45mA
Peak Current (100ns), PE_ .....±300mA
Peak Current (100ns), PMUS__ .....±20mA
Peak Current (100ns), PMUFA_ + PMUFB_ + (FVHH_ Path) .....±70mA
Package Continuous Power Dissipation (T_A = +70°C)
48-Pin QFN-EP, on Single-Layer Board (derate 27.8mW/°C above +70°C) 2222mW
48-Pin QFN-EP, on Multilayer Board (derate 40.0mW/°C above +70°C) 3200mW
Operating Temperature Range .....0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
PE_ PATH						
On-Resistance	R_{ON}	$V_{DUT\_}$ = +2.5V, I_{SW} = -40mA to +40mA, T_A = 0°C to +30°C (Note 1)	2.5	3.0	3.5	Ω
		$V_{DUT\_}$ = +2.5V, I_{SW} = -40mA to +40mA, T_A = +30°C to +70°C (Note 1)	2.5		4.2	
On-Resistance Flatness	$R_{FLAT(ON)}$	$V_{DUT\_}$ = 0 to +5V (Note 1)	-0.6		+0.6	Ω
Ch1 to Ch2 Resistance Match	R_{MATCH}	$V_{DUT\_}$ = +2.5V, I_{SW} = -40mA to +40mA	-0.5		+0.5	Ω
Signal Voltage Range	V_{PE}		-3.5		+8.0	V
Operating DC Current Range	I_{SW}		-40		+40	mA
$FV_{HH\_}$ PATH						
On-Resistance	R_{ON}	$FV_{HH\_}$ = -1.5V to (V_{DD} - 1.5V), $I_{HH\_}$ = -10mA to +10mA (Notes 1, 2)	32		100	Ω
Operating Voltage Range	$FV_{HH\_}$		-1.5		V_{DD} - 1.5	V
Operating DC Current Range	I_{SW}		-10		+10	mA
FORCE PATHS						
On-Resistance	R_{ON}	$V_{PMUF\_\_}$ = -4.25V to +14.5V, $I_{PMUF\_\_}$ = -25mA to +25mA (Note 1)			70	Ω
Operating Voltage Range	V_{PMUF}		-4.25		+14.5	V
Operating DC Current Range	I_{SW}		-25		+25	mA
SENSE PATHS						
On-Resistance	R_{ON}	$V_{PMUS\_\_}$ = -4.25V to +14.5V, $I_{PMUS\_\_}$ = -1mA to +1mA (Note 1)			1250	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{PMUS}		-4.25		+14.5	V
Operating DC Current Range	I_{SW}		-1		+1	mA
FV_{HH}_ BUFFERS						
DC Output Current	I_{ODC}	FV_{HH} = -1.5V to (V_{DD} - 1.5V)	10			mA
Current Limit	I_{LIM}	DUT_ sourcing current	+15		+25	mA
		DUT_ sinking current	-25		-15	
Operating Voltage Range	FV_{HH}	FV_{HH}REF_ = 0 (Note 2)	-1.5		V_{DD} - 1.5V	V
Linearity Error	L_{ER}_FV_{HH}	FV_{HH}REF_ = 0; no load; relative to 2-point line between V_{DUT}_ = 0 and +13V; measured at V_{DUT}_ = +3.25V, +6.5V, and +9.75V	-2		+2	mV
Gain	GFV_{HH}	FV_{HH}REF_ = 0, no load, V_{DUT}_ = 0 to +13V (Note 3)	1.98	2.00	2.02	V/V
Output Offset	V_{OS}_FV_{HH}	FV_{HH}REF_ = 0, V_{DUT}_ = +12V, no load	-50		+50	mV
Output Offset Temperature Coefficient	T_{C_VOS}	V_{DUT}_ = 0 to +13V, FV_{HH}REF_ = 0, T_{CASE} = +30°C to +50°C		±0.2		mV/°C
Input Bias Current	IFV_{HH}	FV_{HH}IN_ = -1.5V to +7.5V, FV_{HH}REF_ = open	-25		+25	µA
Gain Resistor Ground	FV_{HHREF}	(Note 4)	-1.5		+0.5	V
Gain Resistor Current	I_{VHHREF}	Measured with FV_{HH}IN_ = +5V, FV_{HH}REF_ = 0		0.4		mA
LEAKAGE (Notes 5, 6)						
DUT_ Leakage, Disabled	I_{LEAK_OFF}	Switches S1, S2, S6, S7 open; V_{DUT}_ = -4.25V to +14.5V	-1		+1	nA
PE_ Leakage	I_{LEAK_PE}	S1 closed; S2, S6, S7 open; V_{DUT}_ = -3.5V to +8V	-1		+1	nA
PMUA_ Path Leakage, Enabled	$I_{LEAK\_PMUA\_ON}$	S2, S4, S6 closed; S1, S3, S5, S7 open; V_{DUT}_ = -4.25V to +14.5V	-1		+1	nA
PMUB_ Path Leakage, Enabled	$I_{LEAK\_PMUB\_ON}$	S2, S5, S7 closed; S1, S3, S4, S6 open; V_{DUT}_ = -4.25V to +14.5V	-1		+1	nA
PMUA_ Path Leakage, Disabled	$I_{LEAK\_PMUA\_OFF}$	S4, S6 open; V_{PMUFA}_ = -4.25V to +14.5V; measured at PMUFA_ with PMUSA_ externally connected to PMUFA_	-1		+1	nA
PMUB_ Path Leakage, Disabled	$I_{LEAK\_PMUB\_OFF}$	S5, S7 open; V_{PMUFB}_ = -4.25V to +14.5V; measured at PMUFB_ with PMUSB_ externally connected to PMUFB_	-1		+1	nA
DIGITAL INPUTS ($\overline{PMUF\_EN\_}$, $\overline{PMUS\_EN\_}$, $\overline{PE/FV_{HH}EN\_}$, $\overline{PE/FV_{HH}SEL\_}$)						
Input High Voltage	V_{IH}		+2.3			V
Input Low Voltage	V_{IL}				+0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		-0.2		V_L	V
Input Current	I_{IH}, I_{IL}	V_{IN} = -0.2V to V_L	-10		+10	µA
POWER SUPPLIES						
Positive Supply	V_{DD}		14.5	15	16.0	V
Negative Supply	V_{SS}		-6.00	-5	-4.25	V
High Voltage Supply	V+	(Note 1)	23	24	25	V
Logic Supply	VL		3.0	3.3	3.6	V
Quiescent Positive Supply Current	$\sum (I_{DD}, I+)$	V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, $FV_{HH}IN\_$ = +6.5V, $FV_{HH}REF\_$ = 0, all digital inputs = +2.3V, no loads			10	mA
Quiescent Negative Supply Current	I_{SS}	V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, $FV_{HH}IN\_$ = +6.5V, $FV_{HH}REF\_$ = 0, all digital inputs = +2.3V, no loads			8.5	mA
Quiescent Logic Supply Current	I_{VL}	V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, $FV_{HH}IN\_$ = +6.5V, $FV_{HH}REF\_$ = 0, all digital inputs = +2.3V, no loads			2	mA
Quiescent Power Dissipation	P_{DQ}	V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, $FV_{HH}IN\_$ = +6.5V, $FV_{HH}REF\_$ = 0, all digital inputs = +2.3V, no loads			200	mW
AC CHARACTERISTICS						
SWITCHING TIMES BETWEEN PE_ AND FV_{HH}_ PATHS (Note 7) (Figure 3)						
Switch PE_ to FV_{HH}_	t_{ON_FVHH}	+5V to +7V transition		275	425	ns
		0 to +13V transition		350	500	
FV_{HH}_ Settling Time	t_{S_FVHH}	Settling to within larger of 1% step voltage or 50mV of final value		500		ns
Switch FV_{HH}_ to PE_	t_{ON_PE}			300	425	ns
PE_ Settling Time	t_{S_PE}	Settling to within larger of 1% step voltage or 50mV of final value		500		ns
PE_ TO FV_{HH}_ Overshoot/Undershoot				±100		mV
PE_ to FV_{HH}_ Preshoot				±150		mV
Minimum Switching Slew Rate	SR_{MIN}	Over 20% to 80% region		±10		V/µs
SWITCHING TIMES, SAME PATH (Note 8) (Figure 2)						
PE_ Switch On-Time	t_{ON_1}	$V_{PE\_}$ = +5V from 47Ω source		150		ns
FV_{HH}_ Switch On-Time	$t_{ON\_2,3}$	$FV_{HH}IN\_$ = +2.5V, $FV_{HH}REF\_$ = 0		350		ns

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMUF_ _ Switch On-Time	$t_{ON\_2,4}$ $t_{ON\_2,5}$	$V_{PMUF\_\_}$ = +5V		150		ns
PMUS_ _ Switch On-Time	t_{ON_6} t_{ON_7}	$V_{PMUS\_\_}$ = +5V		300		ns
PE_, $FV_{HH\_}$, PMUF_ _, PMUS_ _ Switch Off-Times	t_{OFF}			700		ns
CAPACITANCE AND BANDWIDTH (Note 5)						
Capacitance, All Paths Disconnected	C_{DUT_OFF}	All switches disconnected, for frequencies greater than 2MHz (Note 9)		20		pF
Capacitance, PE_ Path Connected (Note 9)	C_{DUT_PE}	Switch S1 closed, all others open, for frequencies greater than 2MHz		8		pF
		Switch S1 closed, all others open, for frequencies less than 1kHz		50		
Unit-to-Unit Variation, PE_ Path Connected	ΔC_{DUT_PE}	Switch S1 closed, all others open, for frequencies greater than 2MHz (Note 9)		±2		pF
Capacitance, PMUFA_ and PMUSA_ Path Connected	C_{DUT_PMUA}	S2, S4, and S6 closed; all others open (Note 9)		35		pF
Capacitance, PMUFB_ and PMUSB_ Path Connected	C_{DUT_PMUB}	S2, S5, and S7 closed; all others open (Note 9)		35		pF
Capacitance, PMUFA_ Path Disconnected	C_{PMUFA_OFF}	S4 open, measured at PMUFA_ (Note 9)		10		pF
Capacitance, PMUFB_ Path Disconnected	C_{PMUFB_OFF}	S5 open, measured at PMUFB_ (Note 9)		10		pF
Capacitance, PMUSA_ Path Connected	C_{PMUSA_ON}	S6 closed, all others open, measured at PMUSA_ (Note 9)		10		pF
Capacitance, PMUSB_ Path Connected	C_{PMUSB_ON}	S7 closed, all others open, measured at PMUSB_ (Note 9)		10		pF
Capacitance, PMUSA_ Path Disconnected	C_{PMUSA_OFF}	S6 open, measured at PMUSA_ (Note 9)		5		pF
Capacitance, PMUSB_ Path Disconnected	C_{PMUSB_OFF}	S7 open, measured at PMUSB_ (Note 9)		5		pF
PE_ Signal Bandwidth	f_{3DB}	Only PE_ path enabled (Note 10)		600		MHz
$FV_{HH\_}$ BUFFER						
Slew Rate	$SRFV_{HH}$	$FV_{HH}REF\_$ = 0, (gain = 2), $FV_{HH}IN\_$ stepped from 0 to +5V and +5V to 0		±5		V/µs
Settling	t_S	$C_{DUT\_}$ = 200pF to within 0.1% of step voltage, after $FV_{HH}IN\_$ changes		25		µs
		$C_{DUT\_}$ = 4000pF to within 0.1% of step voltage, after $FV_{HH}IN\_$ changes (Note 11)		50		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted. Specifications at T_A = 0°C and T_A = +70°C are guaranteed by design and characterization. Typical values are at T_A = +25°C, unless otherwise noted.) (Figure 1)

Note 1: V+ should be at least 8V above V_{DD} to guarantee specified path resistance values.

Note 2: When the FV_{HH}_ buffer is configured for a gain of +1 (FV_{HH}REF_ open), the output voltage range is limited to -1.5V to +7.5V.

Note 3: FV_{HH}_ buffer gain is typically +1, when FV_{HH}REF_ is open.

Note 4: FV_{HH}REF_ is tested by repeating the FV_{HH}_ path resistance tests over the variation of FV_{HH}REF_. For each value of FV_{HH}REF_, FV_{HH}IN_ is adjusted to FV_{HH}IN_ = (FV_{HH}_ + FV_{HH}REF_) / 2.

Note 5: All measurements taken at DUT_, except where noted.

Note 6: These specifications are guaranteed by design and characterization. In addition, these specifications will be production tested with min/max test limits of ±10nA.

Note 7: Voltage source driving PE_ has 47Ω source resistance. PE_ = 0 to +5.0V, FV_{HH}_ = +7 to +13V. Measured from 50% point of input logic to 90% of analog swing.

Note 8: All unused switches open, unless otherwise noted. Measured from 50% point of input logic to 90% of analog swing.

Note 9: Unless otherwise noted, measured at DUT_. No external connections to any of the switched analog pins—PE_, DUT_, PMUFA_, PMUFB_, PMUSA_, or PMUSB_—except as needed to make measurement.

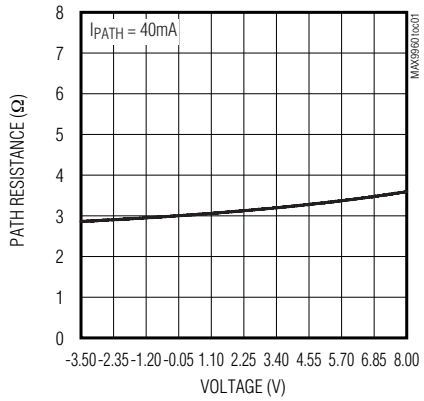
Note 10: $Z_{DUT\_}$ = 50Ω; equivalent bandwidth calculated from measured DUT_ rise and fall time with PE_ stimulated by a 3V step with 1ns 10% to 90% rise/fall time.

Note 11: The maximum load for FV_{HH} buffer is 4000pF.

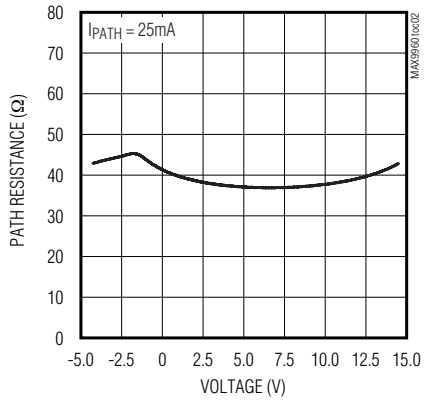
典型工作特性

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

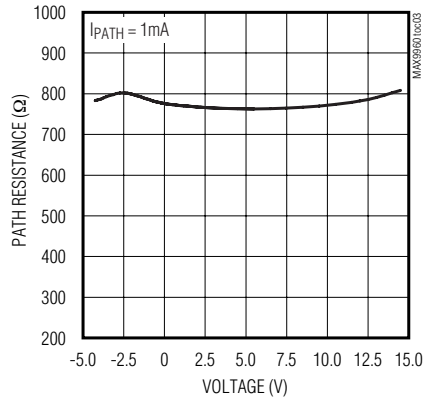
PE PATH RESISTANCE vs. VOLTAGE



FORCE PATH RESISTANCE vs. VOLTAGE



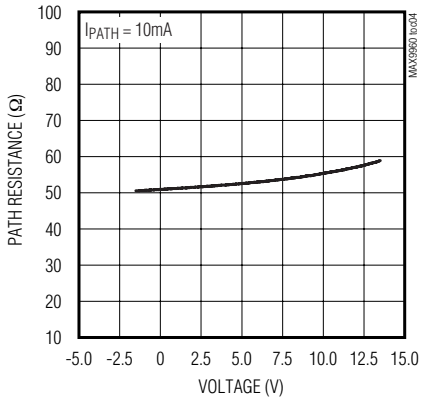
SENSE PATH RESISTANCE vs. VOLTAGE



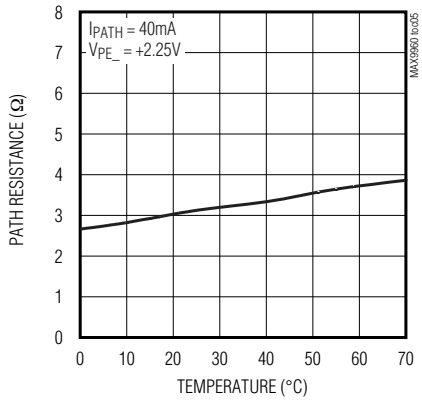
典型工作特性 (续)

(V+ = +24V, V_{DD} = +15V, V_{SS} = -5V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

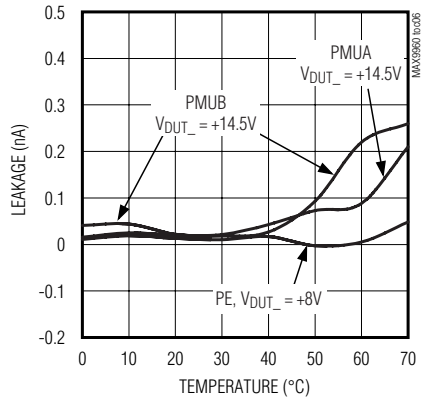
FV_{HH}_ PATH RESISTANCE vs. VOLTAGE



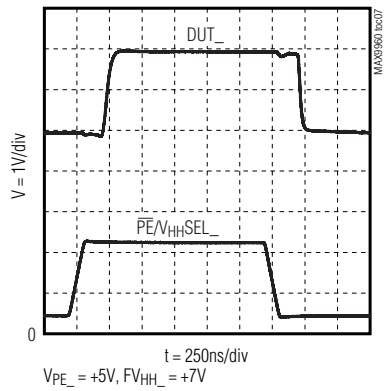
PE PATH RESISTANCE vs. TEMPERATURE



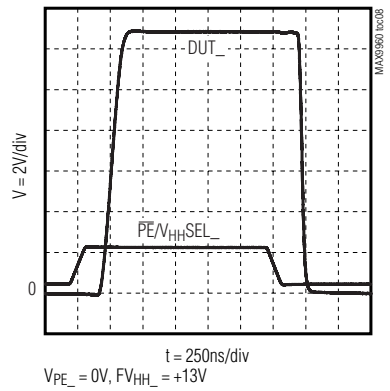
LEAKAGE CURRENT vs. TEMPERATURE



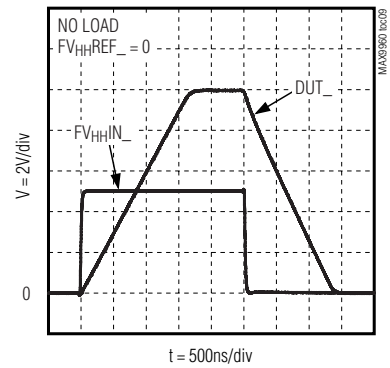
PE_ TO FV_{HH}_ TRANSITIONS



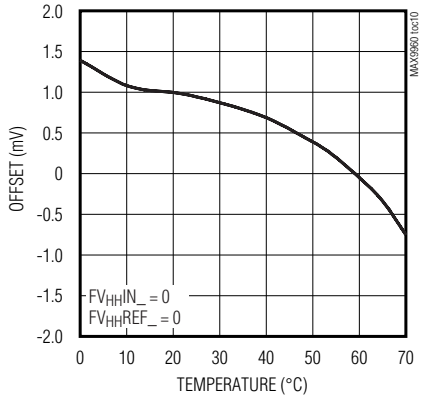
PE_ TO FV_{HH}_ TRANSITIONS



FV_{HH}_ SLEW



FV_{HH} BUFFER OUTPUT OFFSET vs. TEMPERATURE



双闪存引脚电子测量/高压开关矩阵

引脚	名称	功能
1	$\overline{PE}$/FV_{HH}SEL1	PE1或FV_{HH}1选择输入。选择PE1或者FV_{HH}1连接至DUT1。接低电平时选择PE1，接高电平时选择FV_{HH}1。
2, 11	GND	地
3, 10	V_L	逻辑电源。3.3V标称值。
4, 9	V+	正模拟电源，用于栅极驱动。24V标称值。
5, 8, 20, 24, 27, 34, 37, 41	V_{SS}	负模拟电源。-5V标称值。
6, 22, 39	N.C.	无连接。不要连接该引脚。
7, 30, 31	V_{DD}	正模拟电源。15V标称值。
12	$\overline{PE}$/FV_{HH}SEL2	PE2或FV_{HH}2选择输入。选择PE2或者FV_{HH}2连接至DUT2。接低电平时选择PE2，接高电平时选择FV_{HH}2。
13	$\overline{PE}$/FV_{HH}EN2	PE2和FV_{HH}2使能控制。由$\overline{PE}$/FV_{HH}SEL2选择将PE2或FV_{HH}2连接至DUT2。接低电平时使能信号通路，接高电平时禁止信号通路。
14	$\overline{PMUFAEN2}$	PMUFA2使能控制。控制PMUFA2与DUT2之间的连接。接低电平时连接PMUFA2至DUT2，接高电平时断开PMUFA2与DUT2的连接。
15	$\overline{PMUSAEN2}$	PMUSA2使能控制。控制PMUSA2与DUT2之间的连接。接低电平时连接PMUSA2至DUT2，接高电平时断开PMUSA2与DUT2的连接。
16	$\overline{PMUFBEN2}$	PMUFB2使能控制。控制PMUFB2与DUT2之间的连接。接低电平时连接PMUFB2至DUT2，接高电平时断开PMUFB2与DUT2的连接。
17	$\overline{PMUSBEN2}$	PMUSB2使能控制。控制PMUSB2与DUT2之间的连接。接低电平时连接PMUSB2至DUT2，接高电平时断开PMUSB2与DUT2的连接。
18	PMUSA2	通道2检测A路模拟输出。通道2的开尔文反馈输出加载到A通路。
19	PMUSB2	通道2检测B路模拟输出。通道2的开尔文反馈输出加载到B通路。
21	DUT2	通道2模拟I/O。连接至DUT。
23	PE2	通道2模拟I/O。连接至引脚电子I/O。
25	PMUFA2	通道2加载A路模拟输入。连接至外部直流源，如PMU。
26	PMUFB2	通道2加载B路模拟输入。连接至外部直流源，如PMU。
28	FV_{HH}IN2	通道2模拟高压输入。对加载到FV_{HH}IN2输入端的电压进行放大，增益由FV_{HH}REF2决定 (*参考功能框图*)。
29	FV_{HH}REF2	通道2模拟增益设置输入。设置FV_{HH}2缓冲器增益。
32	FV_{HH}REF1	通道1模拟增益设置输入。设置FV_{HH}1缓冲器增益。
33	FV_{HH}IN1	通道1模拟高压输入。对加载到FV_{HH}IN1输入端的电压进行放大，增益由FV_{HH}REF1决定 (*参考功能框图*)。
35	PMUFB1	通道1加载B路模拟输入。连接至外部直流源，如PMU。
36	PMUFA1	通道1加载A路模拟输入。连接至外部直流源，如PMU。
38	PE1	通道1模拟I/O。连接至引脚电子测量I/O。
40	DUT1	通道1模拟I/O。连接至DUT。
42	PMUSB1	通道1感应B路模拟输出。通道1的开尔文反馈输出加载到B通路。
43	PMUSA1	通道1感应A路模拟输出。通道1的开尔文反馈输出加载到A通路。

引脚说明 (续)

引脚	名称	功能
44	$\overline{\text{PMUSBEN1}}$	PMUSB1使能控制。控制PMUSB1与DUT1之间的连接。接低电平时连接PMUSB1至DUT1，接高电平时断开PMUSB1与DUT1的连接。
45	$\overline{\text{PMUFBEN1}}$	PMUFB1使能控制。控制PMUFB1与DUT1之间的连接。接低电平时连接PMUFB1至DUT1，接高电平时断开PMUFB1与DUT1的连接。
46	$\overline{\text{PMUSAEN1}}$	PMUSA1使能控制。控制PMUSA1与DUT1之间的连接。接低电平时连接PMUSA1至DUT1，接高电平时断开PMUSA1与DUT1的连接。
47	$\overline{\text{PMUFAEN1}}$	PMUFA1使能控制。控制PMUFA1与DUT1之间的连接。接低电平时连接PMUFA1至DUT1，接高电平时断开PMUFA1与DUT1的连接。
48	$\overline{\text{PE}}/\overline{\text{FV}_{\text{HH}}\text{EN1}}$	PE1和FV_{HH}1使能控制。由$\overline{\text{PE}}/FV_{HH}$SEL1选择PE1或$FV_{HH}$1连接至DUT1。接低电平时使能信号通路，接高电平时禁止信号通路。
—	EP	裸露焊盘用于散热。内部偏置到V_{SS}。连接至V_{SS}或浮空。

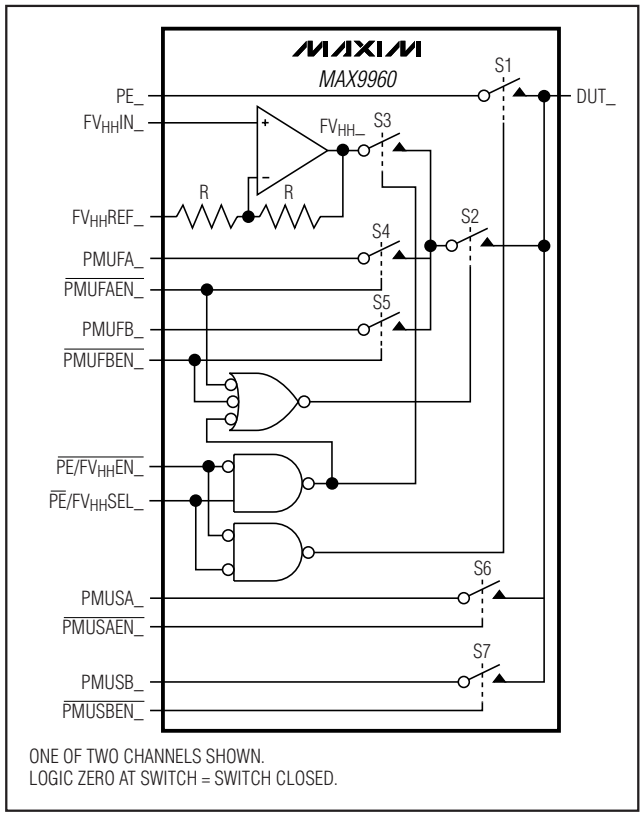


图1. 功能框图

详细说明

MAX9960双通道模拟开关矩阵具有两个开尔文PMU通路、一个PE通路和一个闪存编程高压电路，可采用标准PE器件对闪存存储器进行测试。该器件在不使用继电器的条件下，可实现AC和DC的全功能引脚测量。

信号通路开关在通用引脚电子测量IC的整个电压范围内具有600MHz带宽、3Ω串联电阻和8pF并联电容。倍压缓冲器提供可选的1倍或2倍增益，能够从6.5V输入产生13V闪存存储器编程电压。可使用数字输入$\overline{\text{PMUFAEN}}$_、$\overline{\text{PMUSAEN}}$_、$\overline{\text{PMUFBEN}}$_、$\overline{\text{PMUSBEN}}$_、$\overline{\text{PE}}/\overline{FV_{HH}\text{EN}}$_和$\overline{\text{PE}}/FV_{HH}$SEL_对开关进行设置，如表1、表2所示。

PE_和FV_{HH}_通路的切换时间通常小于350ns (图3)，切换期间DUT_具有单调特性。

FV_{HH}缓冲器负载电容

FV_{HH}缓冲器的最大负载电容为4000pF。正常工作时，不会有如此大的负载电容。偶尔进行校准时，可能需要缓冲器连接至具有大容性负载的PMU通道。即使在这种情况下，也不会损坏MAX9960。

超高压FV_{HH}缓冲器增益

可利用FV_{HH}REF_来选择FV_{HH}缓冲器的增益。FV_{HH}REF_接地时，缓冲器的增益为+2。FV_{HH}REF_浮空时，缓冲器的增益为+1。

表1. 开关控制的所有可能组合

$\overline{PMUFAEN\_}$	$\overline{PMUFBEN\_}$	$\overline{PMUSAEN\_}$	$\overline{PMUSBEN\_}$	$\overline{PE/FV_{HH}EN\_}$	$\overline{PE/FV_{HH}SEL\_}$	DUT_
0	X	X	X	X	X	PMUFA_ path connected
X	0	X	X	X	X	PMUFB_ path connected
X	X	0	X	X	X	PMUSA_ path connected
X	X	X	0	X	X	PMUSB_ path connected
X	X	X	X	0	1	FV_{HH}_ path connected
X	X	X	X	0	0	PE_ path connected
All other combinations						Every path is disconnected

表2. 开关控制和应用实例

$\overline{PMUFAEN\_}$	$\overline{PMUFBEN\_}$	$\overline{PMUSAEN\_}$	$\overline{PMUSBEN\_}$	$\overline{PE/FV_{HH}EN\_}$	$\overline{PE/FV_{HH}SEL\_}$	DUT_
1	1	1	1	0	0	PE_
1	1	1	1	0	1	FV_{HH}_
0	1	0	1	1	X	PMUFA_ + PMUSA_
1	0	1	0	1	X	PMUFB_ + PMUSB_
0	1	0	1	0	0	PE_ + PMUFA_ + PMUSA_
1	0	1	0	0	0	PE_ + PMUFB_ + PMUSB_
0	1	0	1	0	1	FV_{HH}_ + PMUFA_ + PMUSA_
1	0	1	0	0	1	FV_{HH}_ + PMUFB_ + PMUSB_
0	0	0	0	0	0	PE_ + PMUFA_ + PMUSA_ + PMUFB_ + PMUSB_

电源注意事项

MAX9960要求提供4种电源电压，典型值分别为V+ = +24V、V_{DD} = +15V、V_{SS} = -5V以及V_L = +3.3V。靠近每个电源引脚安装一个0.1µF的旁路电容，在电源进入电路板的位置应安装大容量旁路电容。MAX9960不需要任何特定的上电顺序。

芯片信息

TRANSISTOR COUNT: 2020

PROCESS: BiCMOS

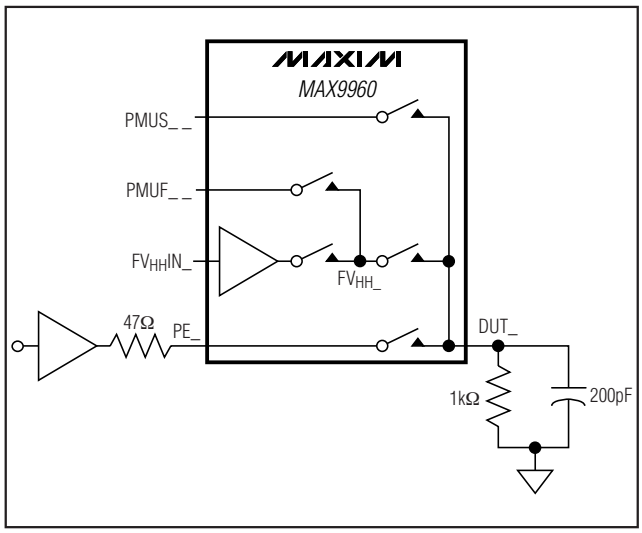


图2. 开关时序测试电路

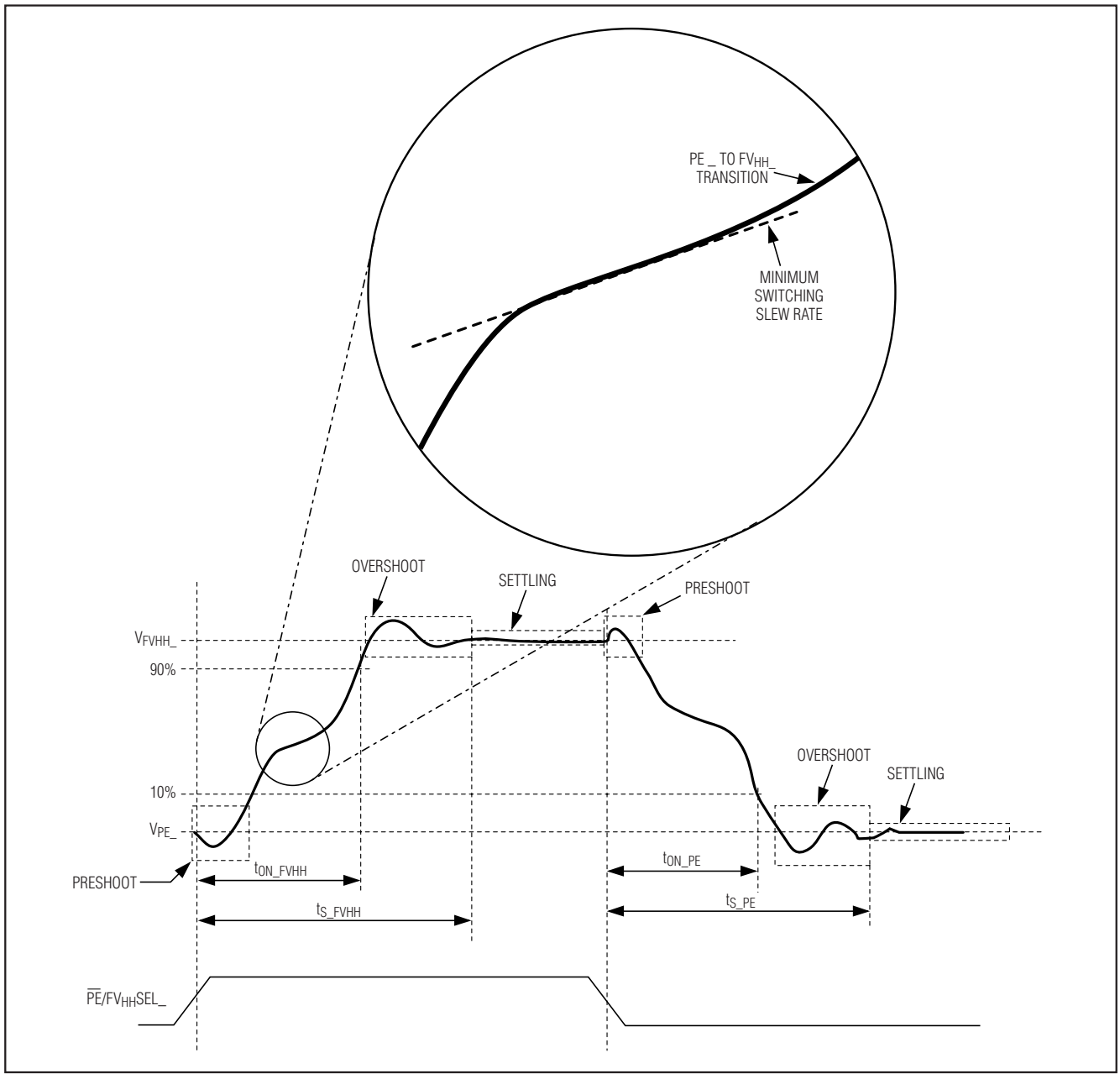


图3. PE_ - $FV_{HH_}$和$FV_{HH_}$ - PE_转换和建立时间

封装信息

如需最近的封装外型信息，请查询
www.maxim-ic.com.cn/packages。