19-6492; Rev 1; 8/13

备有评估板

# MAX98090

# 超低功耗立体声音频编解码器

## 概述

MAX98090是完全集成的音频编解码器，具有高性能、超低功耗和小占位面积，理想用于便携式应用。

器件具有灵活性非常高的输入方法，有六个输入引脚(WLP)，可配置为模拟或数字麦克风输入、差分或单端输入，或者满幅直接差分输入。模拟输入可连接至录音通路ADC或直接连接至任意模拟输出混音器。

器件支持256 x $f_S$或10MHz至60MHz的主机时钟频率。数字音频接口支持主机或从机工作模式，采样率为8kHz至96kHz，标准PCM格式(例如I²S)、左/右对齐和TDM。

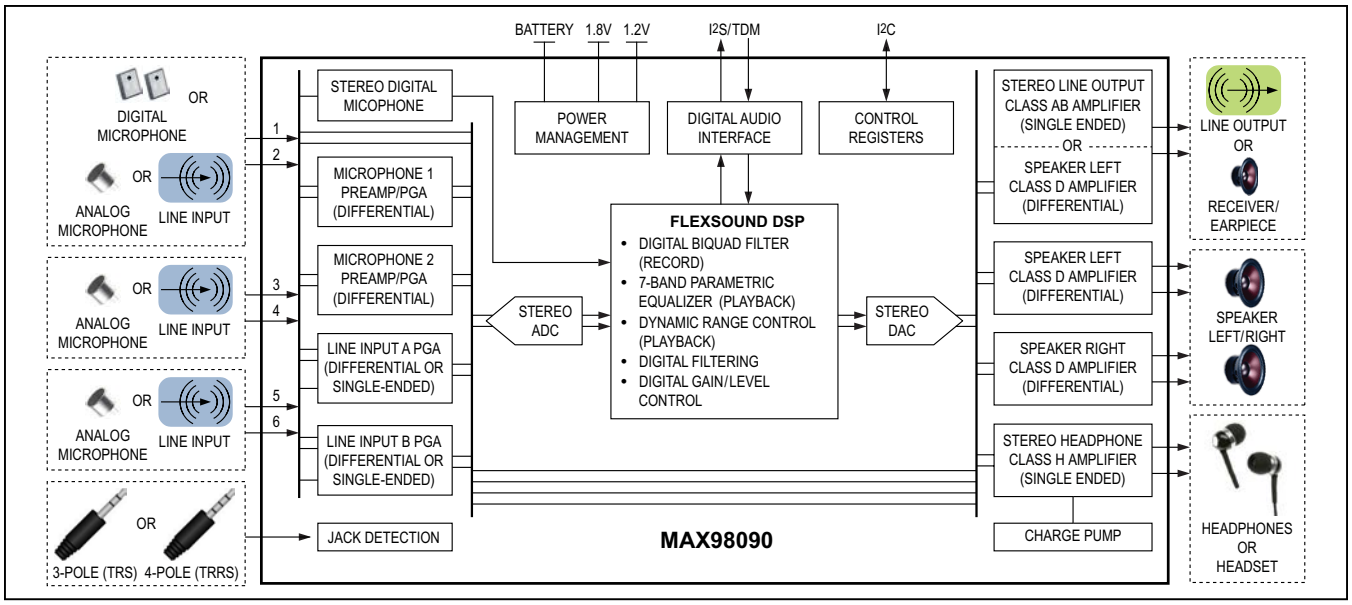
录音/回放通路具有采用FlexSound®技术的DSP，包括数字增益和滤波、双二阶滤波器(录音)、动态范围控制(回放)、七波段参数均衡器(回放)，可通过优化频率响应提高扬声器性能。

立体声D类扬声器放大器提供高效率放大，低辐射发射，支持无滤波工作，可驱动4Ω和8Ω负载。DirectDrive®立体声H类耳机放大器提供接地基准输出，从而不需要大隔直电容。器件也包括差分接收器(听筒)放大器，可重新配置为立体声单端输出。

## 特征和优势

- 102dB DR立体声DAC至HP (8kHz < $f_S$ < 96kHz)
- 3.6mW回放功耗
- 99dB DR立体声ADC (8kHz < $f_S$ < 96kHz)
- 4.2mW录音功耗
- 3路立体声单端/差分模拟麦克风/线输入(WLP版本)
- 立体声PDM数字麦克风输入
- 支持256 x $f_S$至60MHz主控时钟频率
- I²S/LJ/RJ/TDM数字音频接口
- FlexSound技术信号处理
  - 录音通路双二阶滤波
  - 回放通路7波段参数EQ
  - 回放通路自动电平控制
  - 数字滤波和增益/电平控制
- 立体声低EMI D类扬声器放大器
  - 3.2W/通道($R_L$ = 4Ω，$V_{SPK\_VDD}$ = 5V，WLP)
  - 1.8W/通道($R_L$ = 8Ω，$V_{SPK\_VDD}$ = 5V，WLP)
- 立体声DirectDrive H类耳机放大器插孔检测和识别
- 差分接收放大器/立体声输出
- 全面的咔嗒/噼噗声抑制电路
- 具有RF抑制的模拟输入和输出
- 可编程麦克风偏置
- I²C控制接口，具有两个地址选项
- 49焊球、0.4mm WLP和40引脚TQFN封装

## 简化框图




*相关型号以及配合该器件使用的推荐产品，请参见：china.maximintegrated.com/MAX98090.related。*

*定购信息在数据资料的最后给出。*

本文是英文数据资料的译文，文中可能存在翻译上的不准确或错误。如需进一步确认，请在您的设计中参考英文资料。

有关价格、供货及订购信息，请联络Maxim亚洲销售中心：10800 852 1249 (北中国区)，10800 152 1249 (南中国区)，或访问Maxim的中文网站：china.maximintegrated.com。

# 超低功耗立体声音频编解码器

## 目录

## 目录(续)

## 目录(续)

## 图示目录

## 图示目录(续)



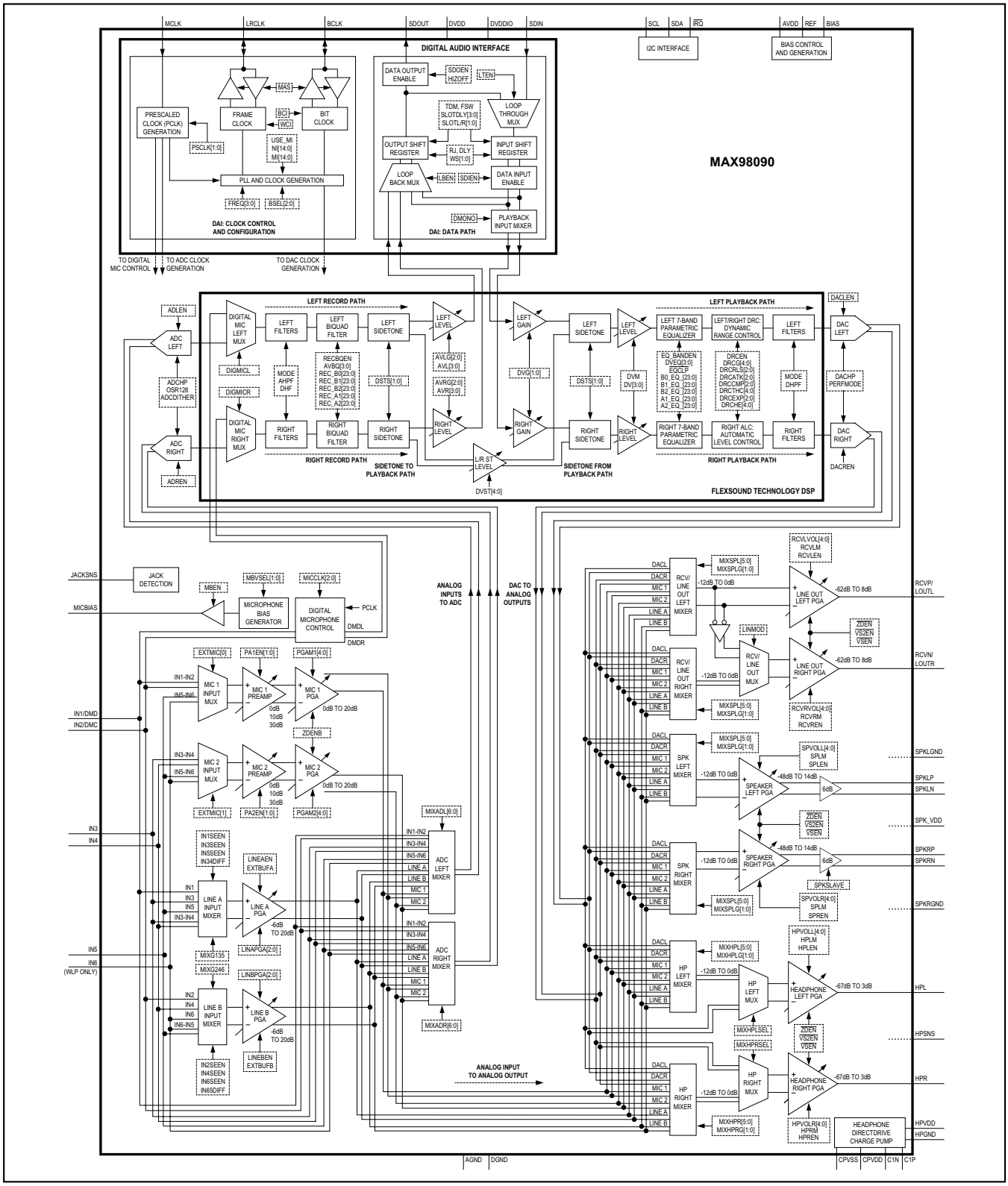
## 表格目录

## 目录

## 表格目录(续)

# 超低功耗立体声音频编解码器

## 功能框图



## Absolute Maximum Ratings

(Voltages with respect to AGND, unless otherwise noted.)
AVDD, DVDD, HPVDD .....-0.3V to +2.2V
SPKLVDD, SPKRVDD, DVDDIO .....-0.3V to +6.0V
DGND, HPGND, SPKLGND, SPKRGND.....-0.1V to +0.1V
CPVDD .....($V_{HPGND}$ - 0.3V) to ($V_{HPGND}$ + 2.2V)
CPVSS .....($V_{HPGND}$ - 2.2V) to ($V_{HPGND}$ + 0.3V)
C1N .....($V_{CPVSS}$ - 0.3V) to ($V_{HPGND}$ + 0.3V)
C1P..... ($V_{HPGND}$ - 0.3V) to ($V_{CPVDD}$ + 0.3V)
MICBIAS..... -0.3V to ($V_{SPKLVDD}$ + 0.3V)
REF, BIAS ..... -0.3V to ($V_{AVDD}$ + 0.3V)
MCLK, SDIN, SDA, SCL, $\overline{IRQ}$.....-0.3V to +6.0V
LRCLK, BCLK, SDOUT..... -0.3V to ($V_{DVDDIO}$ + 0.3V)
IN1, IN2, IN3, IN4, IN5, IN6 .....-0.3V to +2.2V
HPSNS .....($V_{HPGND}$ - 0.3V) to ($V_{HPGND}$ + 0.3V)
HPL, HPR.....($V_{CPVSS}$ - 0.3V) to ($V_{CPVDD}$ + 0.3V)
RCVP/LOUTL.....($V_{SPKLGND}$ - 0.3V) to ($V_{SPKLVDD}$ + 0.3V)
RCVN/LOUTR.....($V_{SPKLGND}$ - 0.3V) to ($V_{SPKLVDD}$ + 0.3V)
SPKLP, SPKLN .....($V_{SPKLGND}$ - 0.3V) to ($V_{SPKLVDD}$ + 0.3V)
SPKRP, SPKRN .....($V_{SPKRGND}$ - 0.3V) to ($V_{SPKRVDD}$ + 0.3V)
JACKSNS.....-0.3V to +6.0V
Continuous Power Dissipation ($T_A$ = +70°C)
WLP (derate 23.8mW/°C above +70°C).....1.9W
TQFN (derate 35.7mW/°C above +70°C).....2.86W
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 1)

Junction-to-Case Thermal Resistance ($\theta_{JC}$)
TQFP .....1°C/W

Junction-to-Ambient Thermal Resistance ($\theta_{JA}$)
TQFP .....1°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to china.maximintegrated.com/thermal-tutorial.

## Electrical Characteristics

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| Supply Voltage Range | | Guaranteed by PSRR (Note 3) | $V_{SPKLVDD}$, $V_{SPKVDD}$, $V_{SPKRVDD}$ | 2.8 | 3.7 | 5.5 | V |
| | | | $V_{AVDD}$, $V_{HPVDD}$ | 1.65 | 1.8 | 2 | |
| | | | $V_{DVDD}$ | 1.08 | 1.2 | 1.98 | |
| | | | $V_{DVDDIO}$ | 1.65 | 1.8 | 3.6 | |
| Total Supply Current (Note 4) | $I_{VDD}$ | Full-duplex 8kHz mono, receiver output | Analog | | 1.94 | 3.5 | mA |
| | | | Speaker | | 0.73 | 2 | |
| | | | Digital | | 0.97 | 1.2 | |
| | | DAC playback 48kHz stereo, headphone outputs | Analog | | 1.45 | 2 | |
| | | | Speaker | | 0 | 0.005 | |
| | | | Digital | | 1.04 | 1.3 | |
| | | DAC playback 48kHz stereo, speaker outputs | Analog | | 0.91 | 2.4 | |
| | | | Speaker | | 2.18 | 3 | |
| | | | Digital | | 1.05 | 1.3 | |

## Electrical Characteristics (continued)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, AV_RCV = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| REF Voltage | | | | | 1.25 | | V |
| BIAS Voltage | | BIAS from resistive division (BIAS_MODE = 0) | | | 0.90 | | V |
| | | BIAS from bandgap (BIAS_MODE = 1) | | | 0.78 | | |
| Shutdown Supply Current (Note 4) | | $T_A$ = +25°C | Analog | | 1 | 10 | µA |
| | | | Speaker | | 1 | 5 | |
| | | | Digital | | 2.1 | 20 | |
| Shutdown to Full Operation | | | | | 10 | | ms |
| **DIFFERENTIAL INPUT (ANALOG MICROPHONE) TO ADC RECORD PATH** | | | | | | | |
| Dynamic Range (Note 5) | DR | $f_S$ = 48kHz, MODE = 1 (FIR audio), A-weighting filter applied | | | 97 | | dB |
| | | $f_S$ = 8kHz, MODE = 0 (IIR voice), A-weighting filter applied | | 90 | 96 | | dB |
| Total Harmonic Distortion + Noise | THD+N | $A_{V\_MICPRE}$ = 20dB, $V_{IN}$ = 90$mV_{RMS}$, f = 1kHz, | | | -82 | -75 | dB |
| | | $A_{V\_MICPRE}$ = 0dB, $V_{IN}$ = 900$mV_{RMS}$, f = 1kHz | | | -91 | | |
| | | $A_{V\_MICPRE}$ = 30dB, $V_{IN}$ = 28.5$mV_{RMS}$, f = 1kHz | | | -73 | | |
| Common-Mode Rejection Ratio | CMRR | f = 217Hz, $V_{IN\_CM}$ = 100$mV_{P-P}$ | | | 59 | | dB |
| Power-Supply Rejection Ratio (Note 3) | PSRR | $V_{AVDD}$ = 1.65V to 2.0V, input referred | | 40 | 57 | | dB |
| | | $V_{RIPPLE}$ = 100$mV_{P-P}$, input referred | f = 217Hz | | 78 | | |
| | | | f = 1kHz | | 78 | | |
| | | | f = 10kHz | | 77 | | |
| Path Phase Delay | | 1kHz, 0dB input, highpass filter disabled measured from analog input to digital output | MODE = 0 (voice) 8kHz | | 2.2 | | ms |
| | | | MODE = 0 (voice) 16kHz | | 1.1 | | |
| | | | MODE = 1 (music) 8kHz | | 4.5 | | |
| | | | MODE = 1 (music) 48kHz | | 0.8 | | |

## Electrical Characteristics (continued)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, AV_RCV = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Gain Error | | DC accuracy | | | 1 | 6.2 | % |
| **DIFFERENTIAL (ANALOG MICROPHONE) PREAMP and PGA** | | | | | | | |
| Full-Scale Input | | $A_{V\_MICPRE}$ = 0dB | | | 1 | | $V_{RMS}$ |
| Microphone Preamplifier Gain | $A_{V\_MICPRE}$ | (Note 6) | PA_EN[1:0] = 01 | | 0 | | dB |
| | | | PA_EN[1:0] = 10 | 19 | 20 | 21 | |
| | | | PA_EN[1:0] = 11 | 29 | 30 | 31 | |
| Microphone Level Adjust Gain (PGA) | $A_{V\_MICPGA}$ | (Note 6) | PGAM_[4:0] = 0x00 | 19 | 20 | 21 | dB |
| | | | PGAM_[4:0] = 0x14 | | 0 | | |
| MIC Input Resistance | $R_{IN\_MIC}$ | All gain settings, measured at IN_ (measured single-ended) | | 28 | 50 | | kΩ |
| **MICROPHONE BIAS** | | | | | | | |
| MICBIAS Output Voltage | $V_{MICBIAS}$ | $I_{LOAD}$ = 1mA, MBVSEL[1:0] = 00 | | 2.1 | 2.2 | 2.3 | V |
| | | $I_{LOAD}$ = 1mA, MBVSEL[1:0] = 01 | | 2.3 | 2.4 | 2.5 | |
| | | $I_{LOAD}$ = 1mA, MBVSEL[1:0] = 10 | | 2.475 | 2.57 | 2.7 | |
| | | $I_{LOAD}$ = 1mA, MBVSEL[1:0] = 11 | | 2.7 | 2.8 | 2.9 | |
| Load Regulation | | $I_{LOAD}$ = 1mA to 2mA, MBVSEL[1:0] = 00 | WLP | | ±0.085 | ±0.5 | mV |
| | | | TQFN | | ±0.085 | ±0.75 | |
| Line Regulation | | $V_{SPKLVDD}$ = 2.8V to 5.5V, MBVSEL[1:0] = 00 | | | ±0.01 | ±1 | mV |
| Ripple Rejection | | f = 217Hz, $V_{RIPPLE\ (SPKLVDD)}$ = $100mV_{P-P}$ | | | 70 | | dB |
| | | f = 10kHz, $V_{RIPPLE\ (SPKLVDD)}$ = $100mV_{P-P}$ | | | 75 | | |
| Noise Voltage | | A-weighted, f = 20Hz to 20kHz | | | 7.4 | | $\mu V_{RMS}$ |
| | | f = 1kHz | | | 52.3 | | $nV/\sqrt{Hz}$ |
| **SINGLE-ENDED (LINE) INPUT TO ADC PATH** | | | | | | | |
| Dynamic Range (Note 5) | DR | $f_S$ = 48kHz, $f_{MCLK}$ = 12.288MHz, MODE = 1 (FIR audio) | | | 98 | | dB |
| Total Harmonic Distortion + Noise | THD+N | $V_{IN}$ = $0.222V_{RMS}$, f = 1kHz | | | -85 | -80 | dB |
| **SINGLE-ENDED (LINE) INPUT PGA** | | | | | | | |
| Full-Scale Input | $V_{IN}$ | | | | 0.5 | | $V_{RMS}$ |
| | | $A_{V\_EXTERNAL}$ = -6dB, EXTBUF = 1 | | | 1 | | |

## Electrical Characteristics (continued)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, AV_RCV = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Line Input Level Adjust Gain (PGA) | $A_{V\_LINEPGA}$ | (Note 6) | PGALIN = 0x0 | 18 | 20 | 21.5 | dB |
| | | | PGALIN = 0x1 | 13 | 14 | 15 | |
| | | | PGALIN = 0x2 | 2 | 3 | 4 | |
| | | | PGALIN = 0x3 | -1 | 0 | +1 | |
| | | | PGALIN = 0x4 | -4 | -3 | -2 | |
| | | | PGALIN = 0x5, 0x6, 0x7 | -7 | -6 | -5 | |
| Line Input Amplifier Gain | $A_{V\_LINEAMP}$ | Single-ended only | | | 6 | | dB |
| Input Resistance | $R_{IN}$ | | | 14 | 20 | | kΩ |
| Feedback Resistance | $R_{IN\_FB}$ | $T_A$ = +25°C | | 19 | 20 | 21 | kΩ |
| **DIGITAL LOOP-THROUGH: RECORD OUTPUT TO PLAYBACK INPUT PATH** | | | | | | | |
| Dynamic Range (Note 5) | DR | $f_S$ = 48kHz, $f_{MCLK}$ = 12.288MHz, MODE = 1 (FIR audio) | | | 97 | | dB |
| Total Harmonic Distortion + Noise | THD+N | $f_{IN}$ = 1kHz, $f_S$ = 48kHz, $f_{MCLK}$ = 12.288MHz, MODE = 1 (FIR audio) | | | -83 | -72 | dB |
| **DAC PLAYBACK PATH TO RECEIVER AMPLIFIER PATH** | | | | | | | |
| Dynamic Range (Note 5) | DR | $f_S$ = 48kHz, $f_{MCLK}$ = 12.288MHz | | | 100 | | dB |
| Total Harmonic Distortion + Noise | THD+N | f = 1kHz, $P_{OUT}$ = 20mW, $R_{REC}$ = 32Ω | | | -68 | -58 | dB |
| **DIFFERENTIAL ANALOG INPUT TO RECEIVER AMPLIFIER PATH** | | | | | | | |
| Dynamic Range (Note 5) | DR | | | 90 | 96 | | dB |
| Total Harmonic Distortion + Noise | THD+N | | | | -71 | | dB |
| Power-Supply Rejection Ratio (Note 3) | PSRR | $V_{SPKLVDD}$ = 2.8V to 5.5V | | 68.4 | 80 | | dB |
| | | $V_{RIPPLE}$ = 100$mV_{P-P}$ | f = 217Hz | | 77 | | |
| | | | f = 1kHz | | 77 | | |
| | | | f = 10kHz | | 69 | | |
| **RECEIVER AMPLIFIER (Note 7)** | | | | | | | |
| Output Power | $P_{OUT}$ | $R_{REC}$ = 32Ω, f = 1kHz, THD < 1%, BIAS_ MODE = 0 | | | 97 | | mW |
| | | $R_{REC}$ = 32Ω, f = 1kHz, THD < 1%, BIAS_ MODE = 1 | | | 74 | | |
| Full-Scale Output | | $A_{V\_RECPGA}$ = 0dB (Note 8) | | | 1 | | $V_{RMS}$ |
| Receiver Volume Control (PGA) | $A_{V\_RECPGA}$ | (Notes 6 and 9) | RCVLVOL = 0x00 | -63 | -61 | -59.5 | dB |
| | | | RCVLVOL = 0x1F | +7.2 | +8 | +8.75 | |

## Electrical Characteristics (continued)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, AV_RCV = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Volume Control Step Size (Note 9) | | +8dB to +6dB | | | 0.5 | | dB |
| | | +6dB to +0dB | | | 1 | | |
| | | 0dB to -14dB | | | 2 | | |
| | | -14dB to -38dB | | | 3 | | |
| | | -38dB to -62dB | | | 4 | | |
| Mute Attenuation | | f = 1kHz | | 87 | 97 | | dB |
| Output Offset Voltage | $V_{OS}$ | $A_{V\_REC}$ = -62dB, $T_A$ = +25°C | | | | ±3 | mV |
| Click-and-Pop Level | $K_{CP}$ | Peak voltage, A-weighted, 32 samples per second, $A_{V\_REC}$ = 0dB | Into shutdown | | -67 | | dBV |
| | | | Out of shutdown | | -68 | | |
| Capacitive Drive Capability | | No sustained oscillations | $R_L$ = 32Ω | | 500 | | pF |
| | | | $R_L$ = ∞ | | 100 | | |
| **DAC PLAYBACK PATH TO LINEOUT AMPLIFIER PATH** | | | | | | | |
| Dynamic Range (Note 5) | DR | $f_S$ = 48kHz, $f_{MCLK}$ = 12.288MHz | | | 100 | | dB |
| Total Harmonic Distortion + Noise | THD+N | f = 1kHz, $R_{LOUT}$ = 10kΩ ($0.5V_{RMS}$ output level) | | | -86 | -70 | dB |
| **SINGLE-ENDED ANALOG INPUT TO LINE OUT AMPLIFIER PATH** | | | | | | | |
| Dynamic Range (Note 5) | DR | | | | 98 | | dB |
| Total Harmonic Distortion + Noise | THD+N | f = 1kHz, $R_{LOUT}$ = 10kΩ ($0.5V_{RMS}$ output level) | | | -86 | | dB |
| Power-Supply Rejection Ratio (Note 3) | PSRR | $V_{SPK\_VDD}$ = 2.8V to 5.5V | | 60 | 74 | | dB |
| | | $V_{RIPPLE}$ = $100mV_{P-P}$ | f = 217Hz | | 74 | | |
| | | | f = 1kHz | | 74 | | |
| | | | f = 10kHz | | 73 | | |
| **LINE OUT AMPLIFIER (Note 7)** | | | | | | | |
| Full-Scale Output | | (Note 8) | | | 0.707 | | $V_{RMS}$ |
| Line Output Amplifier Gain | $A_{V\_LOUTAMP}$ | | | | -3 | | dB |

## Electrical Characteristics (continued)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, AV_RCV = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Line Output Volume Control (PGA) | $A_{V\_LOUTPGA}$ | (Notes 6 and 9) | RCV_VOL = 0x00 | -63 | -61 | -59.5 | dB |
| | | | RCV_VOL = 0x1F | +7.2 | +8 | +8.75 | |
| Volume Control Step Size (Note 9) | | 8dB to 6dB | | | 0.5 | | dB |
| | | 6dB to 0dB | | | 1 | | |
| | | 0dB to -14dB | | | 2 | | |
| | | -14dB to -38dB | | | 3 | | |
| | | -38dB to -62dB | | | 4 | | |
| Mute Attenuation | | f = 1kHz | | 87 | 97 | | dB |
| Capacitive Drive Capability | | No sustained oscillations | $R_{LOUT}$ = 1kΩ | | 500 | | pF |
| | | | $R_{LOUT}$ = ∞ | | 100 | | |
| **DAC PLAYBACK PATH TO SPEAKER AMPLIFIER PATH** | | | | | | | |
| Dynamic Range (Note 5) | DR | | | | 91 | | dB |
| Total Harmonic Distortion + Noise | THD+N | f = 1kHz, $P_{OUT}$ = 200mW, $Z_{SPK}$ = 8Ω + 68µH, $f_{MCLK}$ = 12.288MHz | | | -73 | | dB |
| Crosstalk | | SPKL to SPKR and SPKR to SPKL, $P_{OUT}$ = 640mW, f = 1kHz | | | -104 | | dB |
| Output Noise | | | | | 27 | | $µV_{RMS}$ |
| **DIFFERENTIAL ANALOG INPUT TO SPEAKER AMPLIFIER PATH** | | | | | | | |
| Dynamic Range (Note 5) | DR | Output referenced to $2V_{RMS}$ | | | 91 | | dB |
| Total Harmonic Distortion + Noise | THD+N | f = 1kHz, $P_{OUT}$ = 200mW, $Z_{SPK}$ = 8Ω + 68µH | | | -73 | | dB |
| Output Noise | | | | | 28 | | $µV_{RMS}$ |
| Power-Supply Rejection Ratio (Note 3) | PSRR | $V_{SPK\_VDD}$= 2.8V to 5.5V | | 50 | 80 | | dB |
| | | $V_{RIPPLE}$ = $100mV_{P-P}$ | f = 217Hz | | 68 | | |
| | | | f = 1kHz | | 67 | | |
| | | | f = 10kHz | | 61 | | |

## Electrical Characteristics (continued)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, AV_RCV = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **SPEAKER AMPLIFIER (Note 7)** | | | | | | | |
| Output Power | $P_{OUT}$ | f = 1kHz, THD+N = 1%, $Z_{SPK}$ = 8Ω + 68µH, WLP package | $V_{SPK\_VDD}$ = 5.0V | | 1400 | | mW |
| | | | $V_{SPK\_VDD}$ = 4.2V | | 1000 | | |
| | | | $V_{SPK\_VDD}$ = 3.7V | | 780 | | |
| | | | $V_{SPK\_VDD}$ = 3.3V | | 600 | | |
| | | | $V_{SPK\_VDD}$ = 3.0V | | 500 | | |
| | | f = 1kHz, THD+N = 10%, $Z_{SPK}$ = 8Ω + 68µH, WLP package | $V_{SPK\_VDD}$ = 5.0V | | 1800 | | |
| | | | $V_{SPK\_VDD}$ = 4.2V | | 1250 | | |
| | | | $V_{SPK\_VDD}$ = 3.7V | | 970 | | |
| | | | $V_{SPK\_VDD}$ = 3.3V | | 760 | | |
| | | | $V_{SPK\_VDD}$ = 3.0V | | 620 | | |
| Output Power | $P_{OUT}$ | f = 1kHz, THD+N = 1%, $Z_{SPK}$ = 4Ω + 33µH, WLP package | $V_{SPK\_VDD}$ = 5.0V | | 2600 | | mW |
| | | | $V_{SPK\_VDD}$ = 4.2V | | 1800 | | |
| | | | $V_{SPK\_VDD}$ = 3.7V | | 1400 | | |
| | | | $V_{SPK\_VDD}$ = 3.3V | | 1050 | | |
| | | | $V_{SPK\_VDD}$ = 3.0V | | 850 | | |
| | | f = 1kHz, THD+N = 10%, $Z_{SPK}$ = 4Ω + 33µH, WLP package | $V_{SPK\_VDD}$ = 5.0V | | 3200 | | |
| | | | $V_{SPK\_VDD}$ = 4.2V | | 2200 | | |
| | | | $V_{SPK\_VDD}$ = 3.7V | | 1700 | | |
| | | | $V_{SPK\_VDD}$ = 3.3V | | 1350 | | |
| | | | $V_{SPK\_VDD}$ = 3.0V | | 1100 | | |
| Full-Scale Output | | $A_{V\_SPK}$ = +6dB (Note 8) | | | 2 | | $V_{RMS}$ |
| Speaker Output Amplifier Gain | $A_{V\_SPKAMP}$ | | | | +6 | | dB |
| Speaker Volume Control (PGA) | $A_{V\_SPKPGA}$ | (Notes 6 and 9) | SPVOLL = 0x00 | -51 | -48 | -44.5 | dB |
| | | | SPVOLR = 0x1F | 13 | 14 | 15 | |
| Volume Control Step Size (Note 9) | | 14dB to 9dB | | | 0.5 | | dB |
| | | +9dB to -6dB | | | 1 | | |
| | | -6dB to -14dB | | | 2 | | |
| | | -14dB to -32dB | | | 3 | | |
| | | -32dB to -48dB | | | 4 | | |
| Mute Attenuation | | f = 1kHz | | 76 | 84 | | dB |

## Electrical Characteristics (continued)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, AV_RCV = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Offset Voltage | $V_{OS}$ | $A_{V\_SPKPGA}$ = -62dB, $T_A$ = +25°C | | | ±0.5 | ±4 | mV |
| Click-and-Pop Level | $K_{CP}$ | Peak voltage, A-weighted, 32 samples per second, $A_{V\_SPK}$ = 0dB | Into shutdown | | -65 | | dBV |
| | | | Out of shutdown | | -65 | | |
| **DAC PLAYBACK PATH TO HEADPHONE AMPLIFIER PATH** | | | | | | | |
| Dynamic Range (Note 5) | DR | $f_S$ = 48kHz, $f_{MCLK}$ = 12.288MHz | Master or slave mode | | 102 | | dB |
| | | | Slave mode | 94 | | | |
| Total Harmonic Distortion + Noise | THD+N | f = 1kHz, $P_{OUT}$ = 10mW | $R_{HP}$ = 16Ω | | -86 | -77 | dB |
| | | | $R_{HP}$ = 32Ω | | -88 | | |
| | | f = 1kHz, $V_{OUT}$ = $1V_{RMS}$, $R_{HP}$ = 10kΩ | | | -88 | | |
| Crosstalk | | f = 1kHz, $V_{IN}$ = -1dBFS, $R_{HP}$ = 10kΩ | | | -105 | | dB |
| | | HPL to HPR and HPR to HPL, $P_{OUT}$ = 5mW, f = 1kHz, $R_{HP}$ = 32Ω | | | -104 | | dB |
| Power-Supply Rejection Ratio (Note 3) | PSRR | $V_{AVDD}$ = $V_{HPVDD}$ = 1.65V to 2.0V | | 70 | 80 | | dB |
| | | $V_{RIPPLE}$ = $100mV_{P-P}$, $A_{V\_HP}$ = 0dB | f = 217Hz | | 79 | | |
| | | | f = 1kHz | | 79 | | |
| | | | f = 10kHz | | 74 | | |
| DAC Path Phase Delay | | 1kHz, 0dB input, highpass filter disabled measured from digital input to analog output | MODE = 0 (voice) 8kHz | | 2.2 | | ms |
| | | | MODE = 0 (voice) 16kHz | | 1.1 | | |
| | | | MODE = 1 (music) 8kHz | | 4.5 | | |
| | | | MODE = 1 (music) 48kHz | | 0.76 | | |
| Gain Error | | | | | 1 | 5 | % |
| Channel Gain Mismatch | | | | | 1 | | % |
| **SINGLE-ENDED ANALOG INPUT TO HEADPHONE AMPLIFIER PATH** | | | | | | | |
| Dynamic Range (Note 5) | | $A_{V\_LINE}$ = 0dB $A_{V\_HPPGA}$ = 0 dB | | | 101 | | dB |
| Total Harmonic Distortion + Noise | THD+N | $V_{IN}$ = $250mV_{RMS}$, f =1kHz | | | -80 | | dB |
| Crosstalk | | HPL to HPR and HPR to HPL, $P_{OUT}$ = 5mW, f = 1kHz, $R_{HP}$ = 32Ω | | | -94 | | dB |

## Electrical Characteristics (continued)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, AV_RCV = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Power-Supply Rejection Ratio (Note 3) | PSRR | $V_{AVDD}$ = $V_{HPVDD}$ = 1.65V to 2.0V | | 40 | 60 | | dB |
| | | $V_{RIPPLE}$ = 100m$V_{P-P}$, $A_{V\_TOTAL}$ = 0dB | f = 217Hz | | 61 | | |
| | | | f = 1kHz | | 61 | | |
| | | | f = 10kHz | | 60 | | |
| **HEADPHONE AMPLIFIER (Note 7)** | | | | | | | |
| Output Power | $P_{OUT}$ | f = 1kHz, THD = 1% | $R_{HP}$ = 16Ω | 20 | 40 | | mW |
| | | | $R_{HP}$ = 32Ω | | 30 | | |
| Total Harmonic Distortion + Noise | THD+N | $R_{HP}$ = 16Ω, $P_{OUT}$ = 10mW, f = 1kHz | | | -88 | -77 | dB |
| | | $R_{HP}$ = 10kΩ, $V_{OUT}$ = 1$V_{RMS}$, f = 1kHz | | | -88 | | |
| Full-Scale Output | | $A_{VHP}$ = 0dB (Note 8) | | | 1 | | $V_{RMS}$ |
| Headphone Volume Control (PGA) | $A_{V\_HPPGA}$ | | HPVOL_ = 0x00 | -69 | -67 | -65 | dB |
| | | | HPVOL_ = 0x1F | 2.5 | 3 | 3.5 | |
| Volume Control Step Size (Note 9) | | +3dB to +1dB | | | 0.5 | | dB |
| | | +1dB to -5dB | | | 1 | | |
| | | -5dB to -19dB | | | 2 | | |
| | | -19dB to -43dB | | | 3 | | |
| | | -43dB to -67dB | | | 4 | | |
| Mute Attenuation | | f = 1kHz | | | 110 | | dB |
| Output Offset Voltage | $V_{OS}$ | AV_HP = -67dB | $T_A$ = +25°C | | ±0.5 | ±1 | mV |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±3 | |
| Capacitive Drive Capability | | No sustained oscillations | $R_{HP}$ = 32Ω | | 500 | | pF |
| | | | $R_{HP}$ = ∞ | | 100 | | |
| Click-and-Pop Level | $K_{CP}$ | Peak voltage, A-weighted, 32 samples per second, $A_{V\_HP}$ = -67dB | Into shutdown | | -73 | | dBV |
| | | | Out of shutdown | | -73 | | |
| **JACK DETECTION** | | | | | | | |
| JACKSNS High Threshold | $V_{TH\_HIGH}$ | MICBIAS enabled | | 0.80 x $V_{MICBIAS}$ | 0.95 x $V_{MICBIAS}$ | 0.98 x $V_{MICBIAS}$ | V |
| | | MICBIAS disabled | | 0.80 x $V_{SPKLVDD}$ | 0.95 x $V_{SPKLVDD}$ | 0.98 x $V_{SPKLVDD}$ | |

## Electrical Characteristics (continued)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, AV_RCV = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| JACKSNS Low Threshold | $V_{TH\_LOW}$ | MICBIAS enabled | 0.06 x $V_{MICBIAS}$ | 0.10 x $V_{MICBIAS}$ | 0.17 x $V_{MICBIAS}$ | V |
| | | MICBIAS disabled | 0.06 x $V_{SPKLVDD}$ | 0.10 x $V_{SPKLVDD}$ | 0.17 x $V_{SPKLVDD}$ | |
| JACKSNS Sense Voltage | $V_{SENSE}$ | MICBIAS disabled | | $V_{SPKLVDD}$ | | V |
| JACKSNS Strong Pullup Resistance | $R_{SPU}$ | MICBIAS disabled, JDWK = 0 | 1.9 | 2.4 | 2.7 | kΩ |
| JACKSNS Weak Pullup Current | $I_{WPU}$ | MICBIAS disabled, JDWK = 1 | | 5 | 12 | µA |
| JACKSNS Glitch Debounce Period | $t_{GLITCH}$ | JDEB = 00 | | 25 | | ms |
| | | JDEB = 11 | | 200 | | |

## 数字滤波器规格

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$= 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line Output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 10)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **RECORD PATH LEVEL CONTROL** | | | | | | |
| Record Level Adjust Range | $A_{V\_ADCLVL}$ | AVL/AVR = 0xF to 0x0 (Note 6) | -12 | | +3 | dB |
| Record Level Adjust Step Size | | | | 1 | | dB |
| Record Gain Adjust Range | $A_{V\_ADCGAIN}$ | AVLG/AVRG = 0x0 to 0x3 (Note 6) | 0 | | 42 | dB |
| Record Gain Adjust Step Size | | | | 6 | | dB |
| **RECORD PATH VOICE MODE IIR LOWPASS FILTER (MODE = 0)** | | | | | | |
| Passband Cutoff | $f_{PLP}$ | Ripple limit cutoff | 0.444 x $f_S$ | | | Hz |
| | | -3dB cutoff | 0.449 x $f_S$ | | | |
| Passband Ripple | | $f < f_{PLP}$ | -0.1 | | 0.1 | dB |
| Stopband Cutoff | $f_{SLP}$ | | | | 0.47 x $f_S$ | Hz |
| Stopband Attenuation | | $f > f_{SLP}$ | 74 | | | dB |
| **RECORD PATH STEREO MUSIC MODE FIR LOWPASS FILTER (MODE = 1, DHF = 0, $f_{LRCLK}$ < 50kHz)** | | | | | | |
| Passband Cutoff | $f_{PLP}$ | Ripple limit cutoff | 0.43 x $f_S$ | | | Hz |
| | | -3dB cutoff | 0.48 x $f_S$ | | | |
| | | -6.02dB cutoff | 0.5 x $f_S$ | | | |
| Passband Ripple | | $f < f_{PLP}$ | -0.1 | | +0.1 | dB |
| Stopband Cutoff | $f_{SLP}$ | | | | 0.58 x $f_S$ | Hz |
| Stopband Attenuation | | $f < f_{SLP}$ | 60 | | | dB |
| **RECORD PATH STEREO MUSIC MODE FIR LOWPASS FILTER (MODE = 1, DHF = 1, $f_{LRCLK}$ > 50kHz)** | | | | | | |
| Passband Cutoff | $f_{PLP}$ | Ripple Limit cutoff | 0.208 x $f_S$ | | | Hz |
| | | -3dB cutoff | 0.28 x $f_S$ | | | |
| Passband Ripple | | $f < f_{PLP}$ | -0.1 | | +0.1 | dB |
| Stopband Cutoff | $f_{SLP}$ | | | | 0.45 x $f_S$ | Hz |
| Stopband Attenuation | | $f < f_{SLP}$ | 60 | | | dB |

## 数字滤波器规格(续)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$= 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line Output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 10)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **RECORD PATH DC-BLOCKING HIGHPASS FILTER** | | | | | | | |
| DC Attenuation | $A_{V\_ADCHPF}$ | AHPF = 1 | | | 90 | | dB |
| **RECORD PATH PROGRAMMALE BIQUAD FILTER** | | | | | | | |
| Preattenuator Gain Range | | | | -15 | | 0 | dB |
| Preattenuator Step Size | | | | | 1 | | dB |
| Cutoff Frequency | | Highpass filter | | 0.0008 x $f_S$ | | | Hz |
| | | High-frequency shelving filter | | 0.02 x $f_S$ | | | |
| | | Lowpass filter | | 0.002 x $f_S$ | | | |
| | | Low-frequency shelving filter | | 0.0008 x $f_S$ | | | |
| | | Peak filter | | 0.0008 x $f_S$ | | | |
| Quality Factor | Q | Peak filter | | | | 10 | |
| **DIGITAL SIDETONE: RECORD PATH TO PLAYBACK PATH (MODE = 0)** | | | | | | | |
| Sidetone Level Adjust Range | $A_{V\_STLVL}$ | DVST = 0x1F to 0x01 | | -60.5 | | -0.5 | dB |
| Sidetone Level Adjust Step Side | | | | | 2 | | dB |
| Sidetone Path Phase Delay | | $f_{IN}$ = 1kHz, full-scale amplitude, highpass filter disabled | $f_S$ = 8kHz | | 1.8 | | ms |
| | | | $f_S$ = 16kHz | | 0.9 | | |
| **PLAYBACK PATH LEVEL CONTROL** | | | | | | | |
| Playback Path Attenuation Range | $A_{V\_DACLVL}$ | DV = 0xF to 0x0 (Note 6) | | -15 | | 0 | dB |
| Playback Path Attenuation Step Size | | | | | 1 | | dB |
| Playback Path Gain Adjust Range | $A_{V\_DACGAIN}$ | DVG = 00 to 11 (Note 6) | | 0 | | 18 | dB |

## 数字滤波器规格(续)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$= 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line Output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 10)

| | | | | | | |
|---|---|---|---|---|---|---|
| Playback Path Gain Adjust Step Size | | | | 6 | | dB |
| **PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **PLAYBACK PATH VOICE MODE IIR LOWPASS FILTER (MODE = 0)** | | | | | | |
| Passband Cutoff | $f_{PLP}$ | Ripple limit cutoff | | 0.448 x $f_S$ | | Hz |
| | | -3dB cutoff | | 0.451 x $f_S$ | | |
| Passband Ripple | | f < $f_{PLP}$ | -0.1 | | +0.1 | dB |
| Stopband Cutoff | $f_{SLP}$ | | | | 0.476 x $f_S$ | Hz |
| Stopband Attenuation (Note 11) | | f > $f_{SLP}$ | 75 | | | dB |
| **PLAYBACK PATH STEREO MUSIC MODE FIR LOWPASS FILTER (MODE = 1, DHF = 0, $f_{LRCLK}$ < 50kHz)** | | | | | | |
| Passband Cutoff | $f_{PLP}$ | Ripple limit cutoff | | 0.43 x $f_S$ | | Hz |
| | | -3dB cutoff | | 0.47 x $f_S$ | | |
| | | -6.02dB cutoff | | 0.5 x $f_S$ | | |
| Passband Ripple | | f < $f_{PLP}$ | -0.1 | | +0.1 | dB |
| Stopband Cutoff | $f_{SLP}$ | | | | 0.58 x $f_S$ | Hz |
| Stopband Attenuation (Note 11) | | f > $f_{SLP}$ | 60 | | | dB |
| **PLAYBACK PATH STEREO MUSIC MODE FIR LOWPASS FILTER (MODE1 = 1, DHF = 1 for $f_{LRCLK}$ > 50kHz)** | | | | | | |
| Passband Cutoff | $f_{PLP}$ | Ripple limit cutoff | | 0.24 x $f_S$ | | Hz |
| | | -3dB cutoff | | 0.31 x $f_S$ | | |
| Passband Ripple | | f < $f_{PLP}$ | -0.1 | | +0.1 | dB |
| Stopband Cutoff | $f_{SLP}$ | | | | 0.477 x $f_S$ | Hz |
| Stopband Attenuation (Note 11) | | f < $f_{SLP}$ | 60 | | | dB |

## 数字滤波器规格(续)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$= 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line Output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 10)

| **PLAYBACK PATH DC-BLOCKING HIGHPASS FILTER** | | | | | | |
|---|---|---|---|---|---|---|
| DC Attenuation | | DHPF = 1 | | 89 | | dB |
| **PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **PLAYBACK PATH DYNAMIC RANGE CONTROL** | | | | | | |
| Gain Range | | | 0 | | 12 | dB |
| Compression Threshold | | | -31 | | 0 | dBFS |
| Expansion Threshold | | | -66 | | -35 | dBFS |
| Attack Time | | | 0.0005 | | 0.2 | s |
| Release Time | | | 0.0625 | | 8 | s |
| **PLAYBACK PATH PARAMETRIC EQUALIZER** | | | | | | |
| Number of Bands | | | | 7 | | Bands |
| Per Band Gain Range | | | -12 | | +12 | dB |
| Preattenuator Gain Range | | | -15 | | 0 | dB |
| Preattenuator Step Size | | | | 1 | | dB |
| Cutoff Frequency | | Highpass filter | 0.0008 x $f_S$ | | | Hz |
| | | High-frequency shelving filter | 0.02 x $f_S$ | | | |
| | | Lowpass filter | 0.002 x $f_S$ | | | |
| | | Low-frequency shelving filter | 0.0008 x $f_S$ | | | |
| | | Peak filter | 0.0008 x $f_S$ | | | |
| Quality Factor | Q | Peak filter | | | 10 | |

## 数字输入/输出特性

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (RHP) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **MCLK** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 1.26 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.6 | V |
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $V_{DVDDIO}$ = 2.0V, $T_A$ = +25°C | -1 | | +1 | µA |
| Input Capacitance | | | | 10 | | pF |
| **SDIN, BCLK, LRCLK (Input)** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 0.7 x $V_{DVDDIO}$ | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.3 x $V_{DVDDIO}$ | V |
| Input Hysteresis | | | | 100 | | mV |
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $V_{DVDDIO}$ = 3.6V, $T_A$ = +25°C | -1 | | +1 | µA |
| Input Capacitance | | | | 10 | | pF |
| **BCLK, LRCLK, SDOUT (Output)** | | | | | | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = 3mA | $V_{DVDDIO}$ - 0.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 3mA | | | 0.4 | V |
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $V_{DVDDIO}$ = 2.0V, $T_A$ = +25°C, high-impedance state | -1 | | +1 | µA |
| **SDA, SCL (Input)** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 0.7 x $V_{DVDDIO}$ | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.3 x $V_{DVDDIO}$ | V |
| Input Hysteresis | | | | 100 | | mV |
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $V_{DVDDIO}$ = 2.0V, $T_A$ = +25°C | -1 | | +1 | µA |
| Input Capacitance | | | | 10 | | pF |
| **SDA, $\overline{IRQ}$ (Output)** | | | | | | |
| Output Low Voltage | $V_{OL}$ | $V_{DVDDIO}$ = 1.65V, $I_{OH}$ = 3mA | | | 0.2 x $V_{DVDDIO}$ | V |
| Output High Current | $I_{OH}$ | $V_{DVDDIO}$ = 1.65V, $I_{OL}$ = 3mA | | | 1 | µA |

## 数字输入/输出特性(续)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (RHP) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL MICROPHONE DATA (DMD) INPUT** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 0.65 x $V_{DVDDIO}$ | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.35 x $V_{DVDDIO}$ | V |
| Input Hysteresis | | | | 100 | | mV |
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $V_{DVDDIO}$ = 2.0V, $T_A$ = +25°C | -25 | | +25 | µA |
| Input Capacitance | | | | 10 | | pF |
| **DIGITAL MICROPHONE CLOCK (DMC) OUTPUT** | | | | | | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = 3mA | $V_{AVDD}$ - 0.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 3mA | | | 0.4 | V |

## 输入时钟特性

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$= 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, AV_RCV = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Notes 2, 10)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **INPUT CLOCK CHARACTERISTICS** | | | | | | | |
| MCLK Input Frequency | $f_{MCLK}$ | $f_S$ = 8kHz, voice mode filters (MODE = 0) | | 2.048 | | 60 | MHz |
| | | $f_S$ = 48kHz, music mode filters (MODE = 1) | | 10 | | 60 | |
| | | $f_S$ = 96kHz, music mode filters (MODE = 1) | | 12.288 | | 60 | |
| MCLK Input Duty Cycle | | PSCLK = 01 | | 40 | 50 | 60 | % |
| | | PSCLK = 10 or 11 | | 30 | | 70 | |
| Maximum MCLK Input Jitter | | | | | 1 | | ns |
| LRCLK Sample Rate (Note 12) | $f_{LRCLK}$ | DHF = 0 | | 8 | | 48 | kHz |
| | | DHF = 1 | | 48 | | 96 | |
| DAI LRCLK Average Frequency Error (Note 13) | | FREQ = 0x8 to 0xF | | 0 | | 0 | % |
| | | FREQ = 0x0 | | -0.025 | | +0.025 | |
| Minimum PCLK to LRCLK Frequency Ratio | | 8kHz ≤ $f_S$ ≤ 48kHz, voice mode filters (MODE = 0), DHF = 0 | OSR = 128 or 64 | 256 x $f_S$ | | | $f_{PCLK}$ |
| | | 8kHz ≤ $f_S$ ≤ 48kHz, music mode filters (MODE = 1), DHF = 0 | OSR = 128 | 256 x $f_S$ | | | |
| | | | OSR = 64 | 208 x $f_S$ | | | |
| | | 48kHz < $f_S$ ≤ 96kHz, music mode filters (MODE = 1), DHF = 1 | OSR = 64 | 128 x $f_S$ | | | |
| PLL Lock Time | | | | | 2 | 7 | ms |
| Maximum LRCLK Input Jitter to Maintain PLL Lock | | | | | | ±100 | ns |
| Soft-Start/Stop Time | | | | | 10 | | ms |

## 数字音频接口时序参数

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS** | | | | | | | |
| BCLK Cycle Time | $t_{BCLK}$ | Slave mode | | 80 | | | ns |
| BCLK High Time | $t_{BCLKH}$ | Slave mode | | 20 | | | ns |
| BCLK Low Time | $t_{BCLKL}$ | Slave mode | | 20 | | | ns |
| BCLK or LRCLK Rise and Fall Time | $t_r$, $t_f$ | Master mode, $C_L$ = 15pF | | | 5 | | ns |
| SDIN to BCLK Setup Time | $t_{SETUP}$ | | | 20 | | | ns |
| LRCLK to BCLK Setup Time | $t_{SYNCSET}$ | Slave mode | | 20 | | | ns |
| SDIN to BCLK Hold Time | $t_{HOLD}$ | | | 20 | | | ns |
| LRCLK to BCLK Hold Time | $t_{SYNCHOLD}$ | Slave mode | | 20 | | | ns |
| Minimum Delay Time from LSB BCLK Falling Edge to High-Impedance State | $t_{HIZOUT}$ | Master mode | TDM = 1 | | 20 | | ns |
| | | | TDM = 1, FSW = 1 | | 20 | | |
| | | | TDM = 1, FSW = 0 | | 20 | | |
| | | | TDM = 0, DLY = 1 | | 20 | | |
| LRCLK Rising Edge to SDOUT MSB Delay | $t_{SYNCTX}$ | C = 30pF, TDM = 1, FSW = 1 | | | | 40 | ns |
| BCLK to SDOUT Delay | $t_{CLKTX}$ | C = 30pF | TDM = 1, BCLK rising edge | | | 50 | ns |
| | | | TDM = 0 | | | 50 | |
| Delay Time from BCLK to LRCLK | $t_{CLKSYNC}$ | Master mode | TDM = 1 | -15 | | +15 | ns |
| | | | TDM = 0 | | | 0.8 x $t_{BCLK}$ | |

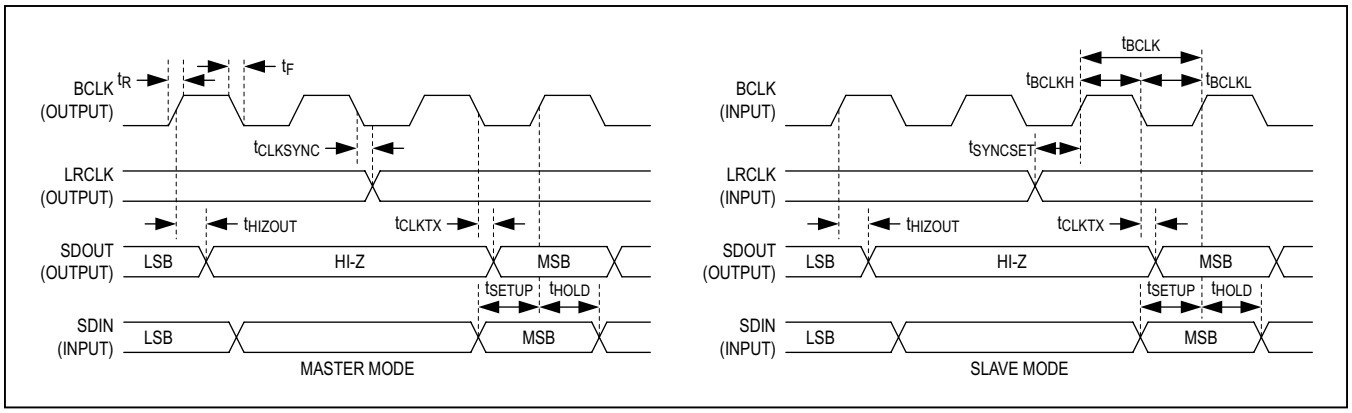



*图1. I²S音频接口时序图(TDM = 0)*

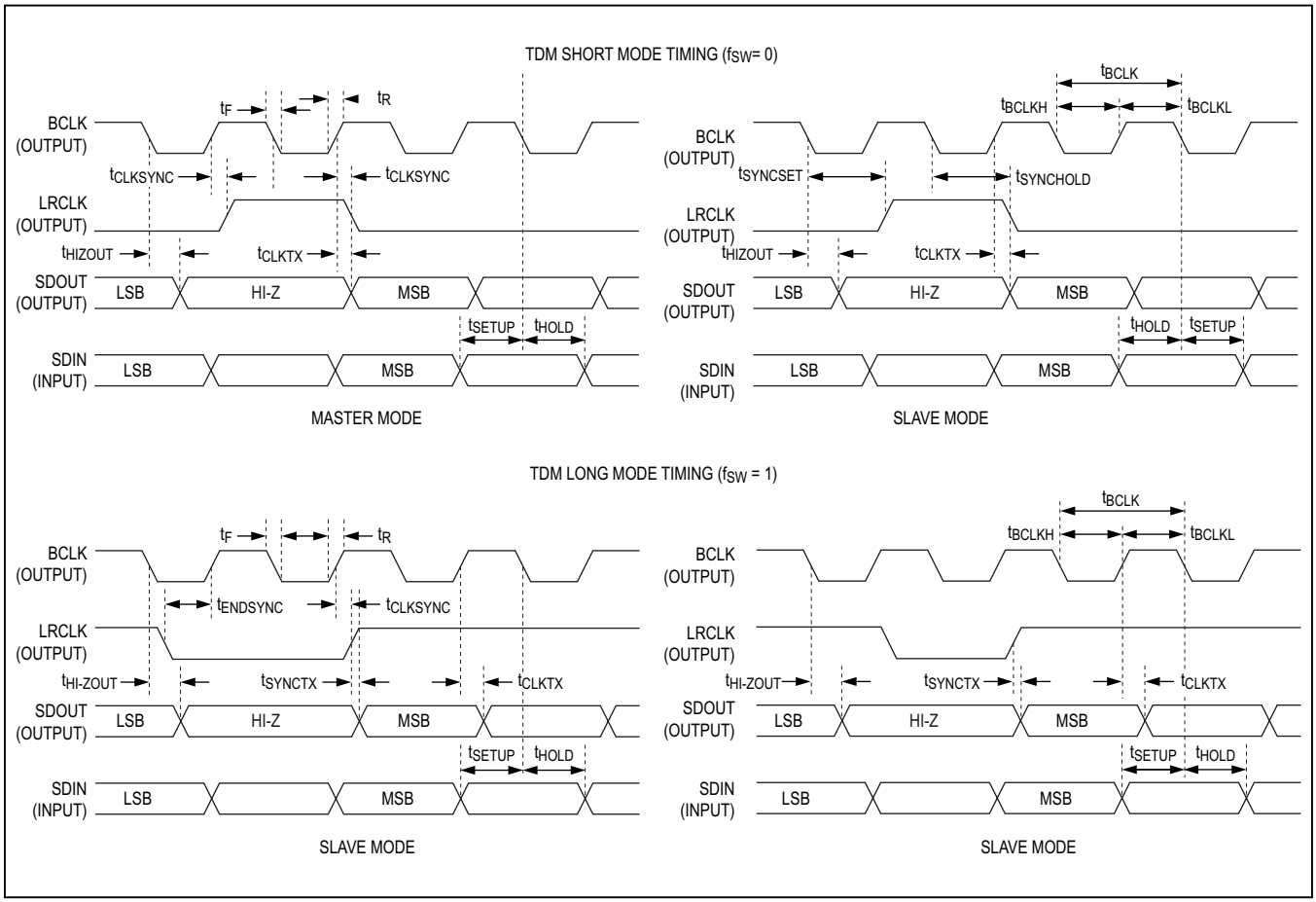



*图2. TDM音频接口短路模式时序图(TDM = 1，BCI = 1)*

## I²C时序参数

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads (RHP) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **I²C TIMING CHARACTERISTICS** | | | | | | |
| Serial Clock Frequency | $f_{SCL}$ | Guaranteed by SCL pulse width low and high | 0 | | 400 | kHz |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$ | | 1.3 | | | µs |
| Hold Time (Repeated) START Condition | $t_{HD,STA}$ | | 0.6 | | | µs |
| SCL Pulse-Width Low | $t_{LOW}$ | | 1.3 | | | µs |
| SCL Pulse-Width High | $t_{HIGH}$ | | 0.6 | | | µs |
| Setup Time for a Repeated START Condition | $t_{SU,STA}$ | | 0.6 | | | µs |
| Data Hold Time | $t_{HD,DAT}$ | $R_{PU}$ = 475Ω, $C_B$ = 100pF, 400pF | 0 | | 900 | ns |
| | | Transmitting | 0 | | 900 | |
| | | Receiving | | | 0 | |
| Data Setup Time | $t_{SU,DAT}$ | | 100 | | | ns |
| SDA and SCL Receiving Rise Time | $t_R$ | (Note 14) | 20 + 0.1 x $C_B$ | | 300 | ns |
| SDA and SCL Receiving Fall Time | $t_F$ | (Note 14) | 20 + 0.1 x $C_B$ | | 300 | ns |
| SDA Transmitting Fall Time | $t_F$ | $R_{PU}$ = 475Ω, $C_B$ = 100pF to 400pF (Note 14) | 20 + 0.1 x $C_B$ | | 250 | ns |
| Setup Time for STOP Condition | $t_{SU,STO}$ | | 0.6 | | | µs |
| Bus Capacitance | $C_B$ | Guaranteed by SDA transmitting fall time | | | 400 | pF |
| Pulse Width of Suppressed Spike | $t_{SP}$ | | 0 | | 50 | ns |

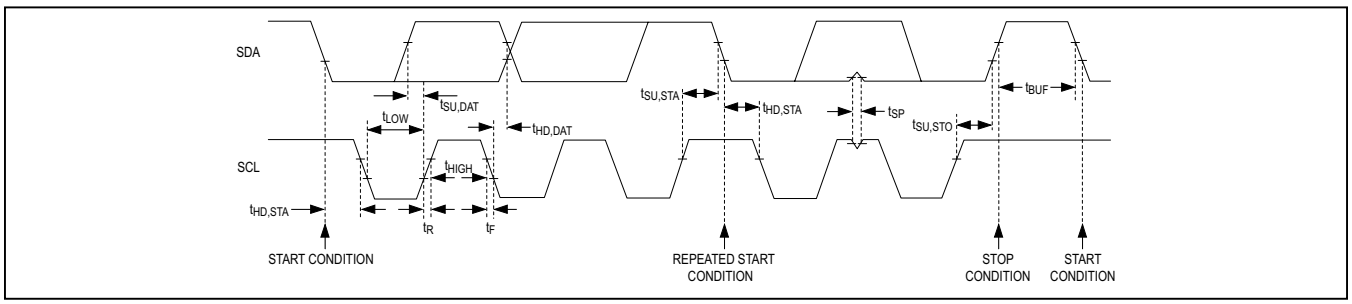



*图3. I²C接口时序图*

## 数字麦克风时序参数

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL MICROPHONE TIMING CHARACTERISTICS** | | | | | | |
| DMC Frequency | $f_{DMC}$ | MICCLK = 000 | | $f_{PCLK}/2$ | | MHz |
| | | MICCLK = 001 | | $f_{PCLK}/3$ | | |
| | | MICCLK = 010 | | $f_{PCLK}/4$ | | |
| | | MICCLK = 011 | | $f_{PCLK}/5$ | | |
| | | MICCLK = 100 | | $f_{PCLK}/6$ | | |
| | | MICCLK = 101 | | $f_{PCLK}/8$ | | |
| DMD to DMC Setup Time | $t_{SU,MIC}$ | Either clock edge | 20 | | | ns |
| DMD to DMC Hold Time | $t_{HD,MIC}$ | Either clock edge | 0 | | | ns |

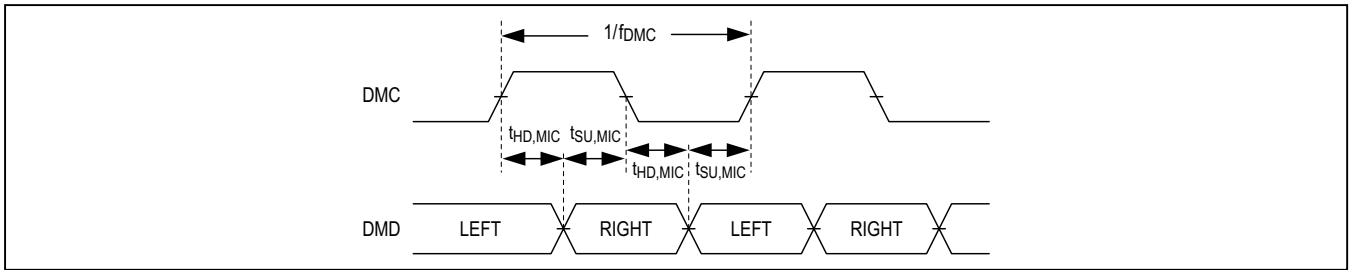



*图4. 数字麦克风时序图*

**Note 2:** The MAX98090 is 100% production tested at $T_A$ =+25°C. Specifications over temperature limits are guaranteed by design.
**Note 3:** BIAS derived from a bandgap reference (BIAS_MODE = 1).
**Note 4:** Analog supply current = AVDD + HPVDD, speaker supply current = SPKLVDD + SPKRVDD, and digital supply current = DVDD + DVDDIO.
**Note 5:** Dynamic range measurements are performed with the EIAJ method (a -60dBFS output signal at 1kHz, A-weighted and normalized to 0dBFS; f = 20Hz – 20kHz).
**Note 6:** Gain measured relative to the 0dB setting.
**Note 7:** Performance measured using DAC Inputs, unless otherwise stated.
**Note 8:** Full-scale analog output with 0dB of programmable gain, and a 0dBFS DAC input amplitude, a $1V_{RMS}$ differential analog input amplitude, or a $0.5V_{RMS}$ single-ended analog input amplitude.
**Note 9:** Performance measured using an analog input to amplifier output path.
**Note 10:** Digital filter performance is invariant over temperature and production tested at $T_A$ = +25°C.
**Note 11:** The filter specification is accurate only for synchronous clocking modes (integer MCLK to LRCLK ratio).
**Note 12:** $f_{LRCLK}$ may be any rate in the indicated range. Asynchronous and non-integer $f_{MCLK}/f_{LRCLK}$ ratios can exhibit some full-scale performance degradation compared to synchronous integer ratios.
**Note 13:** In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.
**Note 14:** $C_B$ is in pF.

## 静态功耗

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V, slave mode operation.)

| DEVICE MODE AND CONFIGURATION | $I_{AVDD}$ (mA) | $I_{HPVDD}$ (mA) | $I_{DVDD}$ (mA) | $I_{DVDDIO}$ (mA) | $I_{SPK\_VDD}$ (mA) | POWER (mW) | DYNAMIC RANGE (dB) |
|---|---|---|---|---|---|---|---|
| **DIGITAL AUDIO INPUT TO PLAYBACK PATH TO HEADPHONE OUTPUT (MUSIC FILTERS)** | | | | | | | |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, $R_{LOAD}$ = 32Ω | 1.39 | 1.28 | 1.04 | 0.02 | 0.00 | 6.05 | 102 |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, $R_{LOAD}$ = 32Ω, low power mode | 0.94 | 0.51 | 1.02 | 0.02 | 0.00 | 3.84 | 99 |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, $R_{LOAD}$ = 32Ω, dynamic range control enabled | 1.39 | 1.28 | 1.11 | 0.02 | 0.00 | 6.14 | 102 |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, $R_{LOAD}$ = 32Ω, parametric equalizer enabled | 1.39 | 1.28 | 1.65 | 0.02 | 0.00 | 6.78 | 102 |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 96kHz, 20-bit, music filters, $R_{LOAD}$ = 32Ω | 1.39 | 1.28 | 1.17 | 0.02 | 0.00 | 6.21 | 102 |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 13MHz, $f_S$ = 44.1kHz, 20-bit, music filters, $R_{LOAD}$ = 32Ω | 1.40 | 1.29 | 1.00 | 0.02 | 0.00 | 6.03 | 102 |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 13MHz, $f_S$ = 44.1kHz, 20-bit, music filters, $R_{LOAD}$ = 32Ω, low power mode | 0.96 | 0.51 | 1.00 | 0.02 | 0.00 | 3.85 | 99 |

## 静态功耗(续)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V, slave mode operation.)

| DEVICE MODE AND CONFIGURATION | $I_{AVDD}$ (mA) | $I_{HPVDD}$ (mA) | $I_{DVDD}$ (mA) | $I_{DVDDIO}$ (mA) | $I_{SPK\_VDD}$ (mA) | POWER (mW) | DYNAMIC RANGE (dB) |
|---|---|---|---|---|---|---|---|
| **DIGITAL AUDIO INPUT TO PLAYBACK PATH TO HEADPHONE OUTPUT (VOICE FILTERS)** | | | | | | | |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω | 1.35 | 1.28 | 0.89 | 0.02 | 0.00 | 5.81 | 101 |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω, low power mode | 0.91 | 0.51 | 0.89 | 0.02 | 0.00 | 3.62 | 98.5 |
| **Mono DAC Playback to Headphone Output** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω | 0.78 | 0.69 | 0.82 | 0.02 | 0.00 | 3.64 | 101 |
| **Mono DAC Playback to Headphone Output** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω, low power mode | 0.56 | 0.30 | 0.82 | 0.02 | 0.00 | 2.55 | 98.5 |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 13MHz, $f_S$ = 16kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω | 1.35 | 1.28 | 0.94 | 0.02 | 0.00 | 5.87 | 99 |
| **Stereo DAC Playback to Headphone Output** $f_{MCLK}$ = 13MHz, $f_S$ = 16kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω, low power mode | 0.91 | 0.50 | 0.94 | 0.02 | 0.00 | 3.68 | 97 |
| **DIGITAL AUDIO INPUT TO PLAYBACK PATH TO SPEAKER OUTPUT** | | | | | | | |
| **Stereo DAC Playback to Speaker Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, $R_{LOAD}$ = 8Ω, $L_{LOAD}$ = 68µH | 1.10 | 0.00 | 1.04 | 0.02 | 2.18 | 11.47 | 91 |
| **Stereo DAC Playback to Speaker Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, $R_{LOAD}$ = 8Ω, $L_{LOAD}$ = 68µH, low power mode | 0.91 | 0.00 | 1.03 | 0.02 | 2.18 | 10.93 | 91 |
| **Mono DAC Playback to Speaker Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, $R_{LOAD}$ = 8Ω, $L_{LOAD}$ = 68µH | 0.65 | 0.00 | 0.90 | 0.02 | 1.11 | 6.36 | 91 |
| **Mono DAC Playback to Speaker Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, $R_{LOAD}$ = 8Ω, $L_{LOAD}$ = 68µH, low power mode | 0.51 | 0.00 | 0.90 | 0.02 | 1.11 | 6.09 | 91 |
| **Stereo DAC Playback to Speaker Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 96kHz, 20-bit, music filters, $R_{LOAD}$ = 8Ω, $L_{LOAD}$ = 68µH | 1.21 | 0.00 | 1.17 | 0.02 | 2.18 | 11.61 | 91 |
| **Stereo DAC Playback to Speaker Output** $f_{MCLK}$ = 13MHz, $f_S$ = 44.1kHz, 20-bit, music filters, $R_{LOAD}$ = 8Ω, $L_{LOAD}$ = 68µH | 1.21 | 0.00 | 1.06 | 0.02 | 2.18 | 11.50 | 91 |

## 静态功耗(续)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V, slave mode operation.)

| DEVICE MODE AND CONFIGURATION | $I_{AVDD}$ (mA) | $I_{HPVDD}$ (mA) | $I_{DVDD}$ (mA) | $I_{DVDDIO}$ (mA) | $I_{SPK\_VDD}$ (mA) | POWER (mW) | DYNAMIC RANGE (dB) |
|---|---|---|---|---|---|---|---|
| **ANALOG AUDIO LINE INPUT TO DIGITAL RECORD PATH OUTPUT** | | | | | | | |
| **Stereo Differential Line Input to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters | 3.09 | 0.00 | 1.38 | 0.02 | 0.00 | 7.19 | 98 |
| **Stereo Differential Line Input to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, low power mode | 1.97 | 0.00 | 1.39 | 0.02 | 0.00 | 5.21 | 98 |
| **Stereo Differential Line Input to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, Digital Biquad Filter Enabled | 3.10 | 0.00 | 1.46 | 0.02 | 0.00 | 7.30 | 98 |
| **Mono Differential Line Input to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters | 1.86 | 0.00 | 1.10 | 0.02 | 0.00 | 4.65 | 98 |
| **Stereo Single-Ended Line Input to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters | 3.19 | 0.00 | 1.35 | 0.02 | 0.00 | 7.33 | 97 |
| **Stereo Single-Ended Line Input to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, low power mode | 2.02 | 0.00 | 1.35 | 0.02 | 0.00 | 5.24 | 97 |
| **Stereo Single-Ended Line Input to Record Path** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters | 2.90 | 0.00 | 0.90 | 0.02 | 0.00 | 6.28 | 98 |
| **Stereo Single-Ended Line Input to Record Path** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters low power mode | 1.73 | 0.00 | 0.90 | 0.02 | 0.00 | 4.20 | 97 |

## 静态功耗(续)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V, slave mode operation.)

| DEVICE MODE AND CONFIGURATION | $I_{AVDD}$ (mA) | $I_{HPVDD}$ (mA) | $I_{DVDD}$ (mA) | $I_{DVDDIO}$ (mA) | $I_{SPK\_VDD}$ (mA) | POWER (mW) | DYNAMIC RANGE (dB) |
|---|---|---|---|---|---|---|---|
| **ANALOG MICROPHONE INPUT TO DIGITAL RECORD PATH OUTPUT (MUSIC FILTERS)** | | | | | | | |
| **Stereo Analog Microphone Input to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters | 3.50 | 0.00 | 1.36 | 0.02 | 0.00 | 7.88 | 97 |
| **Stereo Analog Microphone Input to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, low power mode | 2.22 | 0.00 | 1.38 | 0.02 | 0.00 | 5.65 | 97 |
| **Mono Analog Microphone Input to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters | 2.02 | 0.00 | 1.05 | 0.02 | 0.00 | 4.90 | 97 |
| **Mono Analog Microphone Input to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, low power mode | 1.35 | 0.00 | 1.08 | 0.02 | 0.00 | 3.74 | 97 |
| **ANALOG MICROPHONE INPUT TO DIGITAL RECORD PATH OUTPUT (VOICE FILTERS)** | | | | | | | |
| **Stereo Analog Microphone Input to Record Path** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters | 3.20 | 0.00 | 0.91 | 0.02 | 0.00 | 6.81 | 99 |
| **Stereo Analog Microphone Input to Record Path** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters low power mode | 1.93 | 0.00 | 0.92 | 0.02 | 0.00 | 4.57 | 98 |
| **Mono Analog Microphone Input to Record Path** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters | 1.87 | 0.00 | 0.82 | 0.02 | 0.00 | 4.35 | 99 |
| **Mono Analog Microphone Input to Record Path** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters low power mode | 1.20 | 0.00 | 0.83 | 0.02 | 0.00 | 3.18 | 98 |
| **Stereo Analog Microphone Input to Record Path** $f_{MCLK}$ = 13MHz, $f_S$ = 16kHz, 16-bit, voice filters | 3.26 | 0.00 | 1.11 | 0.02 | 0.00 | 7.16 | 98 |
| **Stereo Analog Microphone Input to Record Path** $f_{MCLK}$ = 13MHz, $f_S$ = 16kHz, 16-bit, voice filters low power mode | 1.98 | 0.00 | 1.12 | 0.02 | 0.00 | 4.91 | 97 |
| **Mono Analog Microphone Input to Record Path** $f_{MCLK}$ = 13MHz, $f_S$ = 16kHz, 16-bit, voice filters | 1.90 | 0.00 | 0.94 | 0.02 | 0.00 | 4.54 | 98 |
| **Mono Analog Microphone Input to Record Path** $f_{MCLK}$ = 13MHz, $f_S$ = 16kHz, 16-bit, voice filters low power mode | 1.23 | 0.00 | 0.94 | 0.02 | 0.00 | 3.35 | 97 |

## 静态功耗(续)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V, slave mode operation.)

| DEVICE MODE AND CONFIGURATION | $I_{AVDD}$ (mA) | $I_{HPVDD}$ (mA) | $I_{DVDD}$ (mA) | $I_{DVDDIO}$ (mA) | $I_{SPK\_VDD}$ (mA) | POWER (mW) | DYNAMIC RANGE (dB) |
|---|---|---|---|---|---|---|---|
| **ANALOG AUDIO INPUT DIRECT TO DIGITAL RECORD PATH OUTPUT** | | | | | | | |
| **Stereo Differential Input Direct to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters | 2.85 | 0.00 | 1.39 | 0.02 | 0.00 | 6.76 | 99 |
| **Stereo Differential Input Direct to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, low power mode | 1.84 | 0.00 | 1.39 | 0.02 | 0.00 | 4.98 | 98 |
| **Mono Differential Input Direct to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters | 1.61 | 0.00 | 1.08 | 0.02 | 0.00 | 4.20 | 99 |
| **Mono Differential Input Direct to Record Path** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, low power mode | 1.09 | 0.00 | 1.09 | 0.02 | 0.00 | 3.29 | 98 |
| **ANALOG AUDIO INPUT TO ANALOG AUDIO OUTPUT** | | | | | | | |
| **Stereo Single-Ended Line Input to Headphones** ($R_{LOAD}$ = 32Ω) | 1.12 | 2.42 | 0.00 | 0.00 | 0.00 | 6.34 | 99 |
| **Mono Single-Ended Line Input to Headphones** ($R_{LOAD}$ = 32Ω) | 0.72 | 1.57 | 0.00 | 0.00 | 0.00 | 3.41 | 99 |
| **Stereo Differential Line Input to Headphones** ($R_{LOAD}$ = 32Ω) | 1.07 | 1.26 | 0.00 | 0.00 | 0.00 | 4.19 | 100 |
| **Stereo Differential Line Input to Speaker Output** ($R_{LOAD}$ = 8Ω, $L_{LOAD}$ = 68µH) | 0.36 | 0.00 | 0.00 | 0.00 | 2.08 | 8.34 | 91 |
| **Mono Differential Line Input to Speaker Output** ($R_{LOAD}$ = 8Ω, $L_{LOAD}$ = 68µH) | 0.31 | 0.00 | 0.00 | 0.00 | 1.04 | 4.42 | 91 |
| **Stereo Single-Ended Line Input to Line Output** ($R_{LOAD}$ = 10kΩ) | 0.76 | 0.00 | 0.00 | 0.00 | 0.74 | 4.12 | 99 |

## 静态功耗(续)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V, slave mode operation.)

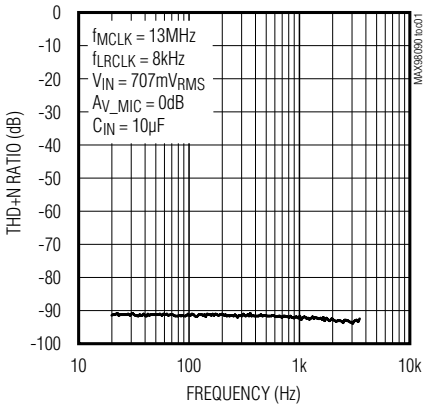
| DEVICE MODE AND CONFIGURATION | $I_{AVDD}$ (mA) | $I_{HPVDD}$ (mA) | $I_{DVDD}$ (mA) | $I_{DVDDIO}$ (mA) | $I_{SPK\_VDD}$ (mA) | POWER (mW) | DYNAMIC RANGE (dB) |
|---|---|---|---|---|---|---|---|
| **FULL-DUPLEX AUDIO OPERATION** | | | | | | | |
| **Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Receiver Output** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω | 2.67 | 0.00 | 0.95 | 0.02 | 0.73 | 8.61 | REC: 99 PB: 100 |
| **Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Receiver Output** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω, low power mode | 1.94 | 0.00 | 0.95 | 0.02 | 0.73 | 7.31 | REC: 99 PB: 98 |
| **Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphone Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, $R_{LOAD}$ = 32Ω | 2.69 | 0.69 | 1.22 | 0.02 | 0.00 | 7.51 | REC: 97 PB: 102 |
| **Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphone Output** $f_{MCLK}$ = 12.288MHz, $f_S$ = 48kHz, 20-bit, music filters, $R_{LOAD}$ = 32Ω, low power mode | 1.80 | 0.30 | 1.24 | 0.02 | 0.00 | 5.26 | REC: 97 PB: 99 |
| **Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphone Output** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω | 2.54 | 0.69 | 0.95 | 0.02 | 0.00 | 6.93 | REC: 99 PB: 102 |
| **Mono Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphone Output** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω, low power mode | 1.66 | 0.30 | 0.96 | 0.02 | 0.00 | 4.67 | REC: 99 PB: 99 |
| **Stereo Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphones** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω | 4.44 | 1.28 | 1.14 | 0.02 | 0.00 | 11.54 | REC: 99 PB: 102 |
| **Stereo Full Duplex: Analog Microphone Input to Record Path and DAC Playback to Headphones** $f_{MCLK}$ = 13MHz, $f_S$ = 8kHz, 16-bit, voice filters, $R_{LOAD}$ = 32Ω, low power mode | 2.73 | 0.51 | 1.15 | 0.02 | 0.00 | 7.18 | REC: 99 PB: 99 |

## 典型工作特性

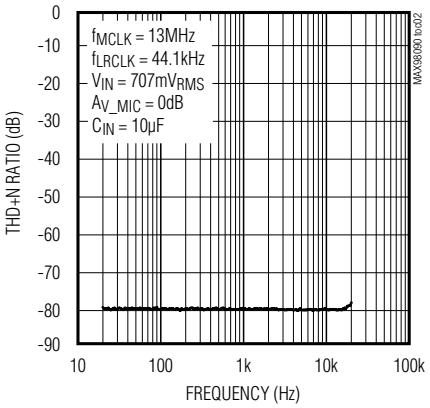
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### ANALOG MICROPHONE INPUT TO ADC RECORD PATH OUTPUT

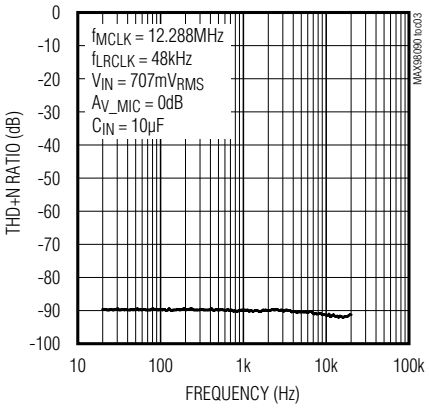
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)**



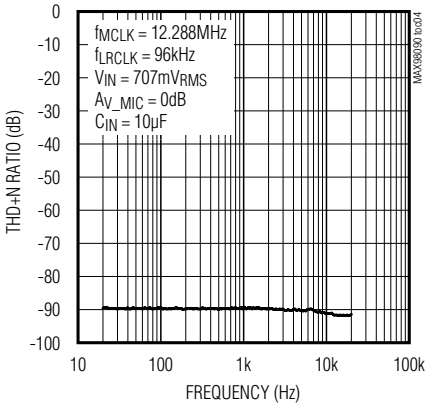

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)**



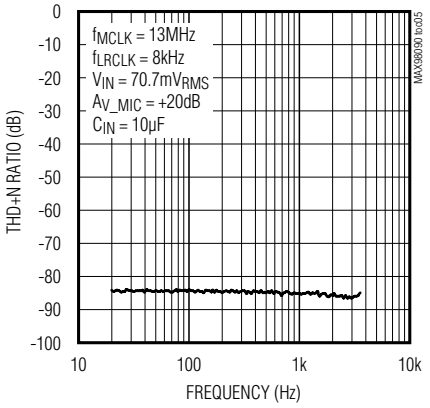

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)**



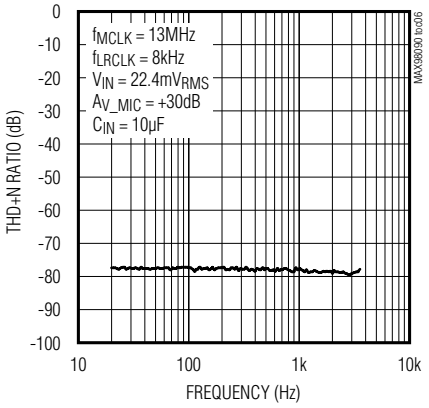

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (MIC TO ADC)**

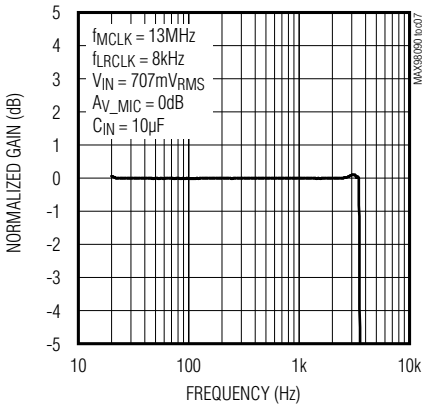


## 典型工作特性(续)

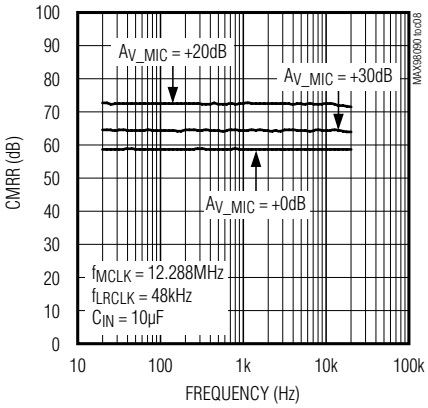
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### ANALOG MICROPHONE INPUT TO ADC RECORD PATH OUTPUT (CONTINUED)

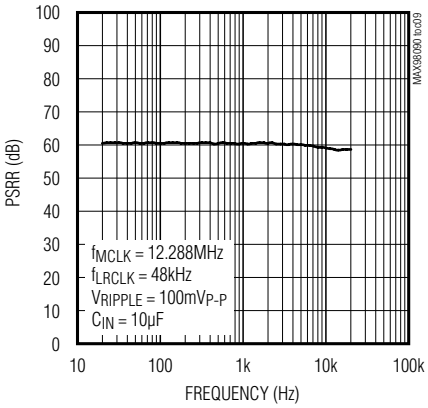
**GAIN vs. FREQUENCY (MIC TO ADC)**



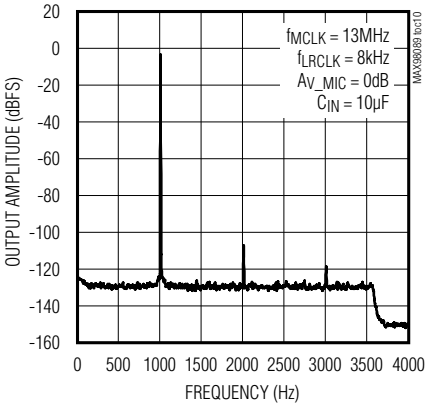

**COMMON-MODE REJECTION RATIO vs. FREQUENCY (MIC TO ADC)**



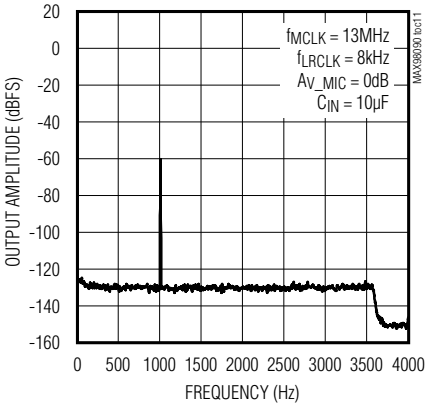

**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MIC TO ADC)**



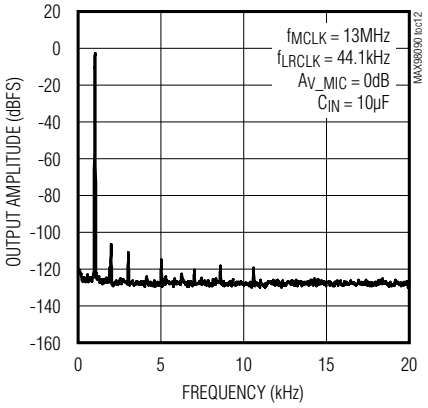

**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (MIC TO ADC)**




**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (MIC TO ADC)**




**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (MIC TO ADC)**

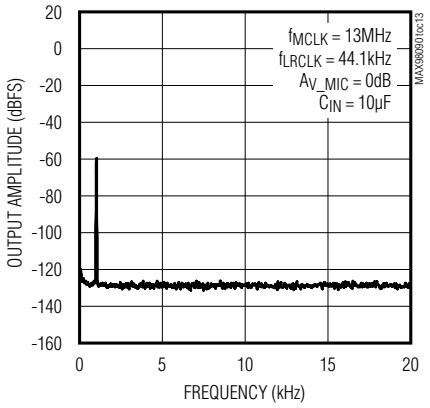


## 典型工作特性(续)

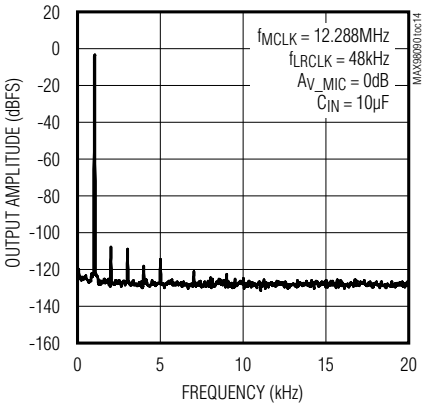
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### ANALOG MICROPHONE INPUT TO ADC RECORD PATH OUTPUT (CONTINUED)

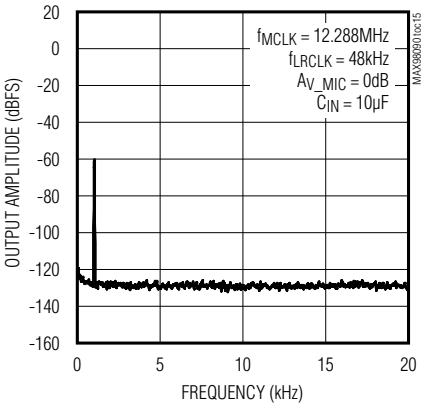
**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (MIC TO ADC)**



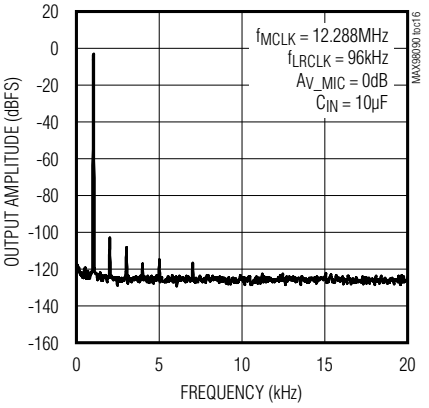

**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (MIC TO ADC)**



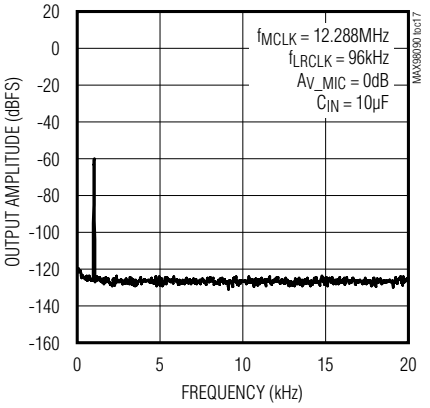

**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (MIC TO ADC)**




**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (MIC TO ADC)**




**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (MIC TO ADC)**

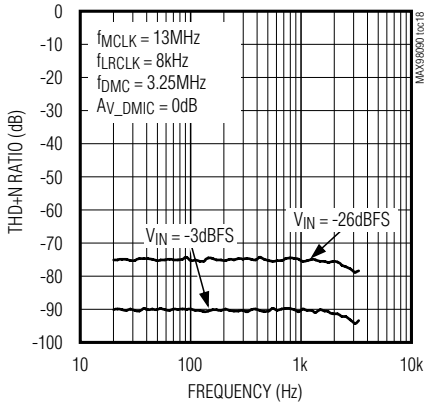


## 典型工作特性(续)

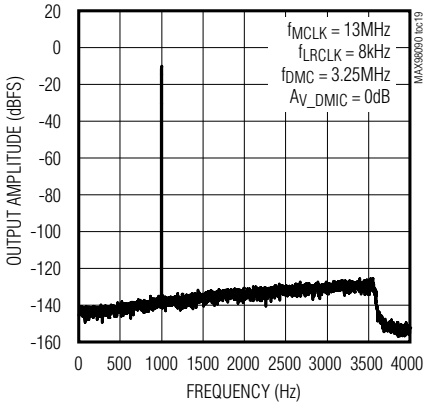
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DIGITAL MICROPHONE INPUT TO RECORD PATH OUTPUT

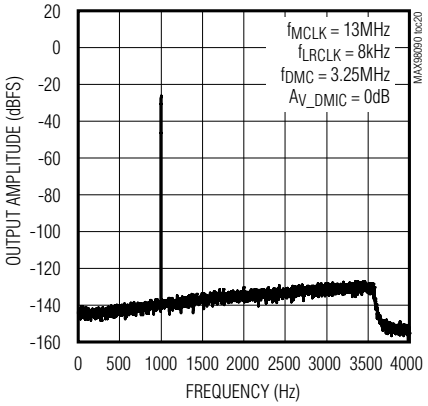
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DIGITAL MIC TO RECORD PATH)**



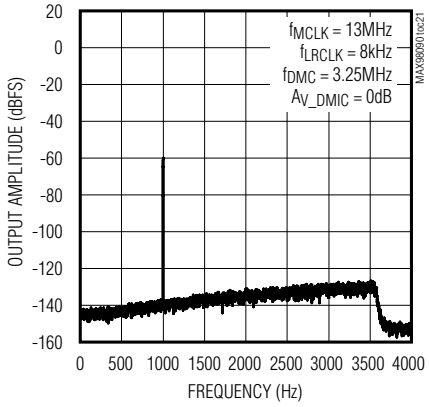

**INBAND OUTPUT SPECTRUM, -10dBFS INPUT (DIGITAL MIC TO RECORD PATH)**



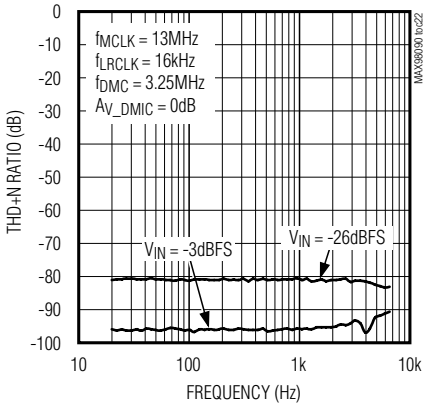

**INBAND OUTPUT SPECTRUM, -26dBFS INPUT (DIGITAL MIC TO RECORD PATH)**



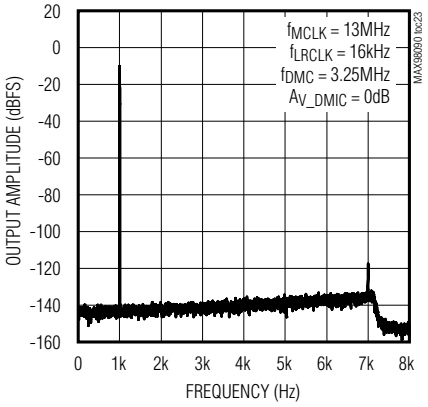

**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DIGITAL MIC TO RECORD PATH)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DIGITAL MIC TO RECORD PATH)**




**INBAND OUTPUT SPECTRUM, -10dBFS INPUT (DIGITAL MIC TO RECORD PATH)**

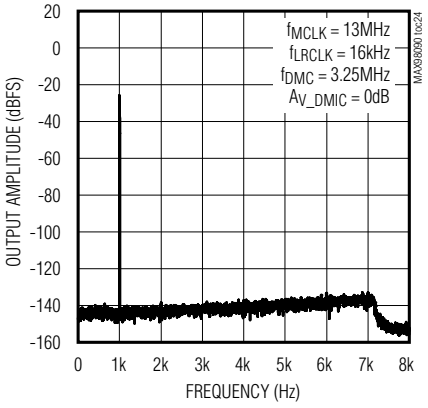


## 典型工作特性(续)

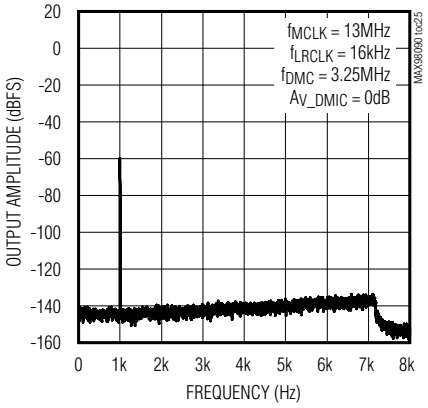
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DIGITAL MICROPHONE INPUT TO RECORD PATH OUTPUT (CONTINUED)

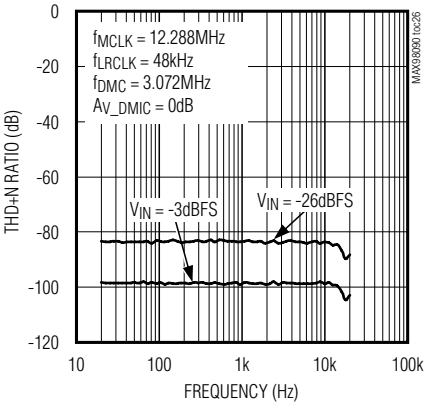
**INBAND OUTPUT SPECTRUM, -26dBFS INPUT (DIGITAL MIC TO RECORD PATH)**



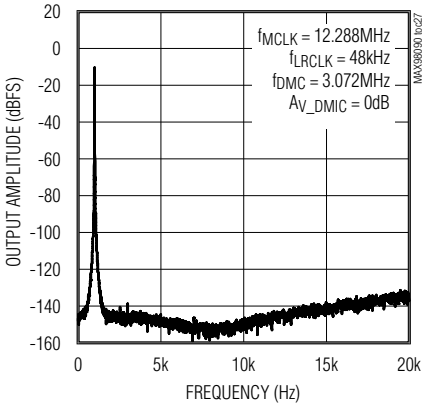

**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DIGITAL MIC TO RECORD PATH)**



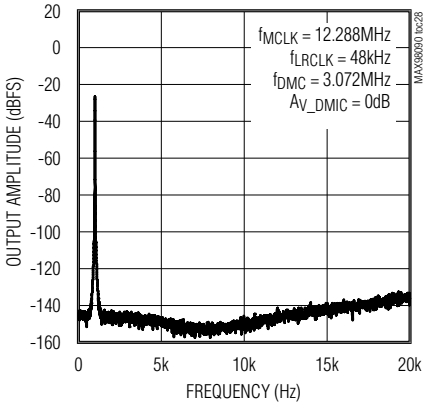

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DIGITAL MIC TO RECORD PATH)**



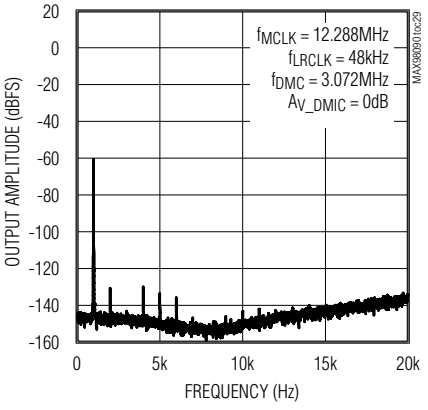

**INBAND OUTPUT SPECTRUM, -10dBFS INPUT (DIGITAL MIC TO RECORD PATH)**




**INBAND OUTPUT SPECTRUM, -26dBFS INPUT (DIGITAL MIC TO RECORD PATH)**




**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DIGITAL MIC TO RECORD PATH)**

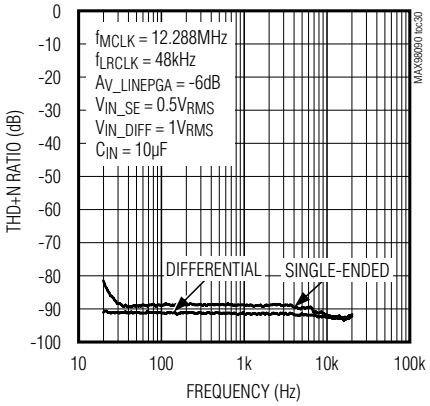


## 典型工作特性(续)

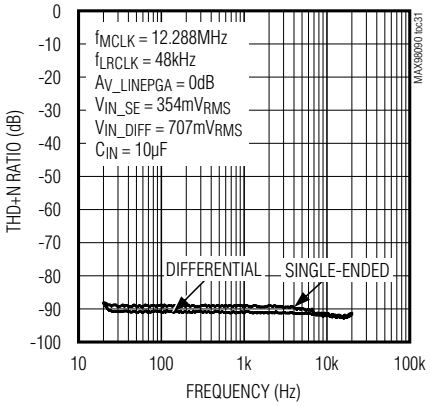
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### LINE INPUT TO ADC RECORD PATH OUTPUT

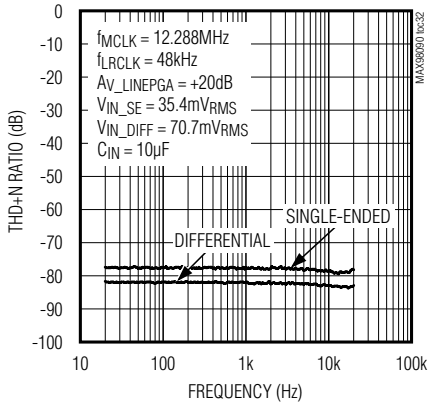
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)**



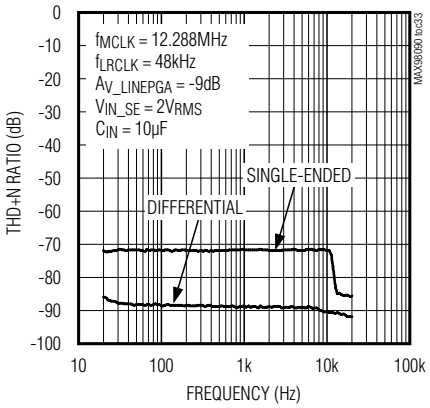

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)**



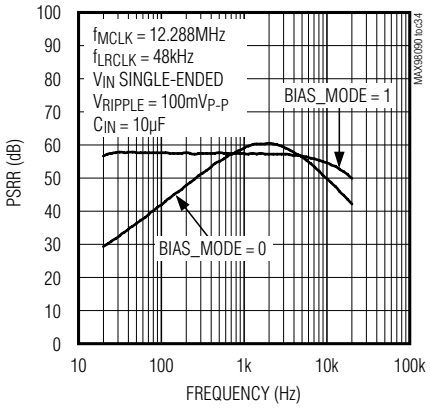

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)**



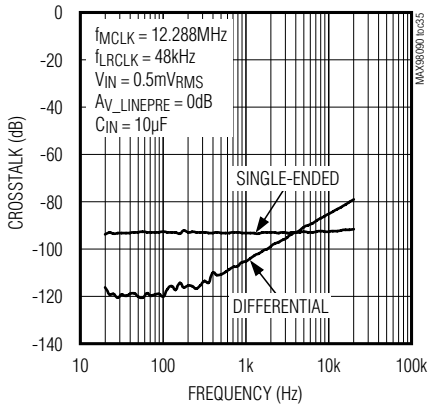

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC)**




**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO ADC)**




**CROSSTALK vs. FREQUENCY (LINE TO ADC)**

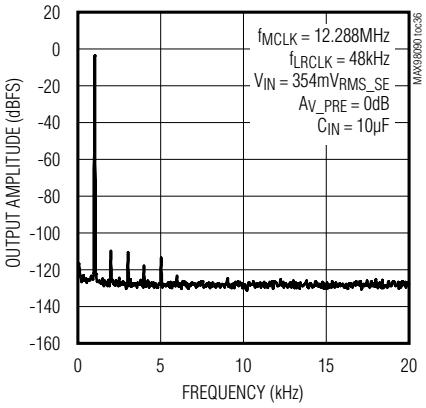


## 典型工作特性(续)

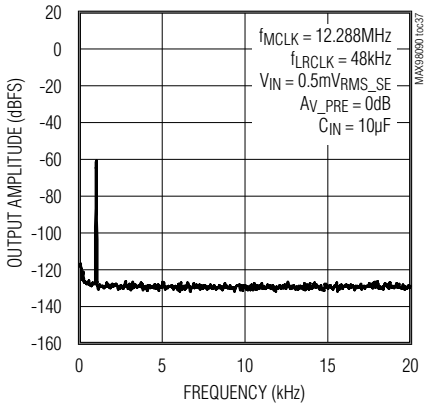
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### LINE INPUT TO ADC RECORD PATH OUTPUT (CONTINUED)

**INBAND OUTPUT SPECTRUM vs. FREQUENCY,-3dBFS INPUT (LINE TO ADC)**

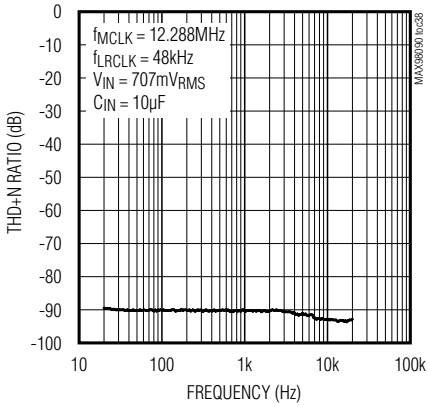



**INBAND OUTPUT SPECTRUM vs. FREQUENCY, -60dBFS INPUT (LINE TO ADC)**

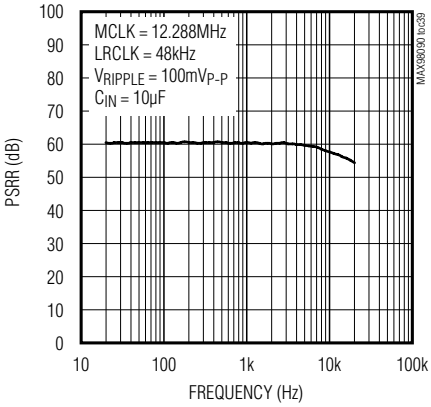



### DIRECT ANALOG INPUT TO ADC RECORD PATH OUTPUT

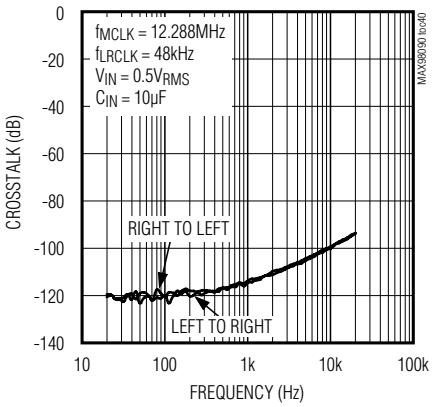
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (INPUT DIRECT TO ADC MIXER)**




**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (INPUT DIRECT TO ADC MIXER)**




**CROSSTALK vs. FREQUENCY (INPUT DIRECT TO ADC MIXER)**

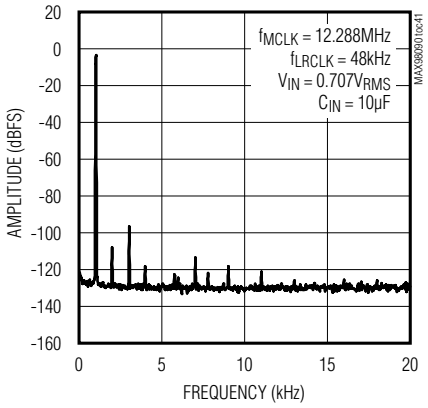


## 典型工作特性(续)

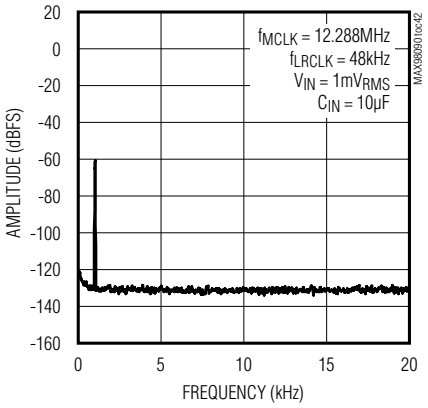
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DIRECT ANALOG INPUT TO ADC RECORD PATH OUTPUT (CONTINUED)

**INBAND OUTPUT SPECTRUM, -3dBFS (INPUT DIRECT TO ADC MIXER)**

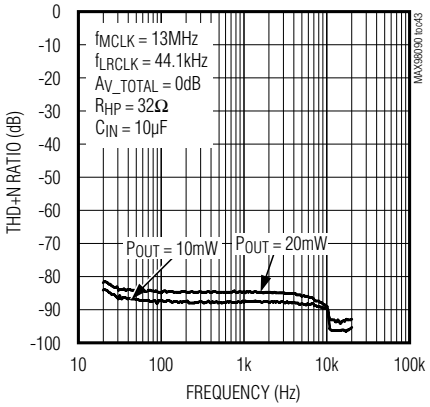



**INBAND OUTPUT SPECTRUM, -60dBFS (INPUT DIRECT TO ADC MIXER)**

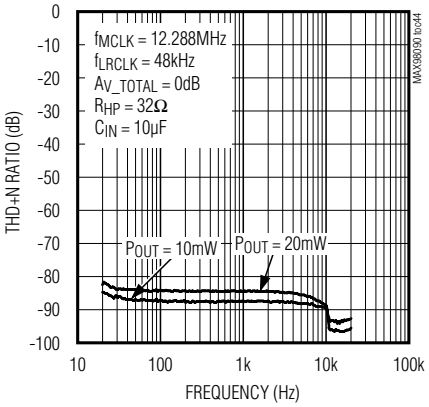



### ADC RECORD PATH TO DAC PLAYBACK INTERNAL LOOP THROUGH

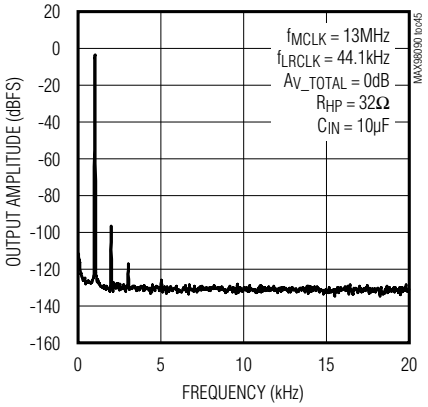
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)**




**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (LINE TO ADC TO DAC TO HEADPHONE)**

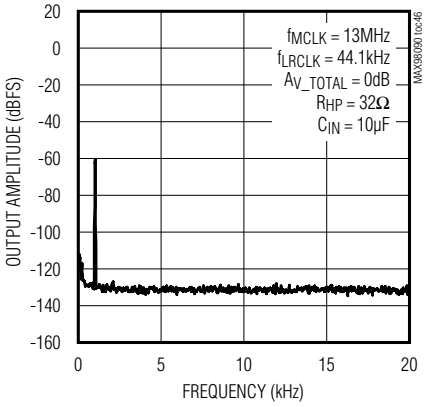


## 典型工作特性(续)

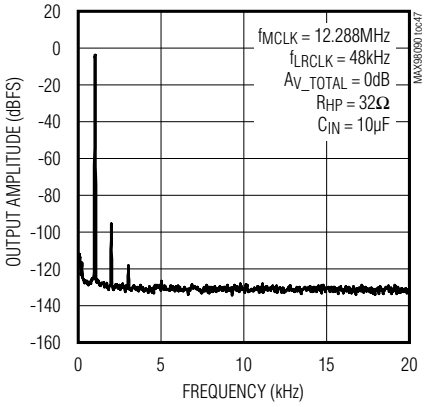
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### ADC RECORD PATH TO DAC PLAYBACK INTERNAL LOOP THROUGH (CONTINUED)

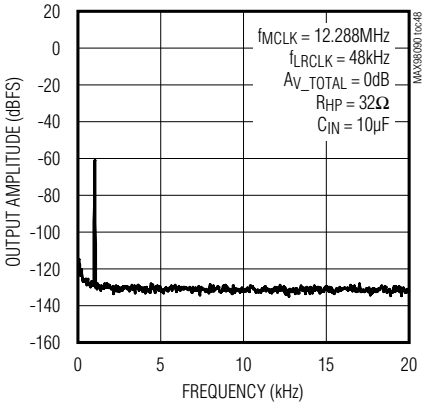
**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (LINE TO ADC TO DAC TO HEADPHONE)**




**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (LINE TO ADC TO DAC TO HEADPHONE)**

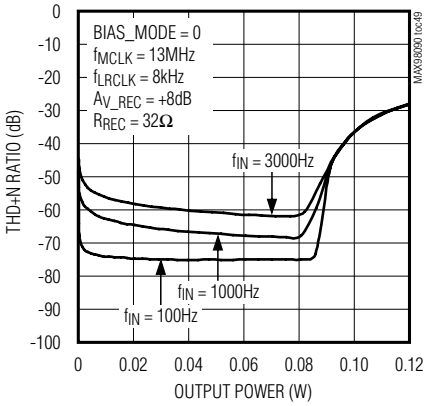



**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (LINE TO ADC TO DAC TO HEADPHONE)**

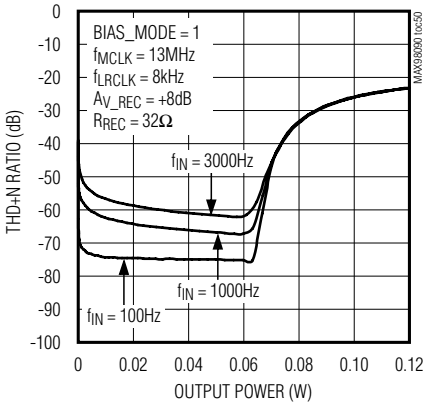



### DAC PLAYBACK PATH INPUT TO RECEIVER OUTPUT

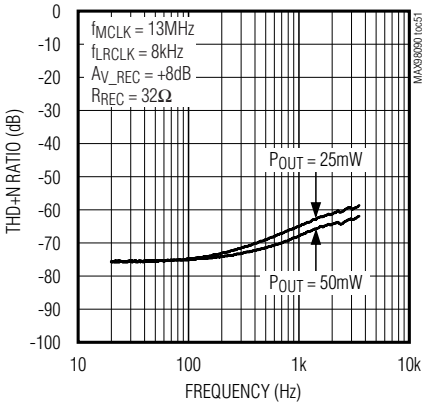
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO RECEIVER)**




**TOTAL HARMONIC DISTORTION vs. OUTPUT POWER (DAC TO RECEIVER)**




**TOTAL HARMONIC DISTORTION vs. FREQUENCY (DAC TO RECEIVER)**

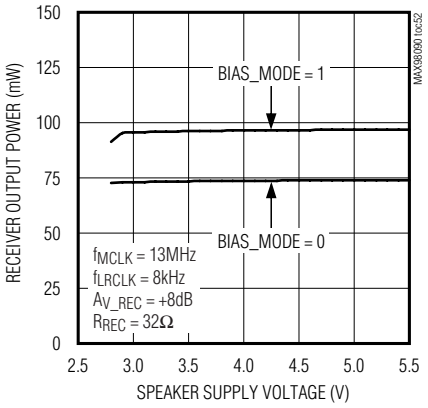


## 典型工作特性(续)

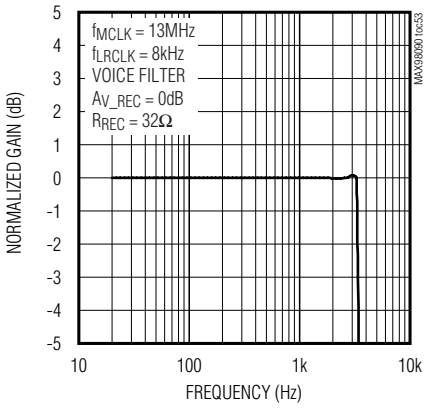
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO RECEIVER OUTPUT (CONTINUED)

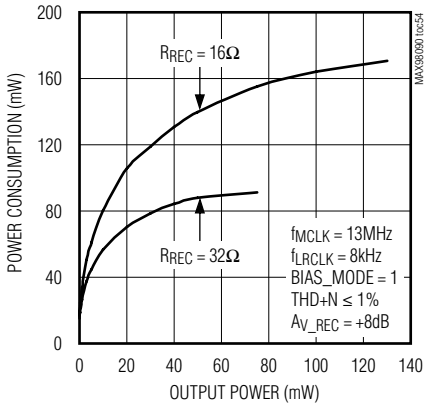
**OUTPUT POWER vs. SPEAKER SUPPLY VOLTAGE (DAC TO RECEIVER)**



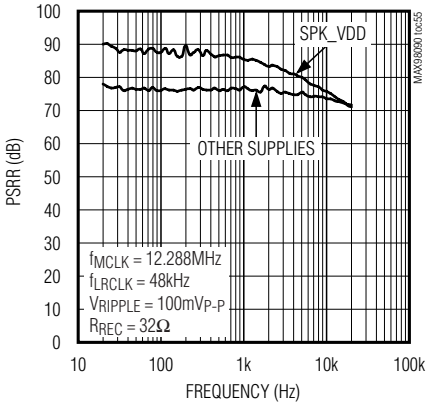

**GAIN vs. FREQUENCY (DAC TO RECEIVER)**



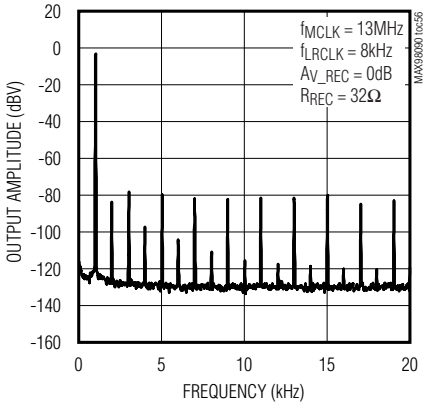

**POWER CONSUMPTION vs. OUTPUT POWER (DAC TO RECEIVER)**



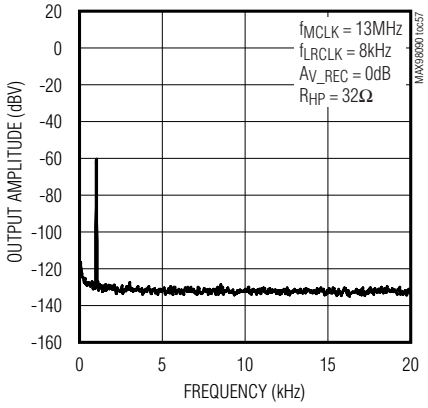

**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO RECEIVER)**




**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO RECEIVER)**




**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO RECEIVER)**

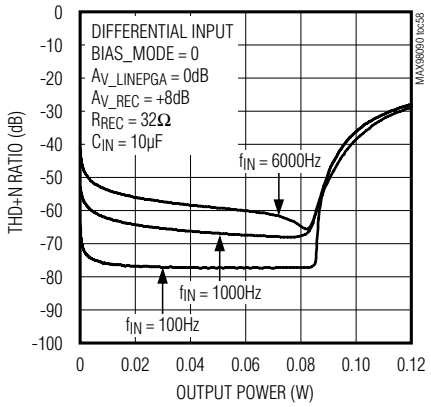


## 典型工作特性(续)

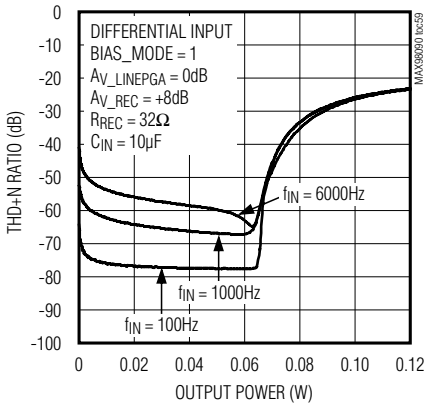
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### LINE INPUT TO RECEIVER OUTPUT

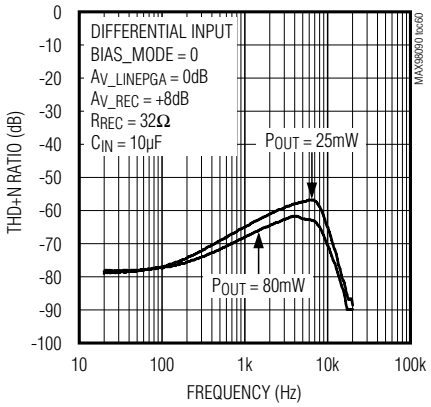
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO RECEIVER)**



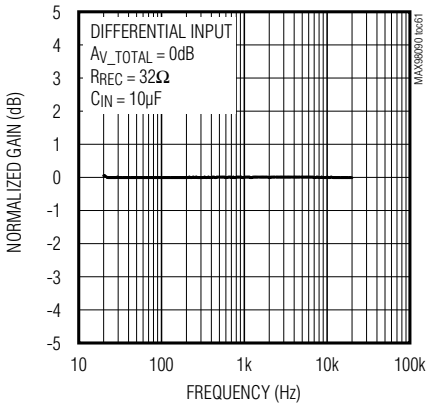

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO RECEIVER)**



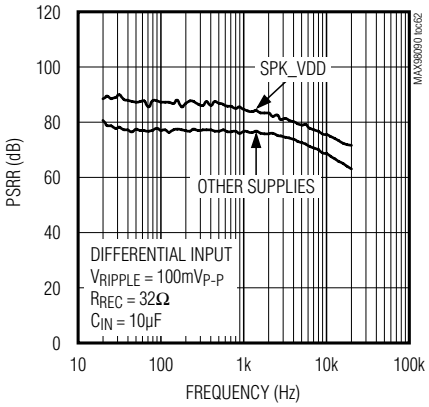

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO RECEIVER)**




**GAIN vs. FREQUENCY (LINE TO RECEIVER)**




**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO RECEIVER)**

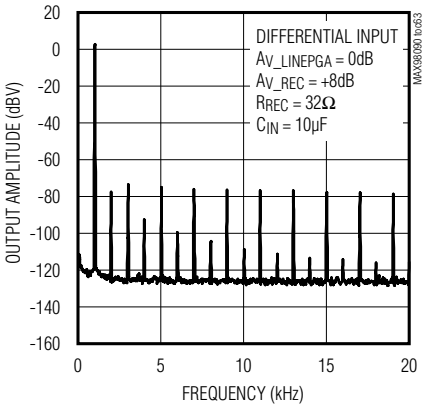


## 典型工作特性(续)

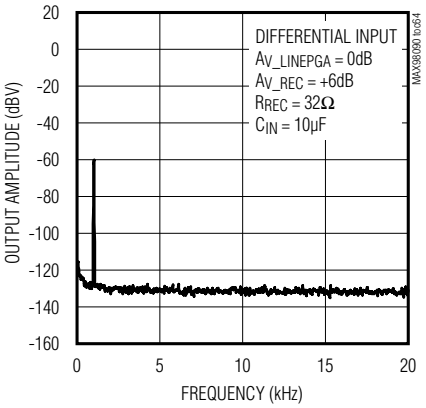
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### LINE INPUT TO RECEIVER OUTPUT (CONTINUED)

**INBAND OUTPUT SPECTRUM, -3dBV INPUT (LINE TO RECEIVER)**

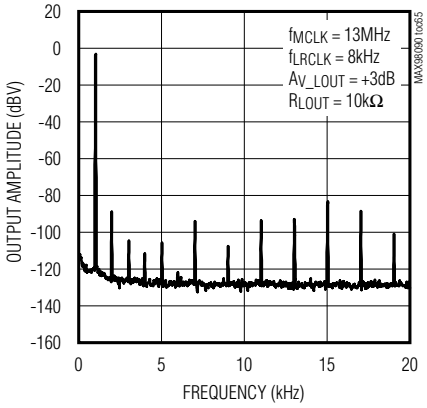



**INBAND OUTPUT SPECTRUM, -60dBV INPUT (LINE TO RECEIVER)**

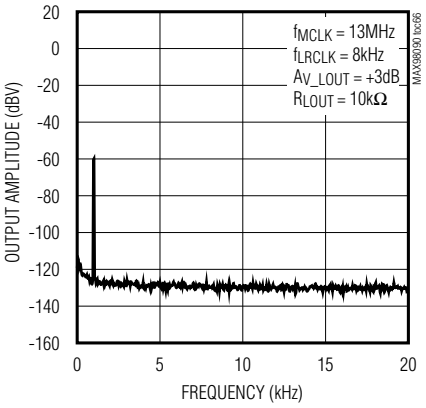



### DAC PLAYBACK PATH INPUT TO LINE OUTPUT

**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO LINE OUT)**




**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO LINE OUT)**

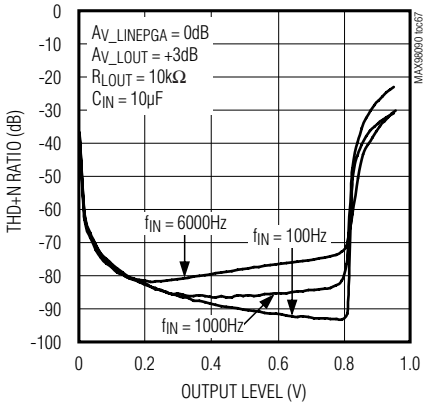


## 典型工作特性(续)

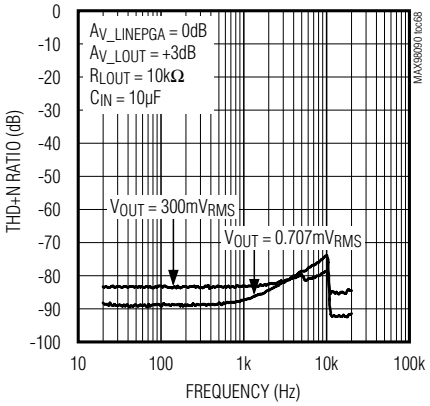
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### LINE INPUT TO LINE OUTPUT

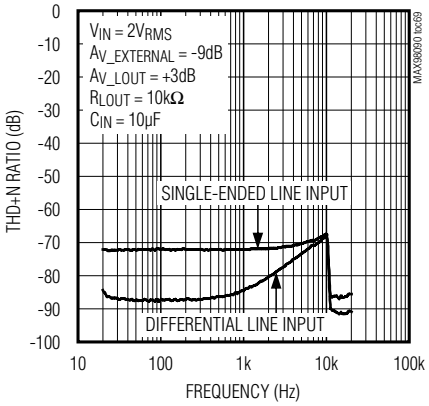
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT LEVEL (LINE IN TO LINE OUT)**



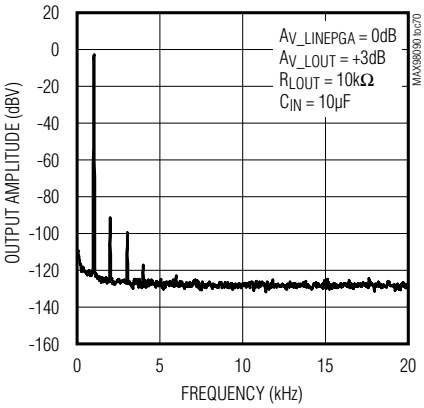

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE IN TO LINE OUT)**



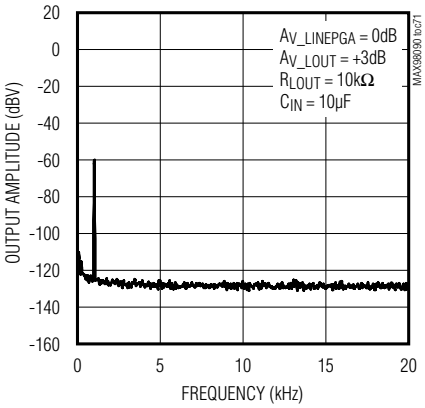

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE IN TO LINE OUT)**




**INBAND OUTPUT SPECTRUM, -3dBV INPUT (LINE IN TO LINE OUT)**




**INBAND OUTPUT SPECTRUM, -60dBV INPUT (LINE IN TO LINE OUT)**

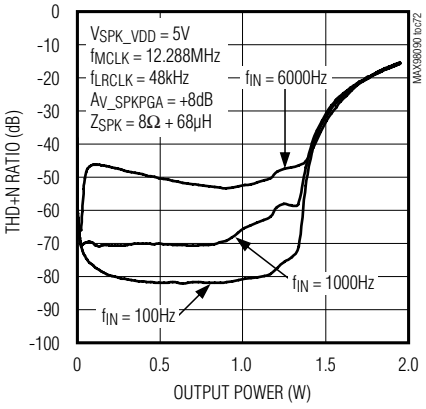


## 典型工作特性(续)

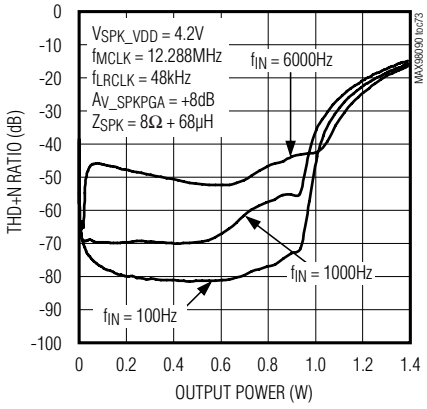
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT

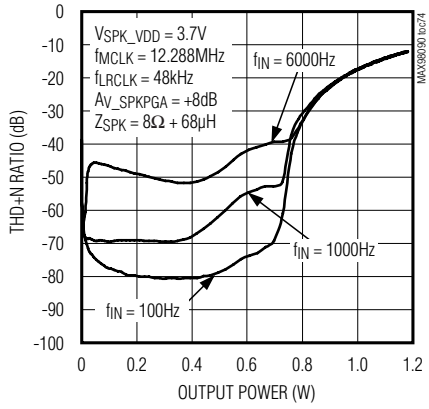
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)**



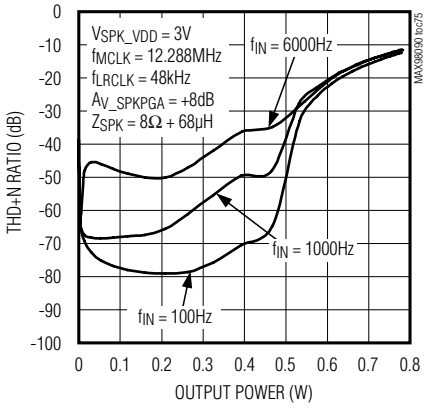

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)**



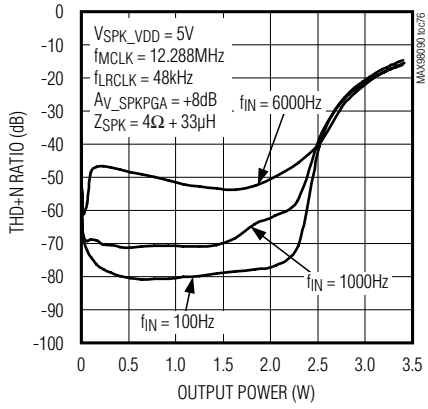

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)**



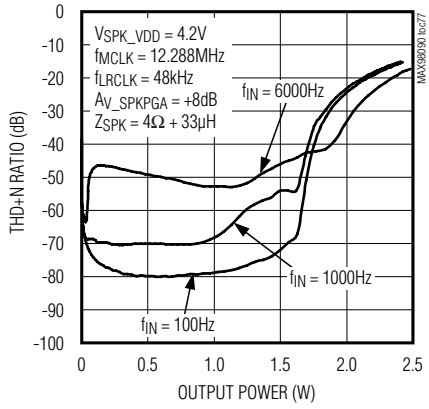

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)**

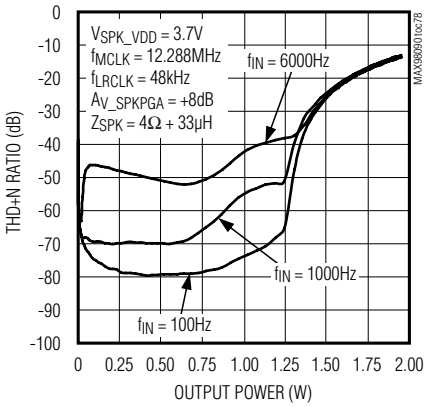


## 典型工作特性(续)

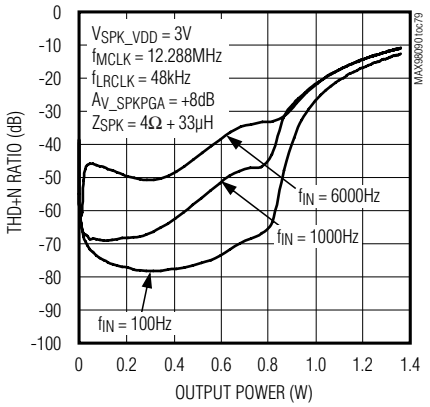
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

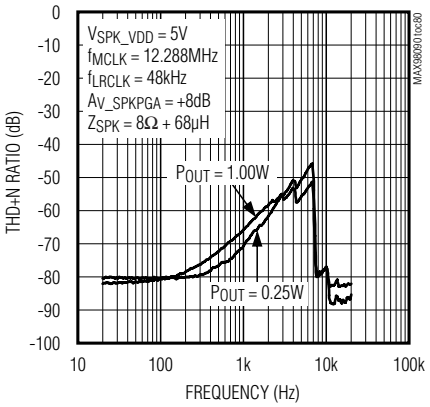
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)**



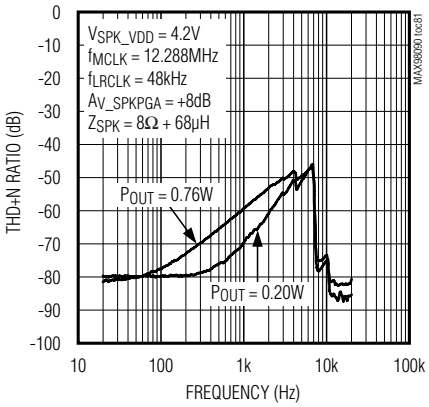

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO SPEAKER)**



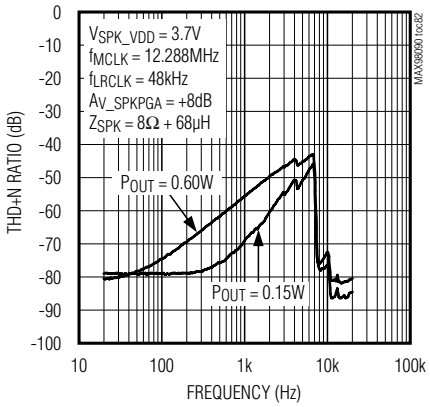

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)**



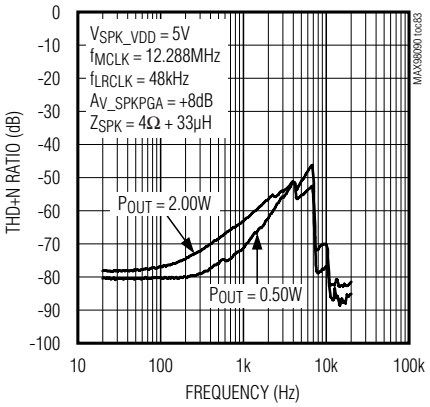

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)**

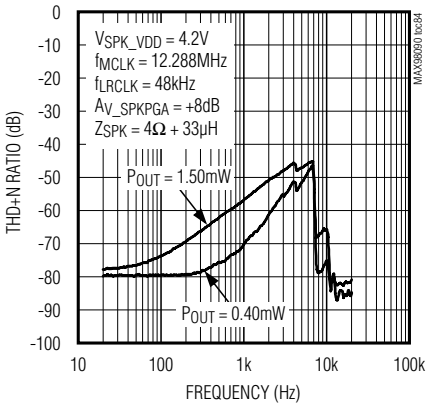


## 典型工作特性(续)

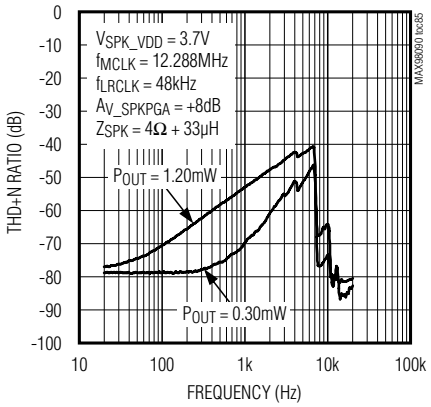
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

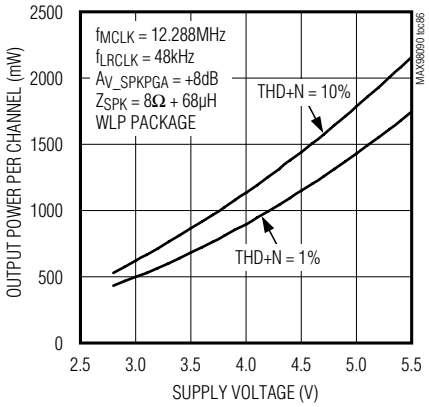
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)**



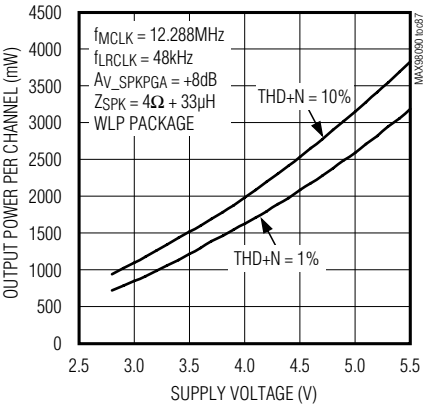

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO SPEAKER)**



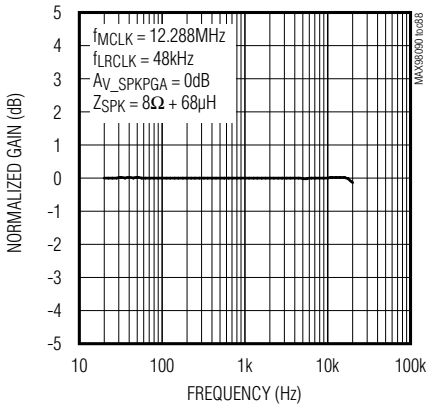

**OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)**



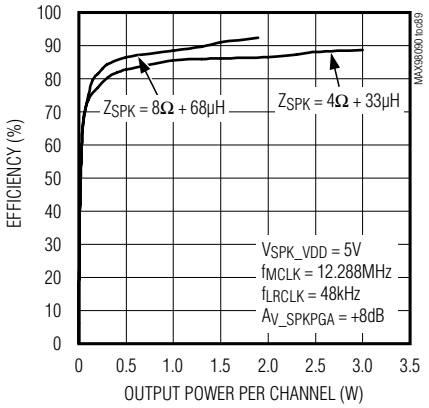

**OUTPUT POWER vs. SUPPLY VOLTAGE (DAC TO SPEAKER)**




**GAIN vs. FREQUENCY (DAC TO SPEAKER)**




**EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)**

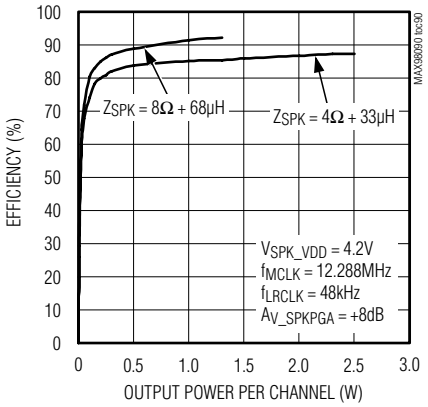


## 典型工作特性(续)

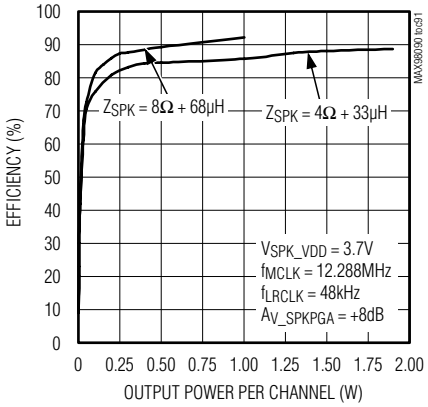
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

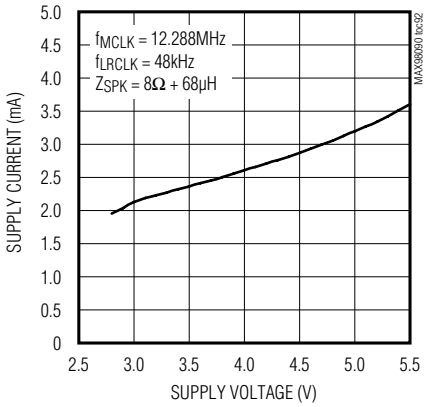
**EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)**



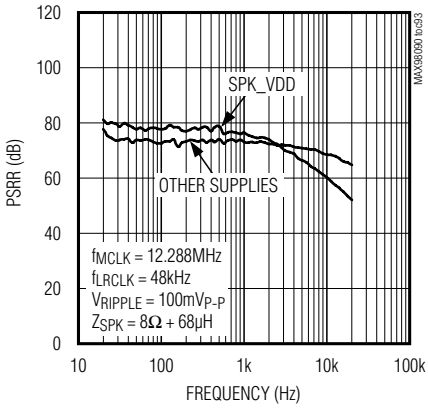

**EFFICIENCY vs. OUTPUT POWER (DAC TO SPEAKER)**



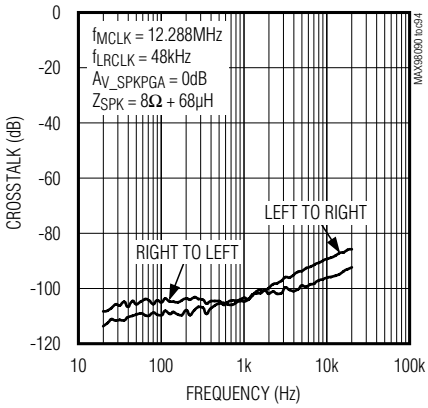

**SUPPLY CURRENT vs. SUPPLY VOLTAGE (DAC TO SPEAKER)**



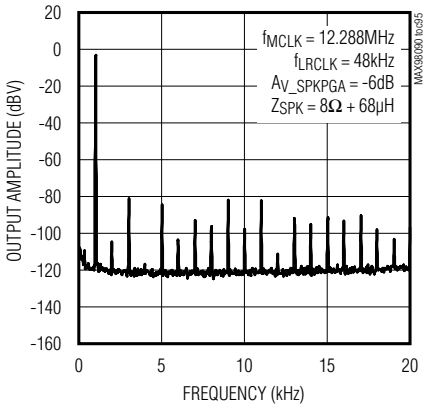

**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO SPEAKER)**




**CROSSTALK vs. FREQUENCY (DAC TO SPEAKER)**




**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO SPEAKER)**

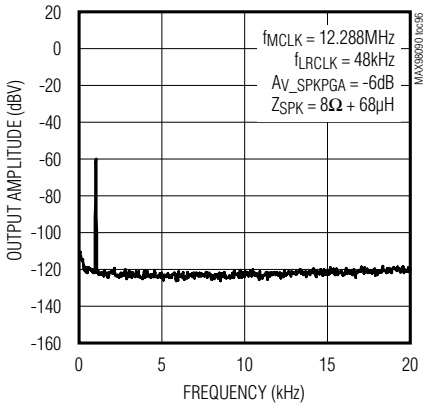


## 典型工作特性(续)

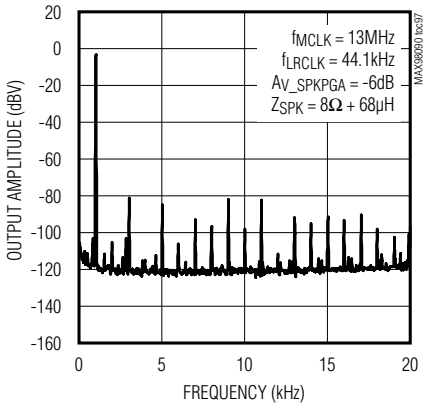
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO SPEAKER OUTPUT (CONTINUED)

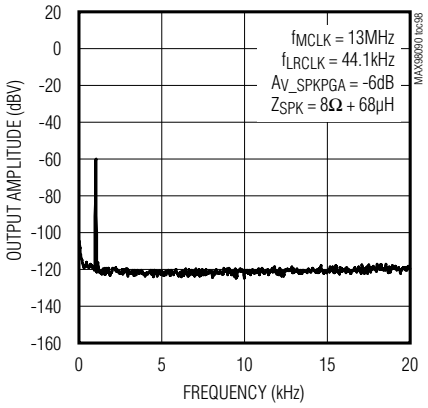
**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO SPEAKER)**



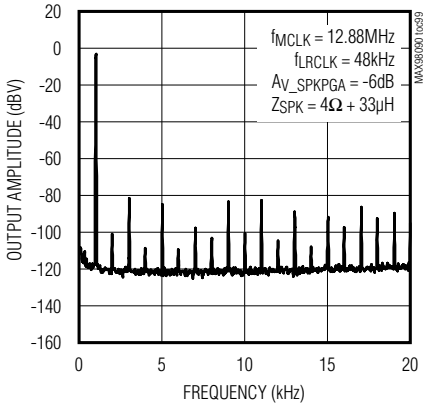

**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO SPEAKER)**



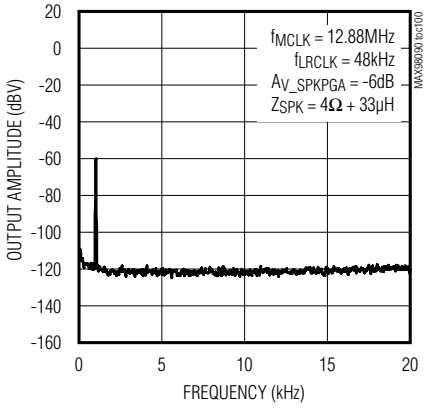

**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO SPEAKER)**



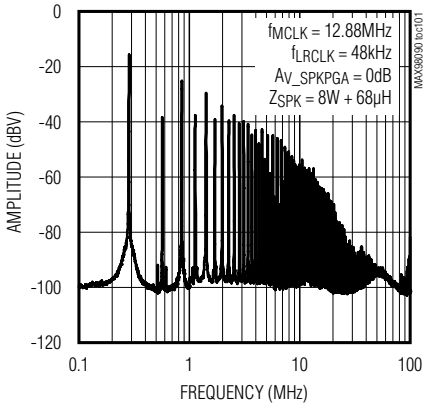

**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO SPEAKER)**




**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO SPEAKER)**




**WIDEBAND FREQUENCY SPECTRUM (DAC TO SPEAKER)**

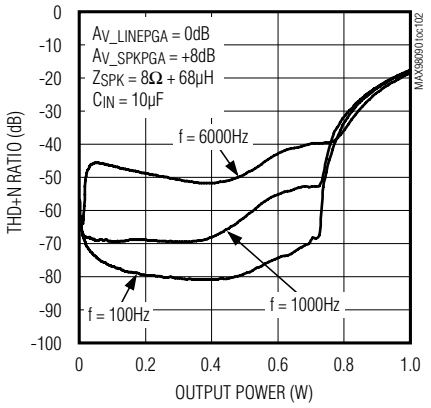


## 典型工作特性(续)

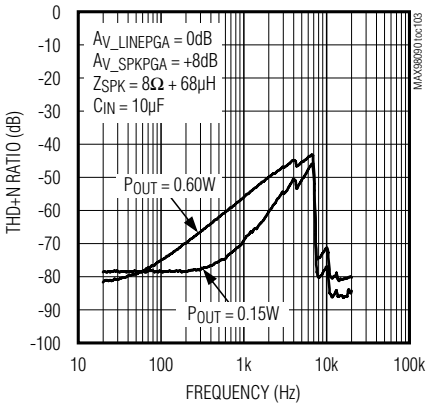
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### LINE INPUT TO SPEAKER OUTPUT

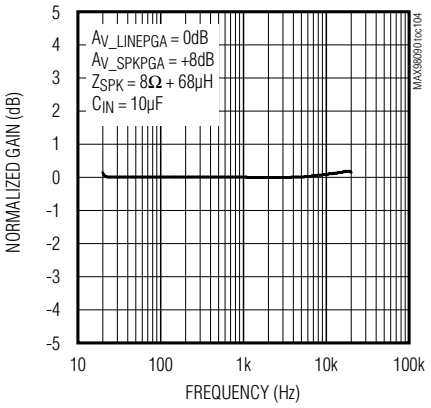
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO SPEAKER)**



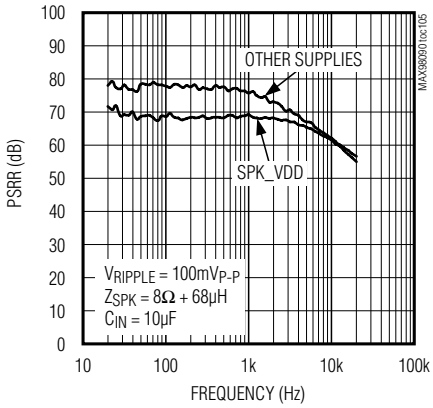

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO SPEAKER)**



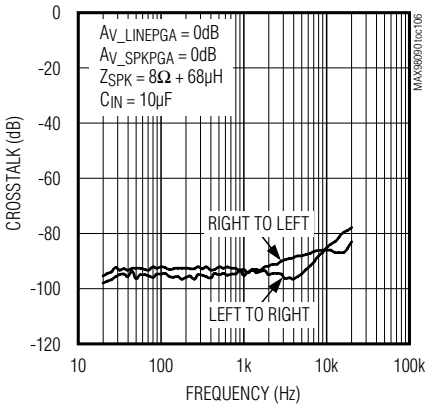

**GAIN vs. FREQUENCY (LINE TO SPEAKER)**



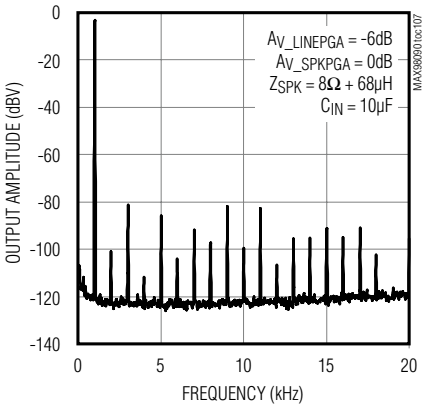

**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO SPEAKER)**




**CROSSTALK vs. FREQUENCY (LINE TO SPEAKER)**




**INBAND OUTPUT SPECTRUM, -3dBV INPUT (LINE TO SPEAKER)**

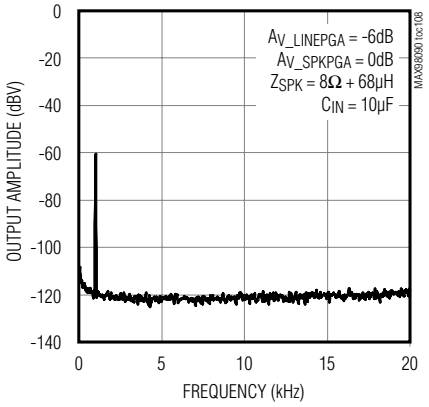


## 典型工作特性(续)

($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

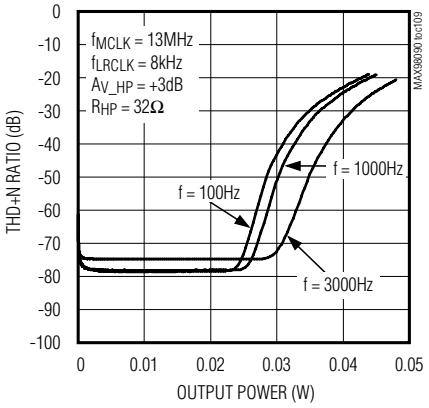
### LINE INPUT TO SPEAKER OUTPUT (CONTINUED)

**INBAND OUTPUT SPECTRUM, -60dBV INPUT (LINE TO SPEAKER)**

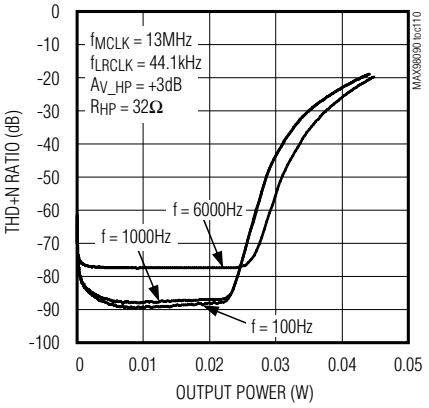



### DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT

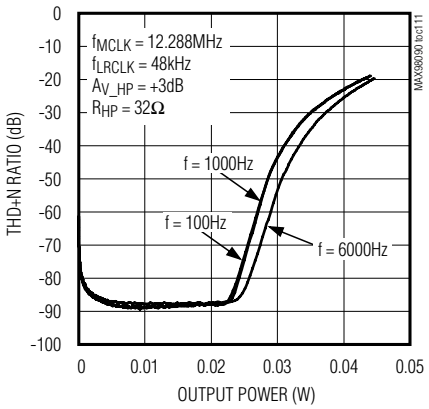
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)**



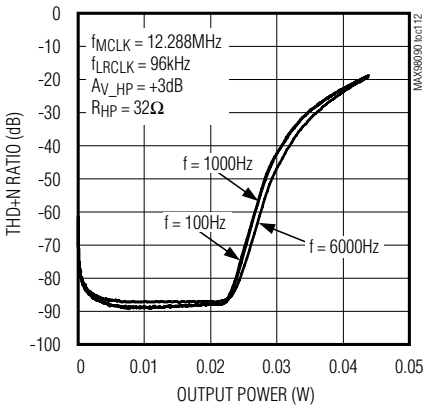

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)**



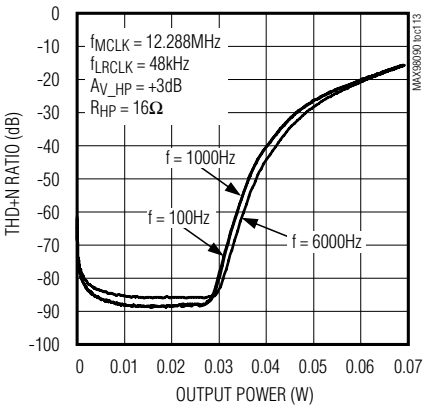

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)**

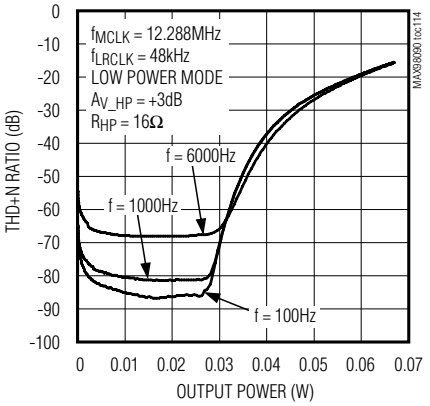


## 典型工作特性(续)

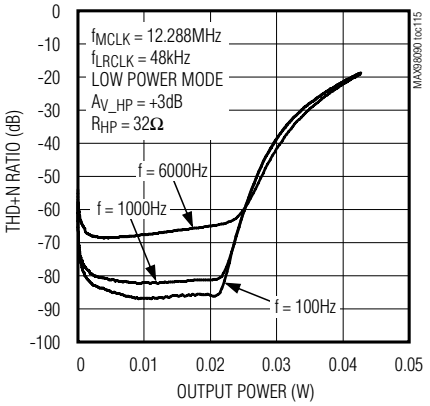
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT (CONTINUED)

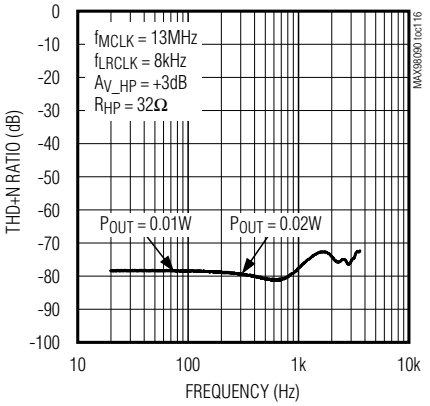
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)**



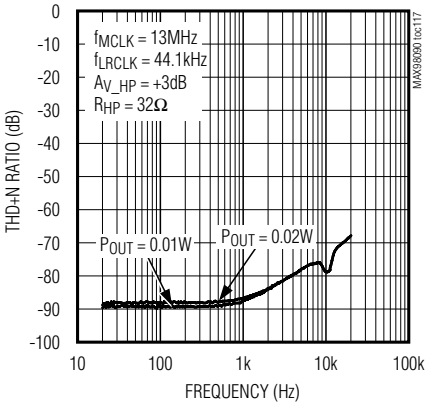

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (DAC TO HEADPHONE)**



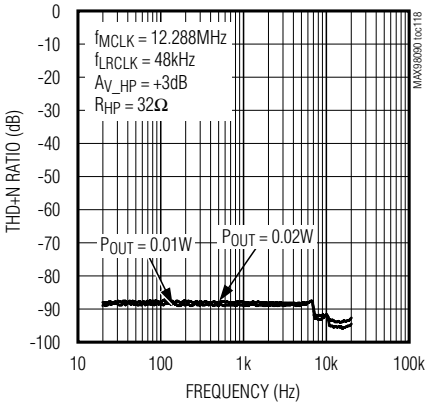

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)**



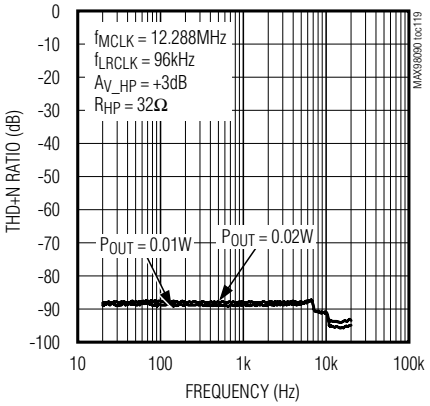

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)**




**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)**

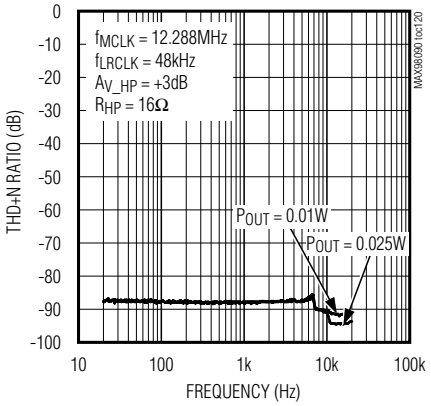


## 典型工作特性(续)

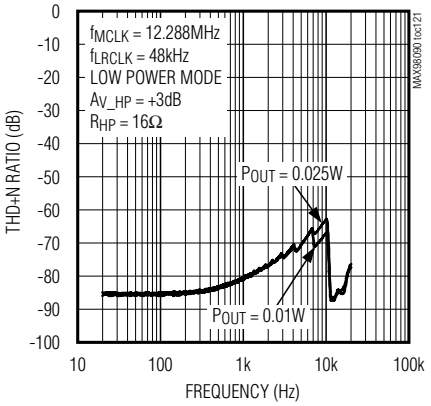
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT (CONTINUED)

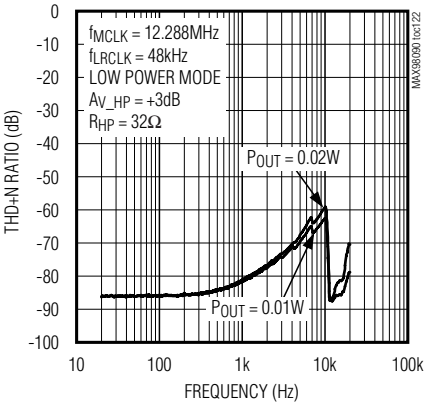
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)**



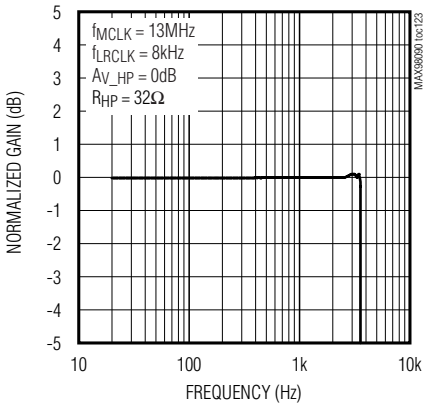

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)**



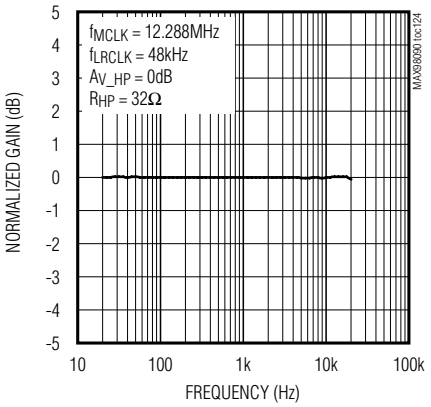

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DAC TO HEADPHONE)**



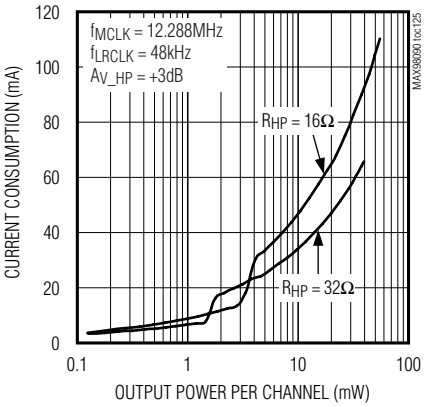

**GAIN vs. FREQUENCY (DAC TO HEADPHONE)**




**GAIN vs. FREQUENCY (LINE TO HEADPHONE)**




**POWER CONSUMPTION vs. OUTPUT POWER (DAC TO HEADPHONE)**

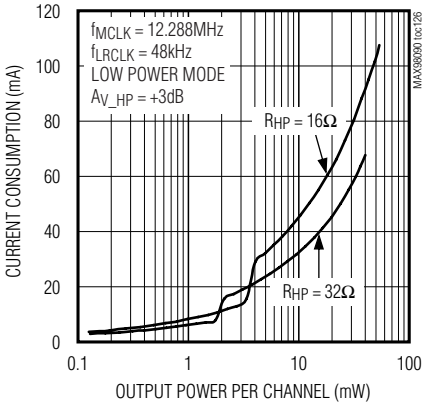


## 典型工作特性(续)

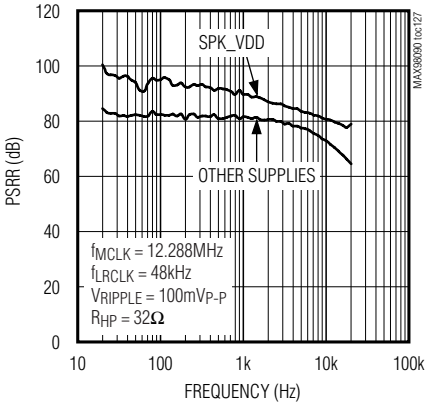
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT (CONTINUED)

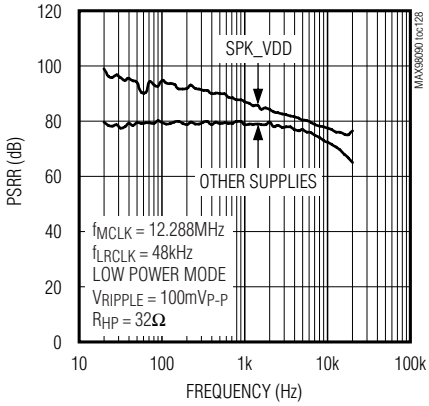
**POWER CONSUMPTION vs. OUTPUT POWER (DAC TO HEADPHONE)**



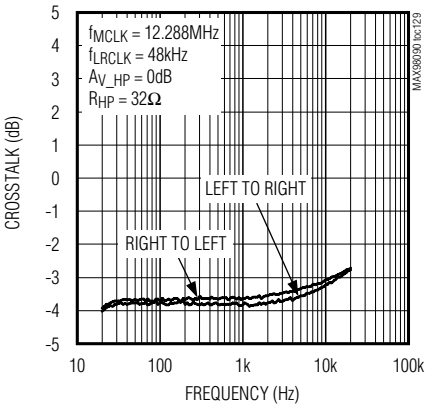

**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)**



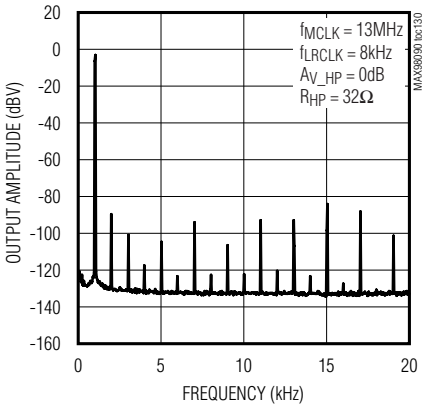

**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)**



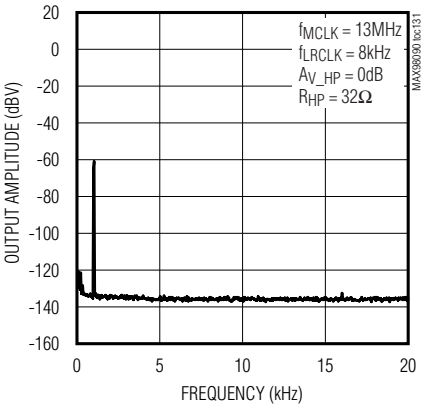

**CROSSTALK vs. FREQUENCY (DAC TO HEADPHONE)**




**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO HEADPHONE)**




**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)**

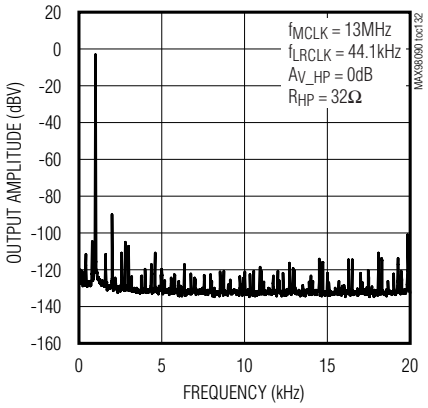


## 典型工作特性(续)

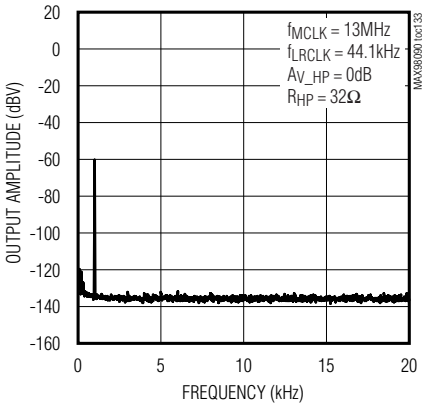
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT (CONTINUED)

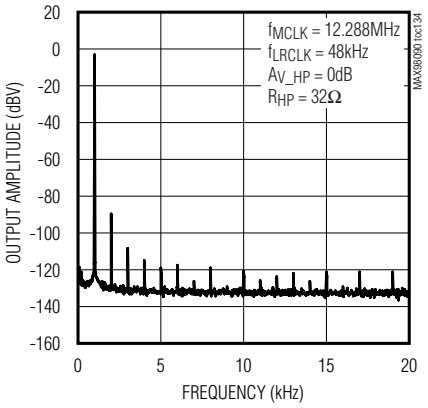
**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO HEADPHONE)**



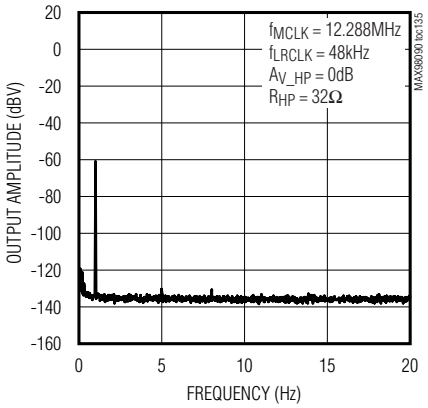

**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)**



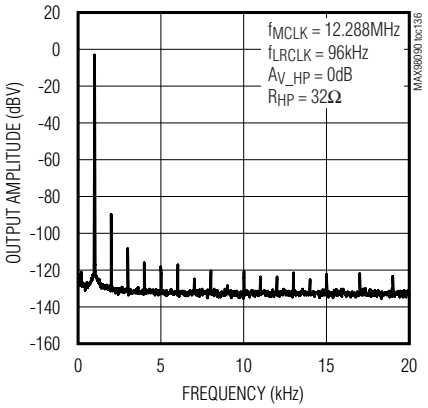

**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)**



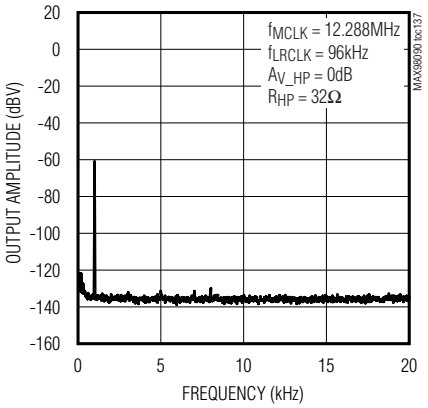

**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)**




**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (DAC TO HEADPHONE)**




**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)**

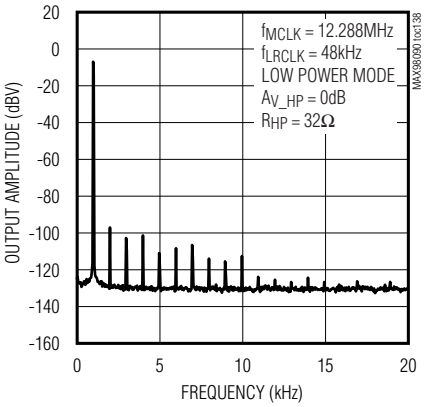


## 典型工作特性(续)

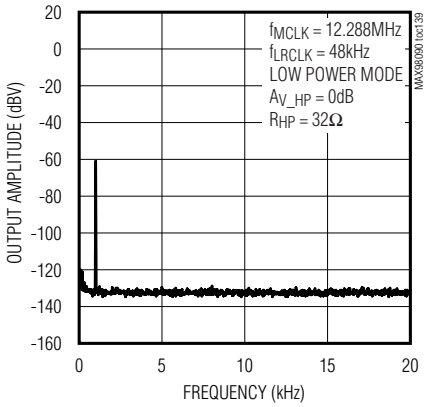
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### DAC PLAYBACK PATH INPUT TO HEADPHONE OUTPUT (CONTINUED)

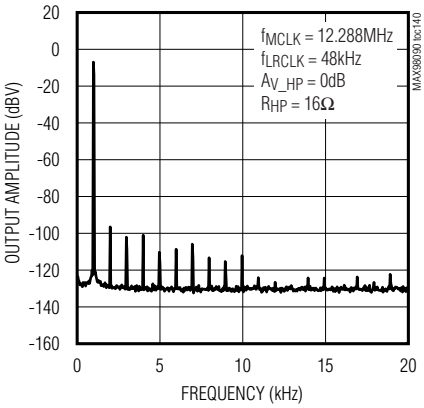
**INBAND OUTPUT SPECTRUM, -6dBFS INPUT (DAC TO HEADPHONE)**



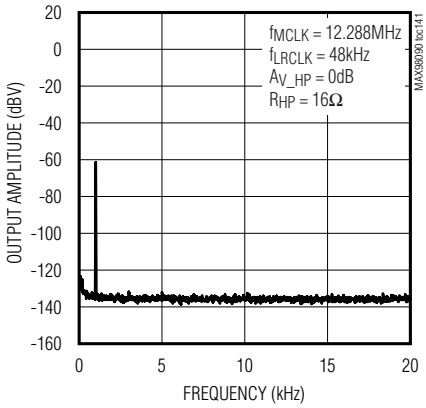

**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)**




**INBAND OUTPUT SPECTRUM, -6dBFS INPUT (DAC TO HEADPHONE)**




**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (DAC TO HEADPHONE)**

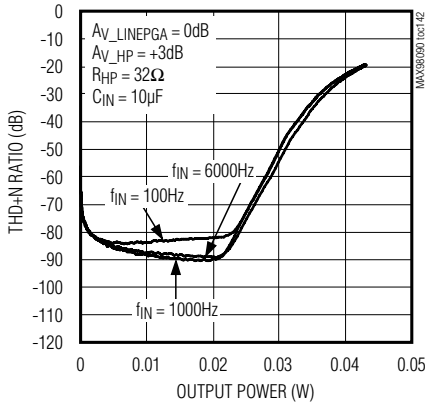


## 典型工作特性(续)

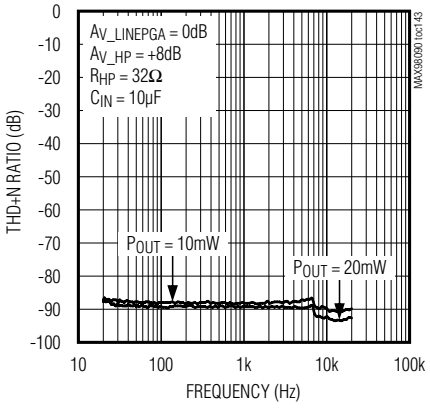
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### LINE INPUT TO HEADPHONE OUTPUT

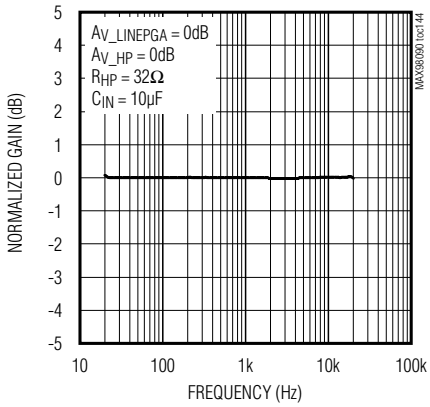
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (LINE TO HEADPHONE)**



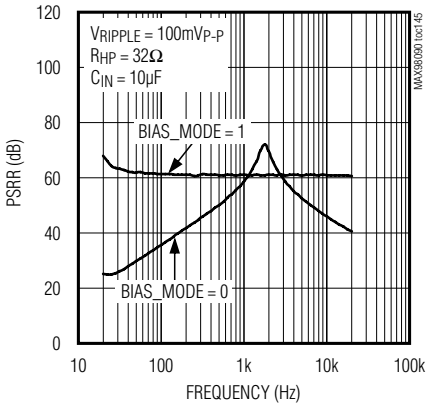

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (LINE TO HEADPHONE)**




**GAIN vs. FREQUENCY (LINE TO HEADPHONE)**




**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (LINE TO HEADPHONE)**

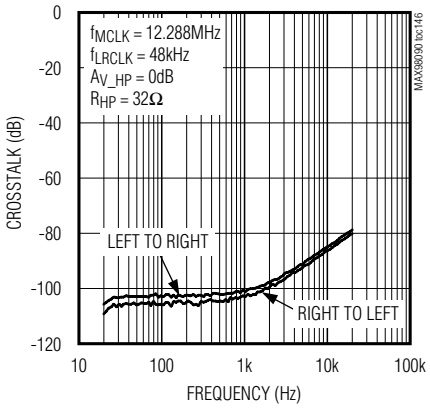


## 典型工作特性(续)

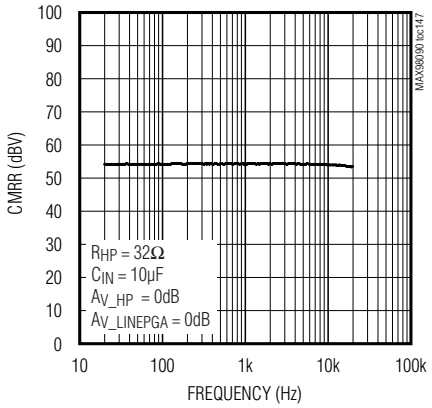
($V_{AVDD}$ = $V_{HPVDD}$ = $V_{DVDDIO}$ = 1.8V, $V_{DVDD}$ = 1.2V, $V_{SPKLVDD}$ = $V_{SPKRVDD}$ = $V_{SPKVDD}$ = 3.7V. Receiver load ($R_{RCV}$) connected between RCVP/LOUTL and RCVN/LOUTR (LINMOD = 0). Line output loads ($R_{LOUT}$) connected between from RCVP/LOUTL and RCVN/LOUTR to GND (LINMOD = 1). Headphone loads ($R_{HP}$) connected from HPL or HPR to GND. Speaker loads ($Z_{SPK}$) connected between SPK_P and SPK_N. $R_{RCV}$ = ∞, $R_{LOUT}$ = ∞, $R_{HP}$ = ∞, $Z_{SPK}$ = ∞. $C_{REF}$ = 2.2µF, $C_{BIAS}$ = $C_{MICBIAS}$ = 1µF, $C_{C1N-C1P}$ = $C_{CPVDD}$ = $C_{CPVSS}$ = 1µF. $A_{V\_MICPRE\_}$ = $A_{V\_MICPGA\_}$ = $A_{V\_LINEPGA\_}$ = 0dB, $A_{V\_ADCLVL}$ = $A_{V\_ADCGAIN}$ = 0dB, $A_{V\_DACLVL}$ = $A_{V\_DACGAIN}$ = 0dB, $A_{V\_MIXGAIN}$ = 0dB, $A_{V\_RCV}$ = $A_{V\_LOUT}$ = $A_{V\_HP}$ = $A_{V\_SPK}$ = 0dB. $f_{MCLK}$ = 12.288MHz, $f_{LRCLK}$ = 48kHz, MAS = 0, 20-bit source data. $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

### LINE INPUT TO HEADPHONE OUTPUT (CONTINUED)

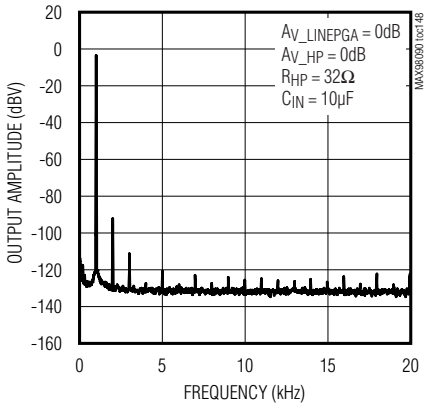
**CROSSTALK vs. FREQUENCY (LINE TO HEADPHONE)**



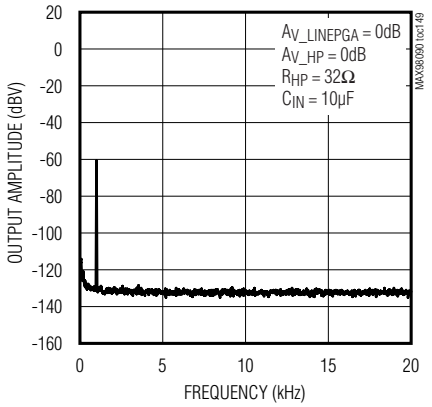

**COMMON-MODE REJECTION RATIO vs. FREQUENCY (LINE TO HEADPHONE)**



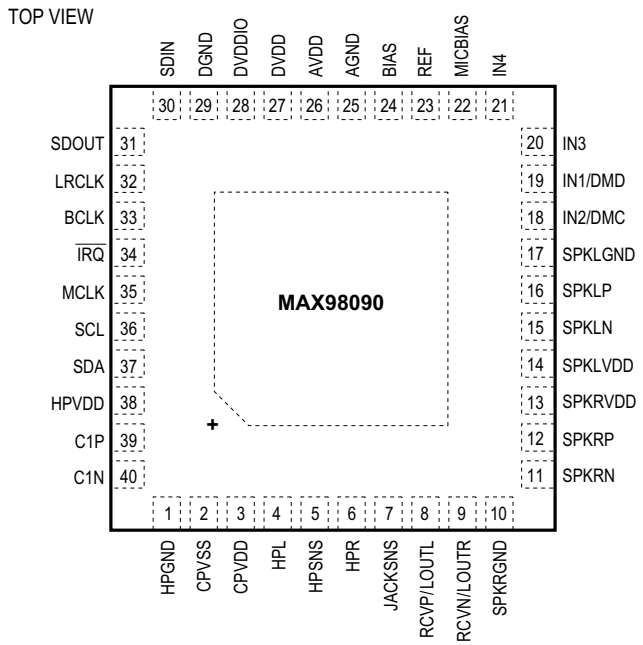

**INBAND OUTPUT SPECTRUM, -3dBFS INPUT (LINE TO HEADPHONE)**




**INBAND OUTPUT SPECTRUM, -60dBFS INPUT (LINE TO HEADPHONE)**



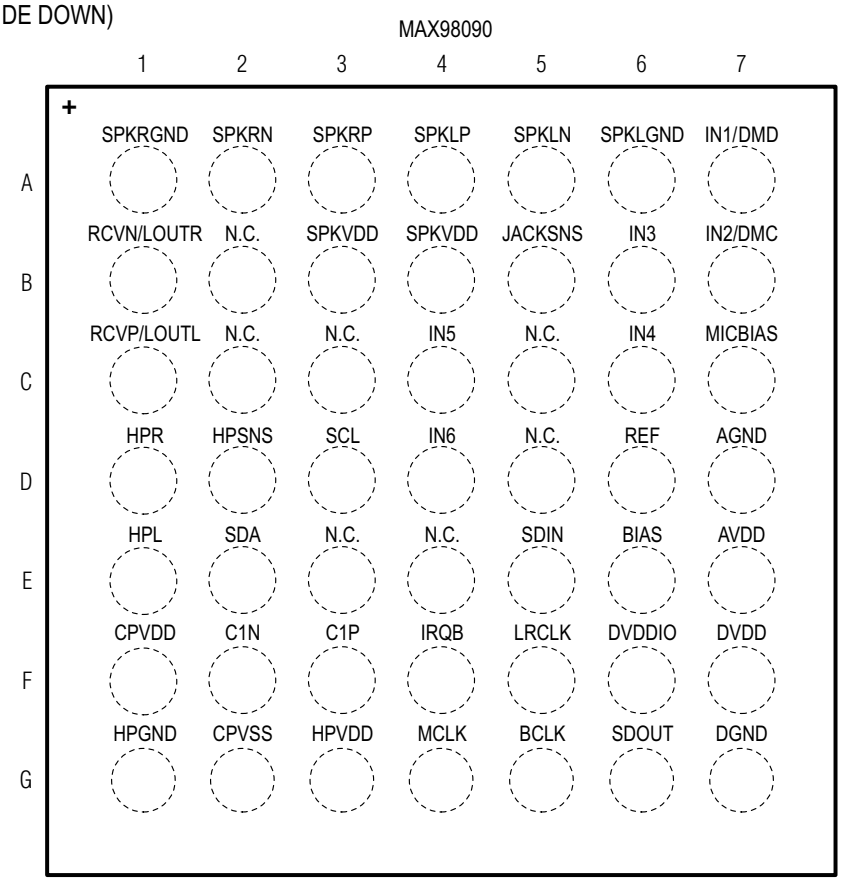
## 焊球/引脚配置




**TQFN**
**(5mm x 5mm x 0.75mm)**

## 焊球/引脚配置(续)

TOP VIEW
(BUMP SIDE DOWN)




**WLP**
**(3.15mm x 3.15 mm, 0.4 PITCH)**

## 焊球/引脚说明

| 引脚 TQFN | 焊球 WLP | MAX98090 | 功能 |
|---|---|---|---|
| 1 | G1 | HPGND | 耳机地。 |
| 2 | G2 | CPVSS | 电荷泵反相输出，利用1µF陶瓷电容旁路至HPGND。 |
| 3 | F1 | CPVDD | 电荷泵同相输出，利用1µF陶瓷电容旁路至HPGND。 |
| 4 | E1 | HPL | 左声道耳机输出。 |
| 5 | D2 | HPSNS | 耳机放大器地检测，连接至耳机插孔地端子，或连接至地。 |
| 6 | D1 | HPR | 右声道耳机输出。 |
| 7 | B5 | JACKSNS | 插孔检测输入，连接至耳机插孔的麦克风端，以检测插孔动作。 |
| 8 | C1 | RCVP/LOUTL | 听筒放大器输出正端/左声道线出。 |
| 9 | B1 | RCVN/LOUTR | 听筒放大器输出负端/右声道线出。 |
| 10 | A1 | SPKRGND | 右声道扬声器放大器地。 |
| 11 | A2 | SPKRN | 右声道D类扬声器输出负端。 |
| 12 | A3 | SPKRP | 右声道D类扬声器输出正端。 |
| 13 | — | SPKRVDD | 右声道扬声器电源，利用1µF电容旁路至SPKRGND。 |
| 14 | — | SPKLVDD | 左声道扬声器和麦克风偏置电源，利用1µF电容旁路至SPKLGND。 |
| 15 | A5 | SPKLN | 左声道D类扬声器输出负端。 |
| 16 | A4 | SPKLP | 左声道D类扬声器输出正端。 |
| 17 | A6 | SPKLGND | 左声道扬声器放大器地。 |
| 18 | B7 | IN2/DMC | 差分麦克风1输入正端或单端线入2，串联一个1µF电容进行交流耦合。可重新配置为数字麦克风时钟输出。 |
| 19 | A7 | IN1/DMD | 差分麦克风1输入负端或单端线入1，串联一个1µF电容进行交流耦合。可重新配置为数字麦克风数据输入。 |
| 20 | B6 | IN3 | 差分麦克风2输入负端或单端线入3，串联一个1µF电容进行交流耦合。 |
| 21 | C6 | IN4 | 差分麦克风2输入正端或单端线入4，串联一个1µF电容进行交流耦合。 |
| 22 | C7 | MICBIAS | 低噪声偏置电压，偏置电压可设置。应采用2.2kΩ至1kΩ的外部电阻设置麦克风电流。 |
| 23 | D6 | REF | 转换器基准，利用2.2µF电容旁路至AGND。 |
| 24 | E6 | BIAS | 共模基准电压，利用1µF电容旁路至AGND。 |
| 25 | D7 | AGND | 模拟地。 |
| 26 | E7 | AVDD | 模拟电源，利用1µF电容旁路至AGND。 |
| 27 | F7 | DVDD | 数字电源，利用1µF电容旁路至DGND。 |
| 28 | F6 | DVDDIO | 数字音频接口电源输入，利用1µF电容旁路至DGND。 |

## 焊球/引脚说明(续)

| 引脚 TQFN | 焊球 WLP | MAX98090 | 功能 |
|---|---|---|---|
| 29 | G7 | DGND | 数字地。 |
| 30 | E5 | SDIN | 数字音频串行数据回放输入。 |
| 31 | G6 | SDOUT | 数字音频串行数据录音输出，输出电压以DVDDIO为基准。 |
| 32 | F5 | LRCLK | 数字音频左、右声道的时钟输入/输出。LRCLK为音频采样率时钟，决定音频数据是否送至左声道或右声道。TDM模式下，LRCLK为帧同步脉冲。LRCLK在器件处于从模式时为输入，在主机模式下作为输出。 |
| 33 | G5 | BCLK | 数字音频的位时钟输入/输出。BCLK在器件处于从模式时为输入，在主机模式下作为输出。输入/输出电压以DVDDIO为基准。 |
| 34 | F4 | IRQ | 低电平有效硬中断输出，通过10kΩ上拉电阻连接至$V_{DD}$。 |
| 35 | G4 | MCLK | 主机时钟输入，支持256 x $f_S$或10MHz至60MHz的输入频率范围。 |
| 36 | D3 | SCL | $I^2C$串行时钟输入，通过一个上拉电阻连接至DVDD，实现满幅输出。 |
| 37 | E2 | SDA | $I^2C$串行数据输入/输出。通过一个上拉电阻连接至DVDD，实现满幅输出。 |
| 38 | G3 | HPVDD | 耳机电源，利用1µF电容旁路至HPGND。 |
| 39 | F3 | C1P | 电荷泵飞电容正端，在C1N和C1P之间连接1µF陶瓷电容。 |
| 40 | F2 | C1N | 电荷泵飞电容负端，在C1N和C1P之间连接1µF陶瓷电容。 |
| — | B3, B4 | SPKVDD | 扬声器和麦克风偏置电源，利用1µF电容旁路至SPK_GND。 |
| — | C4 | IN5 | 辅助差分麦克风输入负端或单端线入，串联一个1µF电容进行交流耦合。 |
| — | D4 | IN6 | 辅助差分麦克风输入正端或单端线入，串联一个1µF电容进行交流耦合。 |
| — | B2, C2, C3, C5, D5, E3, E4 | N.C. | 内部无连接。 |

## 详细说明

MAX98090为完全集成的立体声音频编解码器，采用FlexSound音频处理技术，内置输入和输出音频放大器。

器件具有六路(WLP封装)或四路(TQFN封装)灵活的模拟输入，每对输入可配置为差分模拟麦克风输入、立体声单端或差分线入，或者直接差分输入至ADC混音器，以降低功耗。IN1/IN2输入也可重新配置用于支持两个数字麦克风，所以可同时对两个麦克风信号(模拟或数字)进行录音。输入模拟信号增益高达50dB，由立体声ADC录音或直接送至模拟输出混音器回放。

ADC支持8kHz至96kHz范围的采样率，具有两种性能模式，提供两种过采样率选项。ADC至DAI数字录音通路具有语音(IIR)和音乐(FIR)滤波、可选隔直流高通滤波器、完全可配置的双二阶滤波器以及12dB至+45dB范围的可编程数字增益和电平控制。

数字音频接口(DAI)可同时发送、接收独立的或截然不同的立体声音频信号。DAI支持各种PCM数字音频格式，包括$I^2S$、左对齐(LJ)、右对齐(RJ)，以及四时隙TDM。

利用录音通路，DAI至DAC回放通路支持8kHz至96kHz范围的采样率、语音(IIR)和音乐(FIR)滤波($f_S/2$时高阻带衰减)、可选隔直滤波器，以及-15dB至+18dB范围的可编程数字增益和电平控制。此外，回放通路也具有7波段参数均衡器、动态范围控制(DRC)，以及来自于录音通路DSP的数字侧音求和。器件包括三个模拟输出驱动器。第一个为AB类差分接收器/听筒放大器，接收器放大器也可配置为立体声单端线出驱动器。

第二个为集成的无滤波、D类立体声扬声器放大器，该放大器为两个扬声器提供高效放大，包括有源辐射抑制电路，有效降低D类放大器的EMI辐射。右声道具有从模式，此时切换方法与左声道同步，以消除异步工作中发生的拍音。在大多数扬声器走线较短的系统中，要求D类输出滤波。

第三个为H类立体声麦克风放大器，以地为参考，采用Maxim的第二代DirectDrive架构。H类麦克风放大器具有内置电荷泵，为耳机放大器产生正、负电源，这样就提供了以地为参考的输出信号，从而省去了隔直流电容或耳机插孔地回路的中心电压偏置。耳机专用的地回路检测电流可减小串扰和输出噪声。跟踪电路监测信号电平并自动选择正确的开关频率和电源电压。对于较低电平的信号，电荷泵以较低的频率进行开关，输出$\pm V_{HPVDD}/2$，以提高效率；当信号幅值增大时，电荷泵开关频率也增大，继续输出$\pm V_{HPVDD}/2$。对于较高电平的信号，电荷泵输出满幅电源轨$\pm V_{HPVDD}$，输出功率最大化。

器件也包括多项附加功能，例如可编程外部麦克风偏置、可配置插孔检测和识别、外部咔嗒/噼噗声抑制电路、电源和性能管理设置，以及齐全的快速配置选项。

## 器件$I^2C$寄存器映射

表1列出了全部寄存器及其地址和上电复位(PoR)状态，寄存器0x01、0x02和0xFF为只读，寄存器0x00及其它全部寄存器为可读/写。除非另外说明，更新表中任何寄存器时，向未使用的位写入0。

## 表1. MAX98090控制寄存器

| REGISTER DESCRIPTION | | | REGISTER CONTENTS | | | | | | | | POR STATE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | NAME | R/W | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| **RESET/STATUS/INTERRUPT REGISTERS** | | | | | | | | | | | |
| 0x00 | SOFTWARE RESET | W | SWRESET | — | — | — | — | — | — | — | 0x00 |
| 0x01 | DEVICE STATUS | CoR | CLD | SLD | ULK | — | — | JDET | DRCACT | DRCCLP | 0x00 |
| 0x02 | JACK STATUS | R | — | — | — | — | — | LSNS | JKSNS | — | 0x00 |
| 0x03 | INTERUPT MASKS | R/W | ICLD | ISLD | IULK | — | — | IJDET | IDRCACT | IDRCCLP | 0x04 |
| **QUICK SETUP REGISTERS** | | | | | | | | | | | |
| 0x04 | SYSTEM CLOCK | W | 26M | 19P2M | 13M | 12P288M | 12M | 11P2896M | — | $256F_S$ | 0x00 |
| 0x05 | SAMPLE RATE | W | — | — | SR_96K | SR_32K | SR_48K | SR_44K1 | SR_16K | SR_8K | 0x00 |
| 0x06 | DAI INTERFACE | W | — | — | RJ_M | RJ_S | LJ_M | LJ_S | I2S_M | I2S_S | 0x00 |
| 0x07 | DAC PATH | W | DIG2_HP | DIG2_ EAR | DIG2_ SPK | DIG2_ LOUT | — | — | — | — | 0x00 |
| 0x08 | MIC/DIRECT TO ADC | W | IN12_MIC1 | IN34_ MIC2 | — | — | IN12_ DADC | IN34_ DADC | ***IN56_ DADC*** | — | 0x00 |
| 0x09 | LINE TO ADC | W | IN12S_AB | IN34S_AB | ***IN56S_AB*** | IN34D_A | ***IN65D_B*** | — | — | — | 0x00 |
| 0x0A | ANALOG MIC LOOP | W | IN12_ M1HPL | IN12_ M1SPKL | IN12_ M1EAR | IN12_ M1LOUTL | IN34_ M2HPR | IN34_ M2SPKR | IN34_ M2EAR | IN34_ M2LOUTR | 0x00 |
| 0x0B | ANALOG LINE LOOP | W | IN12S_ ABHP | IN34D_ ASPKL | IN34D_ AEAR | IN12S_ ABLOUT | IN34S_ ABHP | ***IN65D _BSPKR*** | ***IN65D_ BEAR*** | IN34S_ ABLOUT | 0x00 |
| **RESERVED REGISTER** | | | | | | | | | | | |
| 0x0C | RESERVED | — | — | — | — | — | — | — | — | — | 0x00 |
| **ANALOG INPUT CONFIGURATION REGISTERS** | | | | | | | | | | | |
| 0x0D | LINE INPUT CONFIG. | R/W | IN34DIFF | ***IN65DIFF*** | IN1SEEN | IN2SEEN | IN3SEEN | IN4SEEN | ***IN5SEEN*** | ***IN6SEEN*** | 0x00 |
| 0x0E | LINE INPUT LEVEL | R/W | MIXG135 | MIXG246 | LINAPGA[2:0] | | | LINBPGA[2:0] | | | 0x1B |
| 0x0F | INPUT MODE | R/W | EXTBUFA | EXTBUFB | — | — | — | — | ***EXT_MIC[1:0]*** | | 0x00 |
| 0x10 | MIC1 INPUT LEVEL | R/W | — | PA1EN[1:0] | PGAM1[4:0] | | | | | | 0x14 |
| 0x11 | MIC2 INPUT LEVEL | R/W | — | PA2EN[1:0] | PGAM2[4:0] | | | | | | 0x14 |
| **MICROPHONE CONFIGURATION REGISTERS** | | | | | | | | | | | |
| 0x12 | MIC BIAS VOLTAGE | R/W | — | — | — | — | — | — | MBVSEL[1:0] | | 0x00 |
| 0x13 | DIGITAL MIC ENABLE | R/W | — | MICCLK[2:0] | | | — | — | DIGMICR | DIGMICL | 0x00 |
| 0x14 | DIGITAL MIC CONFIG. | R/W | DMIC_COMP[3:0] | | | | — | — | DMIC_FREQ[1:0] | | 0x00 |

***注：****用**粗斜体**表示的寄存器位仅限WLP封装。*

表1. MAX98090控制寄存器(续)

| REGISTER DESCRIPTION | | | REGISTER CONTENTS | | | | | | | | POR STATE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | NAME | R/W | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| **ADC PATH AND CONFIGURATION REGISTERS** | | | | | | | | | | | |
| 0x15 | LEFT ADC MIXER | R/W | — | MIXADL[6:0] | | | | | | | 0x00 |
| 0x16 | RIGHT ADC MIXER | R/W | — | MIXADR[6:0] | | | | | | | 0x00 |
| 0x17 | LEFT RECORD LEVEL | R/W | — | AVLG[2:0] | | | AVL[3:0] | | | | 0x03 |
| 0x18 | RIGHT RECORD LEVEL | R/W | — | AVRG[2:0] | | | AVR[3:0] | | | | 0x03 |
| 0x19 | RECORD BIQUAD LEVEL | R/W | — | — | — | — | AVBQ[3:0] | | | | 0x00 |
| 0x1A | RECORD SIDETONE | R/W | DSTS[1:0] | | — | DVST[4:0] | | | | | 0x00 |
| **CLOCK CONFIGURATION REGISTERS** | | | | | | | | | | | |
| 0x1B | SYSTEM CLOCK | R/W | — | — | PSCLK[1:0] | | — | — | — | — | 0x00 |
| 0x1C | CLOCK MODE | R/W | FREQ[3:0] | | | | — | — | — | USE_MI | 0x00 |
| 0x1D | CLOCK RATIO NI MSB | R/W | — | NI[14:8] | | | | | | | 0x00 |
| 0x1E | CLOCK RATIO NI LSB | R/W | NI[7:0] | | | | | | | | 0x00 |
| 0x1F | CLOCK RATIO MI MSB | R/W | MI[15:8] | | | | | | | | 0x00 |
| 0x20 | CLOCK RATIO MI LSB | R/W | MI[7:0] | | | | | | | | 0x00 |
| 0x21 | MASTER MODE | R/W | MAS | — | — | — | — | BSEL[2:0] | | | 0x00 |
| **INTERFACE CONTROL REGISTERS** | | | | | | | | | | | |
| 0x22 | INTERFACE FORMAT | R/W | — | — | RJ | WCI | BCI | DLY | WS[1:0] | | 0x00 |
| 0x23 | TDM CONTROL | R/W | — | — | — | — | — | — | FSW | TDM | 0x00 |
| 0x24 | TDM FORMAT | R/W | SLOTL[1:0] | | SLOTR[1:0] | | SLOTDLY[3:0] | | | | 0x00 |
| 0x25 | I/O CONFIGURATION | R/W | — | — | LTEN | LBEN | DMONO | HIZOFF | SDOEN | SDIEN | 0x00 |
| 0x26 | FILTER CONFIGURATION | R/W | MODE | AHPF | DHPF | DHF | — | — | — | — | 0x80 |
| 0x27 | DAI PLAYBACK LEVEL | R/W | DVM | — | DVG[1:0] | | DV[3:0] | | | | 0x00 |
| 0x28 | EQ PLAYBACK LEVEL | R/W | — | — | — | $\overline{\text{EQCLP}}$ | DVEQ[3:0] | | | | 0x00 |

表1. MAX98090控制寄存器(续)

| REGISTER DESCRIPTION | | | REGISTER CONTENTS | | | | | | | | POR STATE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | NAME | R/W | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| **HEADPHONE (HP) CONTROL REGISTERS** | | | | | | | | | | | |
| 0x29 | LEFT HP MIXER | R/W | — | — | MIXHPL[5:0] | | | | | | 0x00 |
| 0x2A | RIGHT HP MIXER | R/W | — | — | MIXHPR[5:0] | | | | | | 0x00 |
| 0x2B | HP CONTROL | R/W | — | — | MIXHP RSEL | MIXHP LSEL | MIXHPRG[1:0] | | MIXHPLG[1:0] | | 0x00 |
| 0x2C | LEFT HP VOLUME | R/W | HPLM | — | — | HPVOLL[4:0] | | | | | 0x1A |
| 0x2D | RIGHT HP VOLUME | R/W | HPRM | — | — | HPVOLR[4:0] | | | | | 0x1A |
| **SPEAKER (SPK) CONFIGURATION REGISTERS** | | | | | | | | | | | |
| 0x2E | LEFT SPK MIXER | R/W | — | — | MIXSPL[5:0] | | | | | | 0x00 |
| 0x2F | RIGHT SPK MIXER | R/W | — | SPK_ SLAVE | MIXSPR[5:0] | | | | | | 0x00 |
| 0x30 | SPK CONTROL | R/W | — | — | — | — | MIXSPRG[1:0] | | MIXSPLG[1:0] | | 0x00 |
| 0x31 | LEFT SPK VOLUME | R/W | SPLM | — | SPVOLL[5:0] | | | | | | 0x2C |
| 0x32 | RIGHT SPK VOLUME | R/W | SPRM | — | SPVOLR[5:0] | | | | | | 0x2C |
| **DYNAMIC RANGE CONTROL (DRC) CONFIGURATION REGISTERS** | | | | | | | | | | | |
| 0x33 | DRC TIMING | R/W | DRCEN | DRCRLS[2:0] | | | — | DRCATK[2:0] | | | 0x00 |
| 0x34 | DRC COMPRESSOR | R/W | DRCCMP[2:0] | | | DRCTHC[4:0] | | | | | 0x00 |
| 0x35 | DRC EXPANDER | R/W | DRCEXP[2:0] | | | DRCTHE[4:0] | | | | | 0x00 |
| 0x36 | DRC GAIN | R/W | — | — | — | DRCG[4:0] | | | | | 0x00 |
| **RECEIVER (RCV OR EARPIECE) AND LINE OUTPUT (LOUT) REGISTERS** | | | | | | | | | | | |
| 0x37 | RCV/LOUTL MIXER | R/W | — | — | MIXRCVL[5:0] | | | | | | 0x00 |
| 0x38 | RCV/LOUTL CONTROL | R/W | — | — | — | — | — | — | MIXRCVLG[1:0] | | 0x00 |
| 0x39 | RCV/LOUTL VOLUME | R/W | RCVLM | — | — | RCVLVOL[4:0] | | | | | 0x15 |
| 0x3A | LOUTR MIXER | R/W | LINMOD | — | MIXRCVR[5:0] | | | | | | 0x00 |
| 0x3B | LOUTR CONTROL | R/W | — | — | — | — | — | — | MIXRCVRG[1:0] | | 0x00 |
| 0x3C | LOUTR VOLUME | R/W | RCVRM | — | — | RCVRVOL[4:0] | | | | | 0x15 |
| **JACK DETECT AND ENABLE REGISTERS** | | | | | | | | | | | |
| 0x3D | JACK DETECT | R/W | JDETEN | JDWK | — | — | — | — | JDEB[1:0] | | 0x00 |
| 0x3E | INPUT ENABLE | R/W | — | — | — | MBEN | LINEAEN | LINEBEN | ADREN | ADLEN | 0x00 |
| 0x3F | OUTPUT ENABLE | R/W | HPREN | HPLEN | SPREN | SPLEN | RCVLEN | RCVREN | DAREN | DALEN | 0x00 |
| 0x40 | LEVEL CONTROL | R/W | — | — | — | — | — | $\overline{\text{ZDEN}}$ | $\overline{\text{VS2EN}}$ | $\overline{\text{VSEN}}$ | 0x00 |

表1. MAX98090控制寄存器(续)

| REGISTER DESCRIPTION | | | REGISTER CONTENTS | | | | | | | | POR STATE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | NAME | R/W | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| 0x41 | DSP FILTER ENABLE | R/W | — | — | — | — | RECBQEN | EQ3BANDEN | EQ5BANDEN | EQ7BANDEN | 0x00 |
| **BIAS AND POWER MODE CONFIGURATION REGISTERS** | | | | | | | | | | | |
| 0x42 | BIAS CONTROL | R/W | — | — | — | — | — | — | — | BIAS_MODE | 0x00 |
| 0x43 | DAC CONTROL | R/W | — | — | — | — | — | — | PERF MODE | DACHP | 0x00 |
| 0x44 | ADC CONTROL | R/W | — | — | — | — | — | OSR128 | ADC DITHER | ADCHP | 0x06 |
| 0x45 | DEVICE SHUTDOWN | R/W | $\overline{\text{SHDN}}$ | — | — | — | — | — | — | — | 0x00 |
| **PLAYBACK PARAMETRIC EQUALIZER BAND 1: BIQUAD FILTER COEFFICIENT REGISTERS** | | | | | | | | | | | |
| 0x46 | EQUALIZER BAND 1 COEFFICIENT B0 | R/W | B0_1[23:16] | | | | | | | | — |
| 0x47 | | R/W | B0_1[15:8] | | | | | | | | — |
| 0x48 | | R/W | B0_1[7:0] | | | | | | | | — |
| 0x49 | EQUALIZER BAND 1 COEFFICIENT B1 | R/W | B1_1[23:16] | | | | | | | | — |
| 0x4A | | R/W | B1_1[15:8] | | | | | | | | — |
| 0x4B | | R/W | B1_1[7:0] | | | | | | | | — |
| 0x4C | EQUALIZER BAND 1 COEFFICIENT B2 | R/W | B2_1[23:16] | | | | | | | | — |
| 0x4D | | R/W | B2_1[15:8] | | | | | | | | — |
| 0x4E | | R/W | B2_1[7:0] | | | | | | | | — |
| 0x4F | EQUALIZER BAND 1 COEFFICIENT A1 | R/W | A1_1[23:16] | | | | | | | | — |
| 0x50 | | R/W | A1_1[15:8] | | | | | | | | — |
| 0x51 | | R/W | A1_1[7:0] | | | | | | | | — |
| 0x52 | EQUALIZER BAND 1 COEFFICIENT A2 | R/W | A2_1[23:16] | | | | | | | | — |
| 0x53 | | R/W | A2_1[15:8] | | | | | | | | — |
| 0x54 | | R/W | A2_1[7:0] | | | | | | | | — |

表1. MAX98090控制寄存器(续)

| REGISTER DESCRIPTION | | | REGISTER CONTENTS | | | | | | | | POR STATE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | NAME | R/W | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| PLAYBACK PARAMETRIC EQUALIZER BAND 2: BIQUAD FILTER COEFFICIENT REGISTERS | | | | | | | | | | | |
| 0x55 | EQUALIZER BAND 2 COEFFICIENT B0 | R/W | B0_2[23:16] | | | | | | | | — |
| 0x56 | | R/W | B0_2[15:8] | | | | | | | | — |
| 0x57 | | R/W | B0_2[7:0] | | | | | | | | — |
| 0x58 | EQUALIZER BAND 2 COEFFICIENT B1 | R/W | B1_2[23:16] | | | | | | | | — |
| 0x59 | | R/W | B1_2[15:8] | | | | | | | | — |
| 0x5A | | R/W | B1_2[7:0] | | | | | | | | — |
| 0x5B | EQUALIZER BAND 2 COEFFICIENT B2 | R/W | B2_2[23:16] | | | | | | | | — |
| 0x5C | | R/W | B2_2[15:8] | | | | | | | | — |
| 0x5D | | R/W | B2_2[7:0] | | | | | | | | — |
| 0x5E | EQUALIZER BAND 2 COEFFICIENT A1 | R/W | A1_2[23:16] | | | | | | | | — |
| 0x5F | | R/W | A1_2[15:8] | | | | | | | | — |
| 0x60 | | R/W | A1_2[7:0] | | | | | | | | — |
| 0x61 | EQUALIZER BAND 2 COEFFICIENT A2 | R/W | A2_2[23:16] | | | | | | | | — |
| 0x62 | | R/W | A2_2[15:8] | | | | | | | | — |
| 0x63 | | R/W | A2_2[7:0] | | | | | | | | — |
| PLAYBACK PARAMETRIC EQUALIZER BAND 3: BIQUAD FILTER COEFFICIENT REGISTERS | | | | | | | | | | | |
| 0x64 | EQUALIZER BAND 3 COEFFICIENT B0 | R/W | B0_3[23:16] | | | | | | | | — |
| 0x65 | | R/W | B0_3[15:8] | | | | | | | | — |
| 0x66 | | R/W | B0_3[7:0] | | | | | | | | — |
| 0x67 | EQUALIZER BAND 3 COEFFICIENT B1 | R/W | B1_3[23:16] | | | | | | | | — |
| 0x68 | | R/W | B1_3[15:8] | | | | | | | | — |
| 0x69 | | R/W | B1_3[7:0] | | | | | | | | — |
| 0x6A | EQUALIZER BAND 3 COEFFICIENT B2 | R/W | B2_3[23:16] | | | | | | | | — |
| 0x6B | | R/W | B2_3[15:8] | | | | | | | | — |
| 0x6C | | R/W | B2_3[7:0] | | | | | | | | — |
| 0x6D | EQUALIZER BAND 3 COEFFICIENT A1 | R/W | A1_3[23:16] | | | | | | | | — |
| 0x6E | | R/W | A1_3[15:8] | | | | | | | | — |
| 0x6F | | R/W | A1_3[7:0] | | | | | | | | — |
| 0x70 | EQUALIZER BAND 3 COEFFICIENT A2 | R/W | A2_3[23:16] | | | | | | | | — |
| 0x71 | | R/W | A2_3[15:8] | | | | | | | | — |
| 0x72 | | R/W | A2_3[7:0] | | | | | | | | — |

表1. MAX98090控制寄存器(续)

| REGISTER DESCRIPTION | | | REGISTER CONTENTS | | | | | | | | POR STATE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | NAME | R/W | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| PLAYBACK PARAMETRIC EQUALIZER BAND 4: BIQUAD FILTER COEFFICIENT REGISTERS | | | | | | | | | | | |
| 0x73 | EQUALIZER BAND 4 COEFFICIENT B0 | R/W | B0_4[23:16] | | | | | | | | — |
| 0x74 | | R/W | B0_4[15:8] | | | | | | | | — |
| 0x75 | | R/W | B0_4[7:0] | | | | | | | | — |
| 0x76 | EQUALIZER BAND 4 COEFFICIENT B1 | R/W | B1_4[23:16] | | | | | | | | — |
| 0x77 | | R/W | B1_4[15:8] | | | | | | | | — |
| 0x78 | | R/W | B1_4[7:0] | | | | | | | | — |
| 0x79 | EQUALIZER BAND 4 COEFFICIENT B2 | R/W | B2_4[23:16] | | | | | | | | — |
| 0x7A | | R/W | B2_4[15:8] | | | | | | | | — |
| 0x7B | | R/W | B2_4[7:0] | | | | | | | | — |
| 0x7C | EQUALIZER BAND 4 COEFFICIENT A1 | R/W | A1_4[23:16] | | | | | | | | — |
| 0x7D | | R/W | A1_4[15:8] | | | | | | | | — |
| 0x7E | | R/W | A1_4[7:0] | | | | | | | | — |
| 0x7F | EQUALIZER BAND 4 COEFFICIENT A2 | R/W | A2_4[23:16] | | | | | | | | — |
| 0x80 | | R/W | A2_4[15:8] | | | | | | | | — |
| 0x81 | | R/W | A2_4[7:0] | | | | | | | | — |
| PLAYBACK PARAMETRIC EQUALIZER BAND 5: BIQUAD FILTER COEFFICIENT REGISTERS | | | | | | | | | | | |
| 0x82 | EQUALIZER BAND 5 COEFFICIENT B0 | R/W | B0_5[23:16] | | | | | | | | — |
| 0x83 | | R/W | B0_5[15:8] | | | | | | | | — |
| 0x84 | | R/W | B0_5[7:0] | | | | | | | | — |
| 0x85 | EQUALIZER BAND 5 COEFFICIENT B1 | R/W | B1_5[23:16] | | | | | | | | — |
| 0x86 | | R/W | B1_5[15:8] | | | | | | | | — |
| 0x87 | | R/W | B1_5[7:0] | | | | | | | | — |
| 0x88 | EQUALIZER BAND 5 COEFFICIENT B2 | R/W | B2_5[23:16] | | | | | | | | — |
| 0x89 | | R/W | B2_5[15:8] | | | | | | | | — |
| 0x8A | | R/W | B2_5[7:0] | | | | | | | | — |
| 0x8B | EQUALIZER BAND 5 COEFFICIENT A1 | R/W | A1_5[23:16] | | | | | | | | — |
| 0x8C | | R/W | A1_5[15:8] | | | | | | | | — |
| 0x8D | | R/W | A1_5[7:0] | | | | | | | | — |
| 0x8E | EQUALIZER BAND 5 COEFFICIENT A2 | R/W | A2_5[23:16] | | | | | | | | — |
| 0x8F | | R/W | A2_5[15:8] | | | | | | | | — |
| 0x90 | | R/W | A2_5[7:0] | | | | | | | | — |

表1. MAX98090控制寄存器(续)

| REGISTER DESCRIPTION | | | REGISTER CONTENTS | | | | | | | | POR STATE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | NAME | R/W | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| PLAYBACK PARAMETRIC EQUALIZER BAND 6: BIQUAD FILTER COEFFICIENT REGISTERS | | | | | | | | | | | |
| 0x91 | EQUALIZER BAND 6 COEFFICIENT B0 | R/W | B0_6[23:16] | | | | | | | | — |
| 0x92 | | R/W | B0_6[15:8] | | | | | | | | — |
| 0x93 | | R/W | B0_6[7:0] | | | | | | | | — |
| 0x94 | EQUALIZER BAND 6 COEFFICIENT B1 | R/W | B1_6[23:16] | | | | | | | | — |
| 0x95 | | R/W | B1_6[15:8] | | | | | | | | — |
| 0x96 | | R/W | B1_6[7:0] | | | | | | | | — |
| 0x97 | EQUALIZER BAND 6 COEFFICIENT B2 | R/W | B2_6[23:16] | | | | | | | | — |
| 0x98 | | R/W | B2_6[15:8] | | | | | | | | — |
| 0x99 | | R/W | B2_6[7:0] | | | | | | | | — |
| 0x9A | EQUALIZER BAND 6 COEFFICIENT A1 | R/W | A1_6[23:16] | | | | | | | | — |
| 0x9B | | R/W | A1_6[15:8] | | | | | | | | — |
| 0x9C | | R/W | A1_6[7:0] | | | | | | | | — |
| 0x9D | EQUALIZER BAND 6 COEFFICIENT A2 | R/W | A2_6[23:16] | | | | | | | | — |
| 0x9E | | R/W | A2_6[15:8] | | | | | | | | — |
| 0x9F | | R/W | A2_6[7:0] | | | | | | | | — |
| PLAYBACK PARAMETRIC EQUALIZER BAND 7: BIQUAD FILTER COEFFICIENT REGISTERS | | | | | | | | | | | |
| 0xA0 | EQUALIZER BAND 7 COEFFICIENT B0 | R/W | B0_7[23:16] | | | | | | | | — |
| 0xA1 | | R/W | B0_7[15:8] | | | | | | | | — |
| 0xA2 | | R/W | B0_7[7:0] | | | | | | | | — |
| 0xA3 | EQUALIZER BAND 7 COEFFICIENT B1 | R/W | B1_7[23:16] | | | | | | | | — |
| 0xA4 | | R/W | B1_7[15:8] | | | | | | | | — |
| 0xA5 | | R/W | B1_7[7:0] | | | | | | | | — |
| 0xA6 | EQUALIZER BAND 7 COEFFICIENT B2 | R/W | B2_7[23:16] | | | | | | | | — |
| 0xA7 | | R/W | B2_7[15:8] | | | | | | | | — |
| 0xA8 | | R/W | B2_7[7:0] | | | | | | | | — |
| 0xA9 | EQUALIZER BAND 7 COEFFICIENT A1 | R/W | A1_7[23:16] | | | | | | | | — |
| 0xAA | | R/W | A1_7[15:8] | | | | | | | | — |
| 0xAB | | R/W | A1_7[7:0] | | | | | | | | — |
| 0xAC | EQUALIZER BAND 7 COEFFICIENT A2 | R/W | A2_7[23:16] | | | | | | | | — |
| 0xAD | | R/W | A2_7[15:8] | | | | | | | | — |
| 0xAE | | R/W | A2_7[7:0] | | | | | | | | — |

## 表1. MAX98090控制寄存器(续)

| REGISTER DESCRIPTION | | | REGISTER CONTENTS | | | | | | | | POR STATE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADDR | NAME | R/W | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| RECORD BIQUAD FILTER COEFFICIENT REGISTERS | | | | | | | | | | | |
| 0xAF | RECORD BIQUAD COEFFICIENT B0 | R/W | REC_B0[23:16] | | | | | | | | — |
| 0xB0 | | R/W | REC_B0[15:8] | | | | | | | | — |
| 0xB1 | | R/W | REC_B0[7:0] | | | | | | | | — |
| 0xB2 | RECORD BIQUAD COEFFICIENT B1 | R/W | REC_B1[23:16] | | | | | | | | — |
| 0xB3 | | R/W | REC_B1[15:8] | | | | | | | | — |
| 0xB4 | | R/W | REC_B1[7:0] | | | | | | | | — |
| 0xB5 | RECORD BIQUAD COEFFICIENT B2 | R/W | REC_B2[23:16] | | | | | | | | — |
| 0xB6 | | R/W | REC_B2[15:8] | | | | | | | | — |
| 0xB7 | | R/W | REC_B2[7:0] | | | | | | | | — |
| 0xB8 | RECORD BIQUAD COEFFICIENT A1 | R/W | REC_A1[23:16] | | | | | | | | — |
| 0xB9 | | R/W | REC_A1[15:8] | | | | | | | | — |
| 0xBA | | R/W | REC_A1[7:0] | | | | | | | | — |
| 0xBB | RECORD BIQUAD COEFFICIENT A2 | R/W | REC_A2[23:16] | | | | | | | | — |
| 0xBC | | R/W | REC_A2[15:8] | | | | | | | | — |
| 0xBD | | R/W | REC_A2[7:0] | | | | | | | | — |
| REVISION ID REGISTER | | | | | | | | | | | |
| 0xFF | REVISION ID | R | REVID[7:0] | | | | | | | | 0x43 |

## 软件复位

器件提供可由软件控制的复位(表2)，将大多数寄存器恢复为默认(POR)状态(但不复位录音双二阶均衡器和回放参数均衡器系数)。软件复位寄存器为按钮触发、只写寄存器，所以读取该寄存器时总是返回0x00。向SWRESET写逻辑高触发软件寄存器复位，向SWRESET写逻辑低没有影响。

## 表2. 软件复位寄存器

| ADDRESS: 0x00 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | SWRESET | W | 0 | Pushbutton Software Device Reset<br>0: Writing a logic low to SWRESET has no effect.<br>1: Reset all registers to their default POR values. This excludes the record biquad and playback parametric equalizer filter coefficients (Table 24 and Table 45). |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | — | — | — | — |
| 0 | — | — | — | — |

## 电源和性能管理

器件提供全面的电源管理模式，允许禁用任何不使用的电路，将电源电流降至最小。除此之外，电源模式提供软件可配置的选项，可选择最高性能或低功耗工作。

### 器件性能配置

偏置控制寄存器(表3)选择产生共模参考电压的方法。通过电阻分压(从AVDD电源)产生的共模偏置电压有利于通过禁止带隙基准电路降低总体功耗，而这种BIAS基准的缺点是参考点随AVDD电源电压变化(从而降低PSRR)；从带隙基准产生时，BIAS保持恒定，与电源电压无关，但附加电路增大了功耗。

ADC、DAC和耳机回放均具有可选的高性能模式(表4和5)，无论哪种情况，这些模式都需要通过附加功耗来获得功能的增强。ADC也可选择加抖(建议在频谱非常纯时使用)，可配置为两种不同的过采样率。关于ADC工作的更多详细信息，请参见*模/数转换器(ADC)*部分。

## 表3. 偏置控制寄存器

| ADDRESS: 0x42 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | — | — | — | — |
| 0 | BIAS_MODE | R/W | 0 | **Select source for BIAS.**<br>0: BIAS derived from resistive division.<br>1: BIAS created by bandgap reference. |

## 表4. DAC和耳机性能模式控制寄存器

| ADDRESS: 0x43 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | PERFMODE | R/W | 0 | **Performance Mode**<br>Selects DAC to headphone playback performance mode:<br>1: Low power headphone playback mode.<br>0: High performance headphone playback mode. |
| 0 | DACHP | R/W | 0 | **DAC High-Performance Mode**<br>0: DAC settings optimized for lowest power consumption.<br>1: DAC settings optimized for best performance. |

### 器件使能配置

除了器件的全局关断控制外，主要的输入和输出电路可独立使能(或禁止)，以优化功耗。器件全局关断控制的详细信息请参见表6。

## 表5. ADC性能模式控制寄存器

| ADDRESS: 0x44 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | OSR128 | R/W | 1 | **ADC Oversampling Rate**<br>0: $f_{ADCCLK}$ = 64 x $f_S$<br>1: $f_{ADCCLK}$ = 128 x $f_S$ |
| 1 | ADCDITHER | R/W | 1 | **ADC Quantizer Dither**<br>0: Dither disabled.<br>1: Dither enabled. |
| 0 | ADCHP | R/W | 0 | **ADC High-Performance Mode**<br>0: ADC is optimized for low power operation.<br>1: ADC is optimized for best performance. |

## 表6. 器件关断寄存器

| ADDRESS: 0x45 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | $\overline{\text{SHDN}}$ | R/W | 0 | **Device Active-Low Global Shutdown Control**<br>0: Device is in shutdown.<br>1: Device is active.<br>Certain registers should not be written to while the device is active (Table 90). |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | — | — | — | — |
| 0 | — | — | — | — |

表7详细列出了输入信号通路的使能控制(模拟麦克风输入1/2例外，分别通过寄存器0x10和0x11或表9和10使能)，表8详细列出了输出信号通路使能控制。

器件处于全局关断时，禁止全部主要的输入和输出电路，以节省功率。但此时I²C接口保持有效，可配置器件的所有寄存器。特定的寄存器只有在关断状态下进行配置(详细信息见表90)，器件处于有效状态时更改这些寄存器会导致不可预测结果。为了实现最小功耗，仅使能所需要的信号通路。

## 表7. 输入使能寄存器

| ADDRESS: 0x3E | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | MBEN | R/W | 0 | **Microphone Bias Enable**<br>0: Microphone bias disabled.<br>1: Microphone bias enabled. |
| 3 | LINEAEN | R/W | 0 | **Enables Line A Analog Input Block**<br>0: Line A input amplifier disabled.<br>1: Line A input amplifier enabled. |
| 2 | LINEBEN | R/W | 0 | **Enables Line B Analog Input Block**<br>0: Line B input amplifier disabled.<br>1: Line B input amplifier enabled. |
| 1 | ADREN | R/W | 0 | **Right ADC Enable**<br>0: Right ADC disabled.<br>1: Right ADC enabled. |
| 0 | ADLEN | R/W | 0 | **Left ADC Enable**<br>0: Left ADC disabled.<br>1: Left ADC enabled. |

表8. 输出使能寄存器

| ADDRESS: 0x3F | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | HPREN | R/W | 0 | **Right Headphone Output Enable**<br>0: Right headphone output disabled.<br>1: Right headphone output enabled. |
| 6 | HPLEN | R/W | 0 | **Left Headphone Output Enable**<br>0: Left headphone output disabled.<br>1: Left headphone output enabled. |
| 5 | SPREN | R/W | 0 | **Right Class D Speaker Output Enable**<br>0: Right speaker output disabled.<br>1: Right speaker output enabled. |
| 4 | SPLEN | R/W | 0 | **Left Class D Speaker Output Enable**<br>0: Left speaker output disabled.<br>1: Left speaker output enabled. |
| 3 | RCVLEN | R/W | 0 | **Receiver (Earpiece)/Left Line Output Enable**<br>0: Receiver/left line output disabled.<br>1: Receiver/left line output enabled. |
| 2 | RCVREN | R/W | 0 | **Right Line Output Enable**<br>0: Right line output disabled.<br>1: Right line output enabled. |
| 1 | DAREN | R/W | 0 | **Right DAC Digital Input Enable**<br>0: Right DAC input disabled.<br>1: Right DAC input enabled. |
| 0 | DALEN | R/W | 0 | **Left DAC Digital Input Enable**<br>0: Left DAC input disabled.<br>1: Left DAC input enabled. |

## 模拟音频输入配置

器件具有六路(WLP封装)或四路(TQFN封装)灵活的模拟输入，每对输入可配置为模拟麦克风输入、单端或差分线入，或将满幅差分模拟输入直接连接至ADC混音器，以降低功耗。模拟麦克风和线入可连接至立体声ADC混音器进行录音或直接连接至任意模拟输出混音器进行回放。

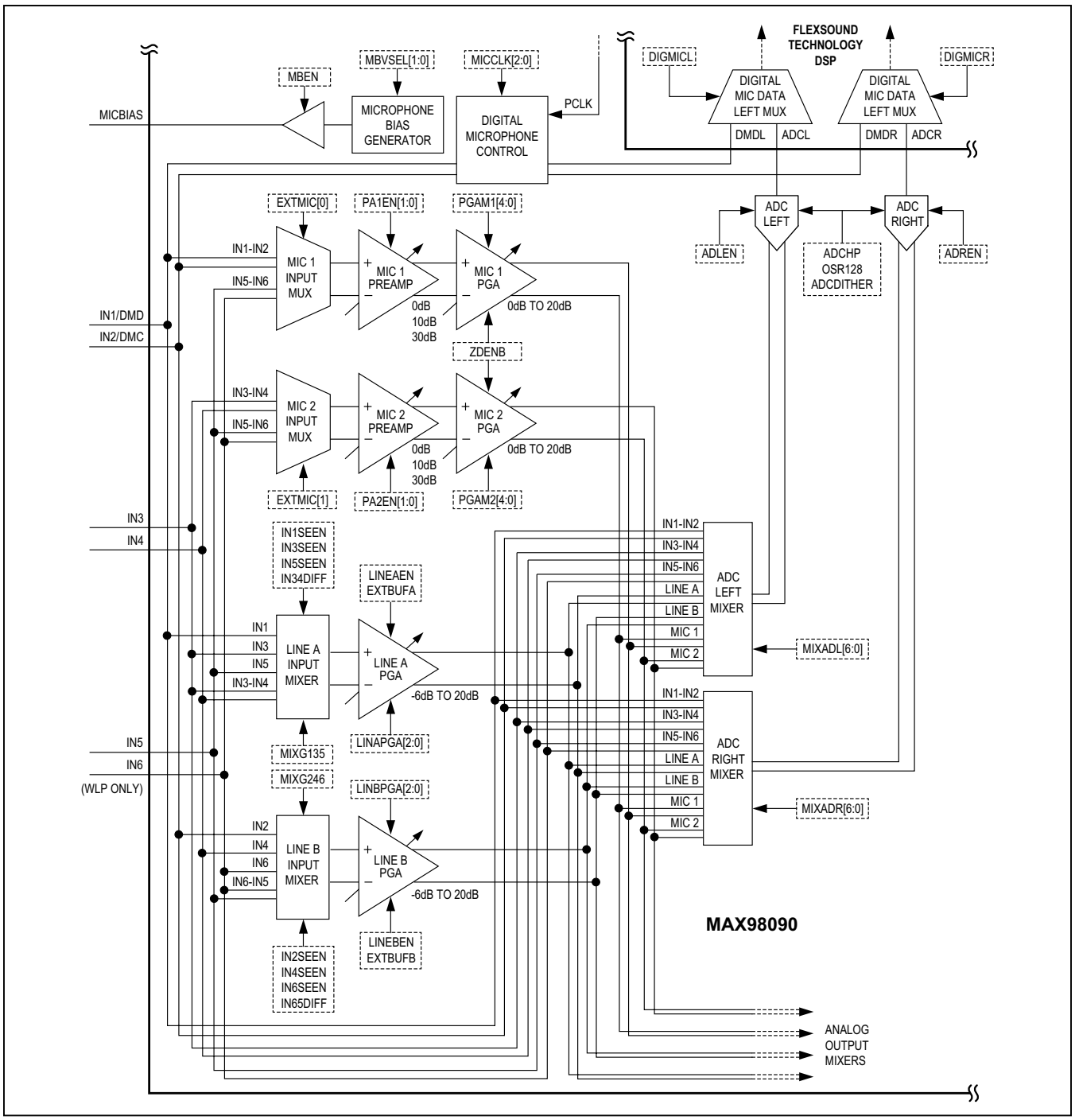



*图5. 模拟音频输入功能框图*

### 模拟麦克风输入

器件包括三路差分麦克风输入(WLP封装为三路，TQFN封装为两路)，以及一路可编程低噪声麦克风偏置，用于为各种外部麦克风供电(图6)。默认设置下，输入IN1和IN2为麦克风放大器1提供差分(IN1/IN2)输入，IN3和IN4为麦克风放大器2提供差分(IN3/IN4)输入。对于WLP封装，附加模拟输入对(IN5和IN6)可配置为差分输入(IN5 - IN6)，连接至麦克风放大器1或2(表24)。

典型应用中，一路麦克风输入用于手持麦克风，另一路作为麦克风附件(IN1/IN2和IN3/IN4)。系统需要利用背景噪声时，IN5/IN6(仅限WLP封装)可以重新配置成另一路麦克风输入。

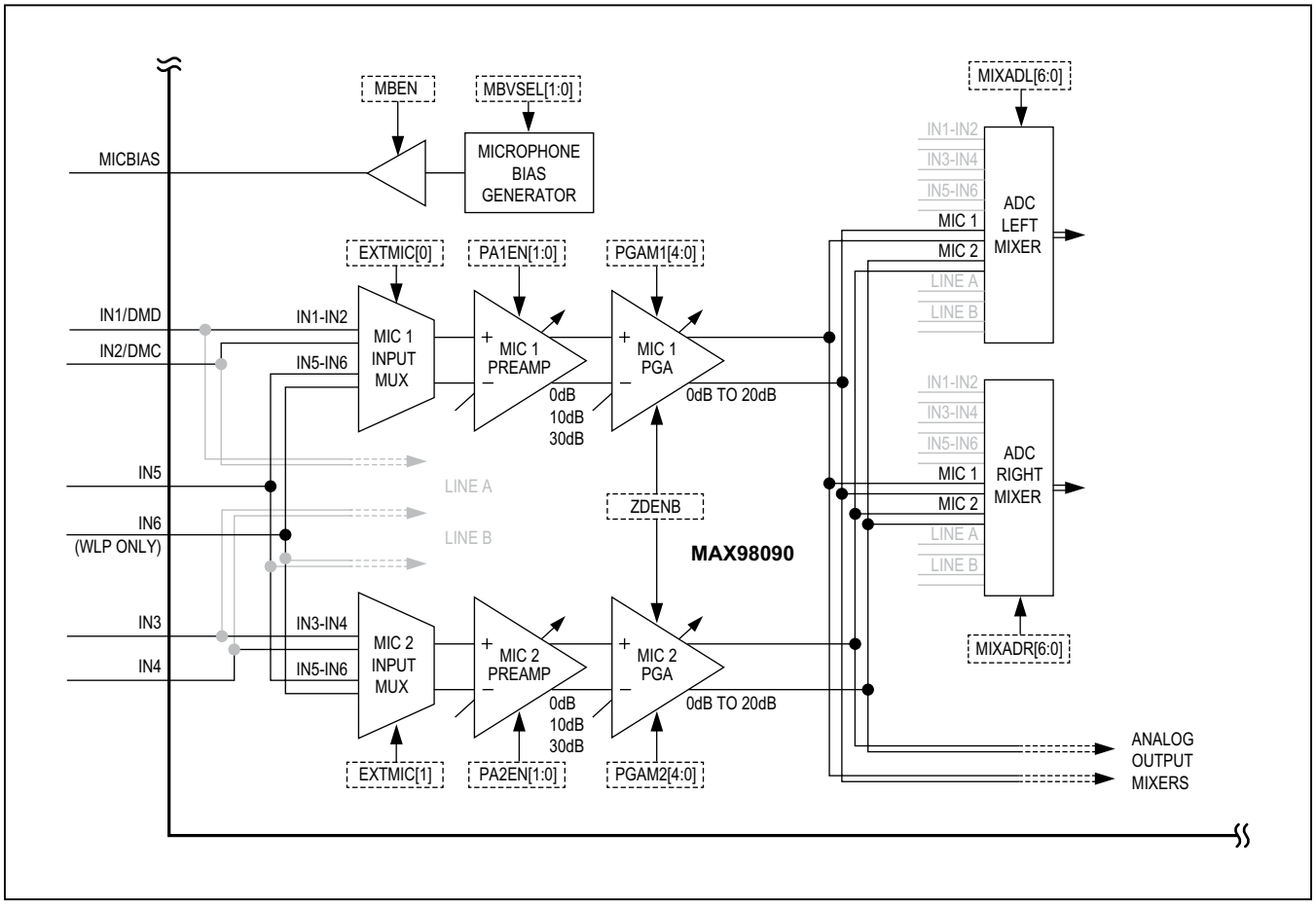



*图6. 模拟麦克风输入功能框图*

### 模拟麦克风前置放大器和PGA

模拟麦克风输入具有两级可编程增益放大器，然后连接至ADC混音器(录音)、模拟输出(回放)，或者同时连接到两者。第一级为粗调前置放大器增益级，包括模拟麦克风使能，可选择0dB、20dB或30dB增益设置。第二级为精调可编程增益放大器(PGA)增益级，增益从0dB至20dB可调，步长为1dB(表9和10)。两级一起为模拟麦克风输入提供高达50dB的信号增益。为获得最高的信噪比，尽可能充分利用第一级的粗调增益设置。PGA提供过零检测功能，从而抑制增益改变时的噪声。

## 表9. 麦克风1使能和电平配置寄存器

| ADDRESS: 0x10 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | PA1EN[1:0] | R/W | 0 | **Microphone 1 Input Amplifier Enable and Coarse Gain Setting**<br>00: Disabled 10: 20dB<br>01: 0dB 11: 30dB |
| 5 | | | 0 | |
| 4 | PGAM1[4:0] | R/W | 1 | **Microphone 1 Programmable Gain Amplifier Fine Adjust Configuration** |
| 3 | | | 0 | 0x1F: 0dB 0x0E: 6dB 0x06: 14dB<br>⋮ 0x0D: 7dB 0x05: 15dB<br>0x14: 0dB 0x0C: 8dB 0x04: 16dB<br>0x13: 1dB 0x0B: 9dB 0x03: 17dB<br>0x12: 2dB 0x0A: 10dB 0x02: 18dB<br>0x11: 3dB 0x09: 11dB 0x01: 19dB<br>0x10: 4dB 0x08: 12dB 0x00: 20dB<br>0x0F: 5dB 0x07: 13dB |
| 2 | | | 1 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

## 表10. 麦克风2使能和电平配置寄存器

| ADDRESS: 0x11 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | PA2EN[1:0] | R/W | 0 | **Microphone 2 Input Amplifier Enable and Coarse Gain Setting**<br>00: Disabled 10: 20dB<br>01: 0dB 11: 30dB |
| 5 | | | 0 | |
| 4 | PGAM2[4:0] | R/W | 1 | **Microphone 2 Programmable Gain Amplifier Fine Adjust Configuration** |
| 3 | | | 0 | 0x1F: 0dB 0x0E: 6dB 0x06: 14dB<br>⋮ 0x0D: 7dB 0x05: 15dB<br>0x14: 0dB 0x0C: 8dB 0x04: 16dB<br>0x13: 1dB 0x0B: 9dB 0x03: 17dB<br>0x12: 2dB 0x0A: 10dB 0x02: 18dB<br>0x11: 3dB 0x09: 11dB 0x01: 19dB<br>0x10: 4dB 0x08: 12dB 0x00: 20dB<br>0x0F: 5dB 0x07: 13dB |
| 2 | | | 1 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

### 模拟麦克风偏置电压

器件具有一路稳压、低噪声麦克风偏置输出(MICBIAS)，为各种外部麦克风设备供电。为使能麦克风偏置输出，将输入使能寄存器的MBEN置位(表7)。器件上电且禁止麦克风偏置时(MBEN为低电平或器件处于关断状态)，MICBIAS置于高阻态。通过设置麦克风偏置电平配置寄存器，麦克风偏置电压可由软件设置为4种电压之一(2.2V、2.4V、2.55V或2.8V)(表11)。

## 数字麦克风输入

也可将一对麦克风输入(IN1/IN2)配置为连接多达两个数字麦克风(图7)。使能时，录音通路DSP自动切换，以接收相应数字麦克风数据声道(图13)；必须使能两个声道(左声道和右声道)，以便使用数字麦克风接口。使能两个声道时，数字麦克风接口提供IN2/DMC的数字麦克风时钟，并接收IN1/DMD的PDM数据。单个数字麦克风输入不能与单个模拟麦克风输入配对工作。在时钟下降沿接收左声道数据，在时钟上升沿接收右声道数据(时序要求请参见图4)。

使用数字麦克风输入(AHPF，表21)时，为避免任何潜在的削波和失真，始终使能录音通路的隔直流滤波器，以消除任何内部直流失调。录音通路双二阶滤波器及数字增益和电平控制电路也可以作用到数字麦克风输入。

### 数字麦克风时钟配置

使用MICCLK[2:0]，可将数字麦克风时钟频率($f_{DMC}$)配置为6种设置之一(表13)。数字麦克风时钟由PCLK分频器获得，可用设置范围为$f_{PCLK}/2$至$f_{PCLK}/8$。较宽的数字麦克风时钟频率范围可支持当前和下一代数字麦克风。表12中列出了常用主控时钟(以及产生的PCLK)频率下得到的麦克风时钟频率。

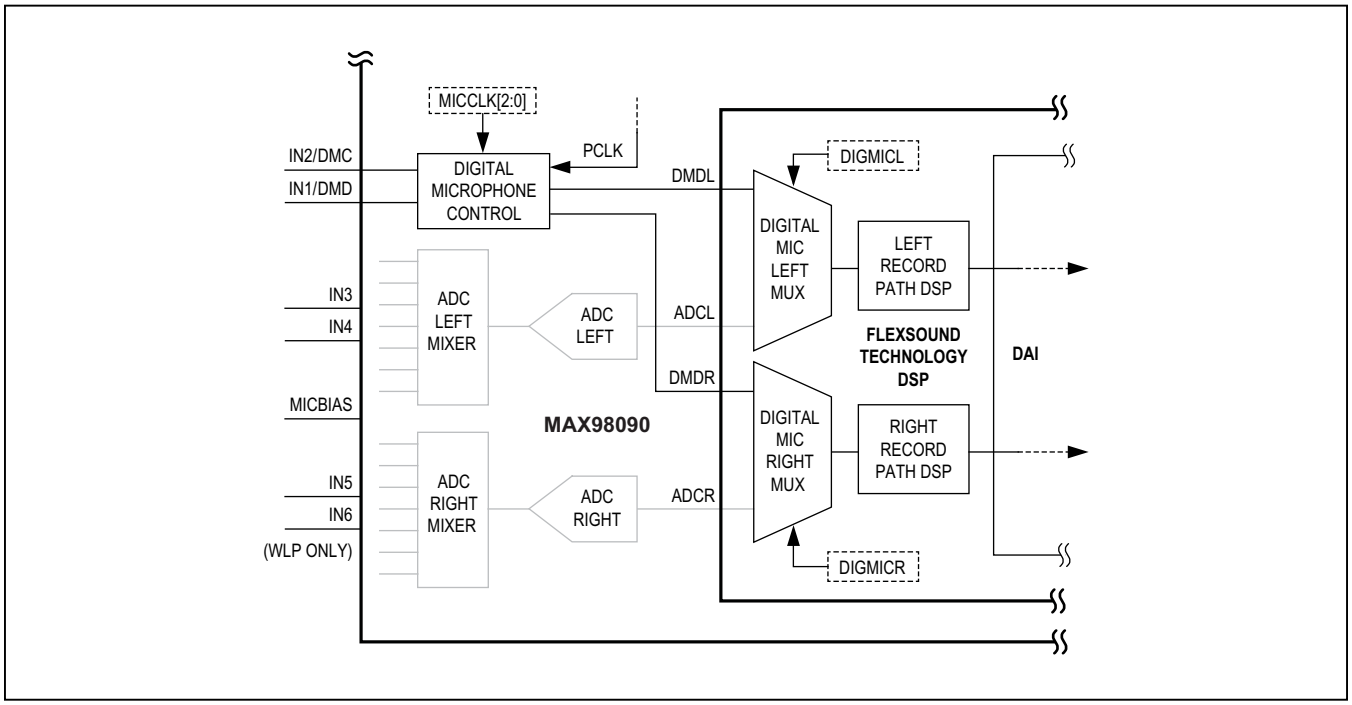



*图7. 数字麦克风输入功能框图*

## 表11. 麦克风偏置电平配置寄存器

| ADDRESS: 0x12 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | MBVSEL[1:0] | R/W | 0 | **Microphone Bias Level Configuration**<br>00: 2.2V 10: 2.55V<br>01: 2.4V 11: 2.8V |
| 0 | | | 0 | |

## 表12. 常用主控时钟设置下的数字麦克风时钟

| Master Clock Frequency ($f_{MCLK}$) | | 10MHz | 11.2896MHz | 12MHz | 12.288MHz | 13/26MHz | 19.2MHz |
|---|---|---|---|---|---|---|---|
| Approximate Digital Microphone Clock Frequency ($f_{DMC}$) | $f_{PCLK}/2$ | 5.0MHz | 5.645MHz | 6.0MHz | 6.144MHz | 6.5MHz | — |
| | $f_{PCLK}/3$ | 3.333MHz | 3.763MHz | 4.0MHz | 4.096MHz | 4.333MHz | 6.4MHz |
| | $f_{PCLK}/4$ | 2.5MHz | 2.822MHz | 3.0MHz | 3.072MHz | 3.25MHz | 4.8MHz |
| | $f_{PCLK}/5$ | 2.0MHz | 2.258MHz | 2.4MHz | 2.458MHz | 2.6MHz | 3.84MHz |
| | $f_{PCLK}/6$ | 1.667MHz | 1.882MHz | 2.0MHz | 2.048MHz | 2.167MHz | 3.2MHz |
| | $f_{PCLK}/8$ | 1.25MHz | 1.411MHz | 1.5MHz | 1.536MHz | 1.625MHz | 2.4MHz |

## 表13. 数字麦克风使能

| ADDRESS: 0x13 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | MICCLK[2:0] | R/W | 0 | **Digital Microphone Clock Rate Configuration**<br>000: $f_{DMC} = f_{PCLK}/2$ 100: $f_{DMC} = f_{PCLK}/6$<br>001: $f_{DMC} = f_{PCLK}/3$ 101: $f_{DMC} = f_{PCLK}/8$<br>010: $f_{DMC} = f_{PCLK}/4$ 110: Reserved<br>011: $f_{DMC} = f_{PCLK}/5$ 111: Reserved |
| 5 | | | 0 | |
| 4 | | | 0 | |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | DIGMICR | R/W | 0 | **Digital Microphone Clock and Right Channel Enable**<br>0: Right record channel uses on-chip ADC.<br>1: Right record channel uses digital microphone input.<br>Digital microphone clock (DMC) is enabled once both data channels are enabled. |
| 0 | DIGMICL | R/W | 0 | **Digital Microphone Clock and Left Channel Enable**<br>0: Left record channel uses on-chip ADC.<br>1: Left record channel uses digital microphone input.<br>Digital microphone clock (DMC) is enabled once both data channels are enabled. |

### 数字麦克风频率补偿

数字麦克风输入可配置为产生宽范围数字麦克风时钟频率。为优化整个频率范围的性能，器件提供可配置的频率范围和补偿设置。一旦确定主控时钟(以及预分频时钟)频率并选择数字麦克风时钟驱动器，应将数字麦克风频率范围配置位设置在正确状态(DMIC_FREQ，表14)。如果使用快速配置模式并选择了系统时钟位(表36)，配置数字麦克风时钟分频器后，器件将自动计算和选择正确范围。

数字麦克风输入也提供可配置的频率补偿滤波器，具有九种频率响应设置(图8)。每种数字麦克风时钟和采样率组合产生不同的基线频率响应。表15至表20列出了适合于大多数常用时钟和采用率组合的推荐补偿滤波器设置。对于非标准组合，使用最接近的推荐设置或选择最接近实测响应的曲线。快速配置模式下，选定系统时钟和采样率位(表36和表37)后，一旦配置了数字麦克风时钟分频器，器件自动选择推荐的响应曲线。数字麦克风输入不支持超过50kHz(此时DHF = 1，表27)的采样率。

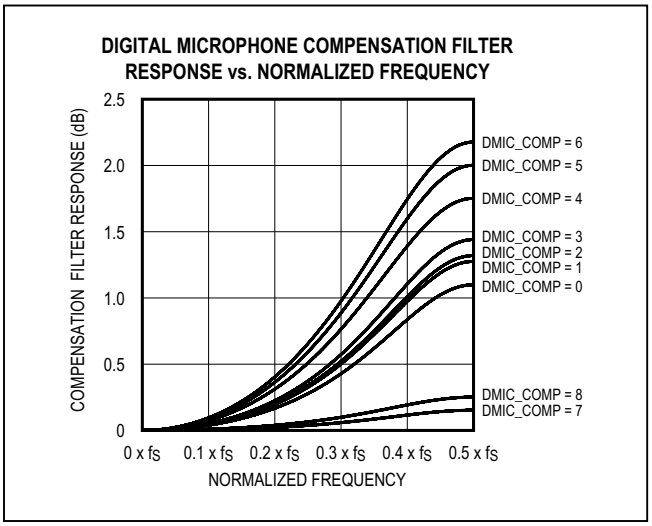



*图 8. 数字麦克风补偿滤波器频率响应*

## 表14. 数字麦克风配置

| ADDRESS: 0x14 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | DMIC_COMP[3:0] | R/W | 0 | **Digital Microphone Compensation Filter Configuration**<br>0000–1000: Figure 8 details the available compensation filter configurations.<br>1001–1111: Configures the compensation filter to a pass through response.<br>The compensation filter response scales with the sample rate up to the Nyquist bandwidth limit ($f_S$/2). Automatically decoded in quick configuration mode. |
| 6 | | | 0 | |
| 5 | | | 0 | |
| 4 | | | 0 | |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | DMIC_FREQ[1:0] | R/W | 0 | **Digital Microphone Frequency Range Configuration**<br>00: $f_{DMC}$ < 3.5MHz<br>01: 3.5MHz ≤ $f_{DMC}$ < 4.5MHz<br>10: 4.5MHz ≤ $f_{DMC}$<br>11: Reserved<br>If any of the system clock quick configuration bits in register 0x04 are set, then the frequency range configuration is automatically decoded. |
| 0 | | R/W | 0 | |

表15. 推荐补偿滤波器设置，$f_{MCLK}$ = 11.2896MHz

| $f_{PCLK}$ = 11.2896MHz | | | | RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz) | | | | |
|---|---|---|---|---|---|---|---|---|
| MICCLK | DIVIDER | $f_{DMC}$ (MHz) | DMIC_FREQ | 8 | 16 | 32 | 44.1 | 48 |
| 0 | $f_{PCLK}$/2 | 5.6448 | 2 | 7 | 8 | 3 | 3 | 3 |
| 1 | $f_{PCLK}$/3 | 3.7632 | 1 | 7 | 8 | 2 | 2 | 2 |
| 2 | $f_{PCLK}$/4 | 2.8224 | 0 | 7 | 8 | 3 | 3 | 3 |
| 3 | $f_{PCLK}$/5 | 2.25792 | 0 | 7 | 8 | 6 | 6 | 6 |
| 4 | $f_{PCLK}$/6 | 1.8816 | 0 | 7 | 8 | 3 | 3 | 3 |
| 5 | $f_{PCLK}$/8 | 1.4112 | 0 | 7 | 8 | 3 | 3 | 3 |

表16. 推荐补偿滤波器设置，$f_{MCLK}$ = 12MHz

| $f_{PCLK}$ = 12MHz | | | | RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz) | | | | |
|---|---|---|---|---|---|---|---|---|
| MICCLK | DIVIDER | $f_{DMC}$ (MHz) | DMIC_FREQ | 8 | 16 | 32 | 44.1 | 48 |
| 0 | $f_{PCLK}$/2 | 6 | 2 | 7 | 8 | 3 | 3 | 3 |
| 1 | $f_{PCLK}$/3 | 4 | 1 | 7 | 8 | 2 | 2 | 2 |
| 2 | $f_{PCLK}$/4 | 3 | 0 | 7 | 8 | 3 | 3 | 3 |
| 3 | $f_{PCLK}$/5 | 2.4 | 0 | 7 | 8 | 5 | 5 | 6 |
| 4 | $f_{PCLK}$/6 | 2 | 0 | 7 | 8 | 3 | 3 | 3 |
| 5 | $f_{PCLK}$/8 | 1.5 | 0 | 7 | 8 | 3 | 3 | 3 |

表17. 推荐补偿滤波器设置，$f_{MCLK}$ = 12.288MHz

| $f_{PCLK}$ = 12.288(MHz) | | | | RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz) | | | | |
|---|---|---|---|---|---|---|---|---|
| MICCLK | DIVIDER | $f_{DMC}$ (MHz) | DMIC_FREQ | 8 | 16 | 32 | 44.1 | 48 |
| 0 | $f_{PCLK}$/2 | 6.144 | 2 | 7 | 8 | 3 | 3 | 3 |
| 1 | $f_{PCLK}$/3 | 4.096 | 1 | 7 | 8 | 2 | 2 | 2 |
| 2 | $f_{PCLK}$/4 | 3.072 | 0 | 7 | 8 | 3 | 3 | 3 |
| 3 | $f_{PCLK}$/5 | 2.4576 | 0 | 7 | 8 | 6 | 6 | 6 |
| 4 | $f_{PCLK}$/6 | 2.048 | 0 | 7 | 8 | 3 | 3 | 3 |
| 5 | $f_{PCLK}$/8 | 1.536 | 0 | 7 | 8 | 3 | 3 | 3 |

表18. 推荐补偿滤波器设置，$f_{MCLK}$ = 13MHz/26MHz

| $f_{PCLK}$ = 13MHz | | | | RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz) | | | | |
|---|---|---|---|---|---|---|---|---|
| MICCLK | DIVIDER | $f_{DMC}$ (MHz) | DMIC_FREQ | 8 | 16 | 32 | 44.1 | 48 |
| 0 | $f_{PCLK}$/2 | 6.5 | 2 | 7 | 8 | 1 | 1 | 1 |
| 1 | $f_{PCLK}$/3 | 4.333 | 1 | 7 | 8 | 0 | 0 | 1 |
| 2 | $f_{PCLK}$/4 | 3.25 | 0 | 7 | 8 | 1 | 1 | 1 |
| 3 | $f_{PCLK}$/5 | 2.6 | 0 | 7 | 8 | 4 | 4 | 5 |
| 4 | $f_{PCLK}$/6 | 2.167 | 0 | 7 | 8 | 1 | 1 | 1 |
| 5 | $f_{PCLK}$/8 | 1.625 | 0 | 7 | 8 | 1 | 1 | 1 |

表19. 推荐补偿滤波器设置，$f_{MCLK}$ = 19.2MHz

| $f_{PCLK}$ = 19.2MHz | | | | RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz) | | | | |
|---|---|---|---|---|---|---|---|---|
| MICCLK | DIVIDER | $f_{DMC}$ (MHz) | DMIC_FREQ | 8 | 16 | 32 | 44.1 | 48 |
| 0 | $f_{PCLK}$/2 | — | — | — | — | — | — | — |
| 1 | $f_{PCLK}$/3 | 6.4 | 2 | 7 | 8 | 1 | 1 | 1 |
| 2 | $f_{PCLK}$/4 | 4.8 | 2 | 7 | 8 | 5 | 5 | 6 |
| 3 | $f_{PCLK}$/5 | 3.84 | 1 | 7 | 8 | 2 | 2 | 3 |
| 4 | $f_{PCLK}$/6 | 3.2 | 0 | 7 | 8 | 1 | 1 | 2 |
| 5 | $f_{PCLK}$/8 | 2.4 | 0 | 7 | 8 | 5 | 5 | 6 |

表20. 推荐补偿滤波器设置，$f_{MCLK}$ = 256 x $f_S$

| $f_{PCLK}$ = 256 x $f_S$ | | | | RECOMMENDED DMIC_COMP SETTING BY SAMPLE RATE (kHz) | | | | |
|---|---|---|---|---|---|---|---|---|
| MICCLK | DIVIDER | $f_{DMC}$ (MHz) | DMIC_FREQ | 8 | 16 | 32 | 44.1 | 48 |
| 0 | $f_{PCLK}$/2 | — | — | 7 | 8 | 3 | 3 | 3 |
| 1 | $f_{PCLK}$/3 | — | — | 7 | 8 | 2 | 2 | 2 |
| 2 | $f_{PCLK}$/4 | — | — | 7 | 8 | 3 | 3 | 3 |
| 3 | $f_{PCLK}$/5 | — | — | 7 | 8 | 6 | 6 | 6 |
| 4 | $f_{PCLK}$/6 | — | — | 7 | 8 | 3 | 3 | 3 |
| 5 | $f_{PCLK}$/8 | — | — | 7 | 8 | 3 | 3 | 3 |

### 模拟线入

器件包括多种线入电平选项，以及两个模拟线入可编程增益放大器(PGA，图9)。线入架构支持多种配置，包括立体声单端输入、立体声差分输入和立体声混音单端输入(每个线入混音器支持其中任意两路)。

### 模拟线入混音器

模拟线入混音器允许选择单端或差分输入连接至每路线入声道(表21)。线入A混音器可接收来自IN1、IN3和IN5的单端输入，或来自IN3和IN4 (IN3 – IN4)的差分输入；线入B混音器可接收来自IN2、IN4和IN6的单端输入，或来自IN5和IN6 (IN6 – IN5)的差分输入。全部模拟输入通路在内部

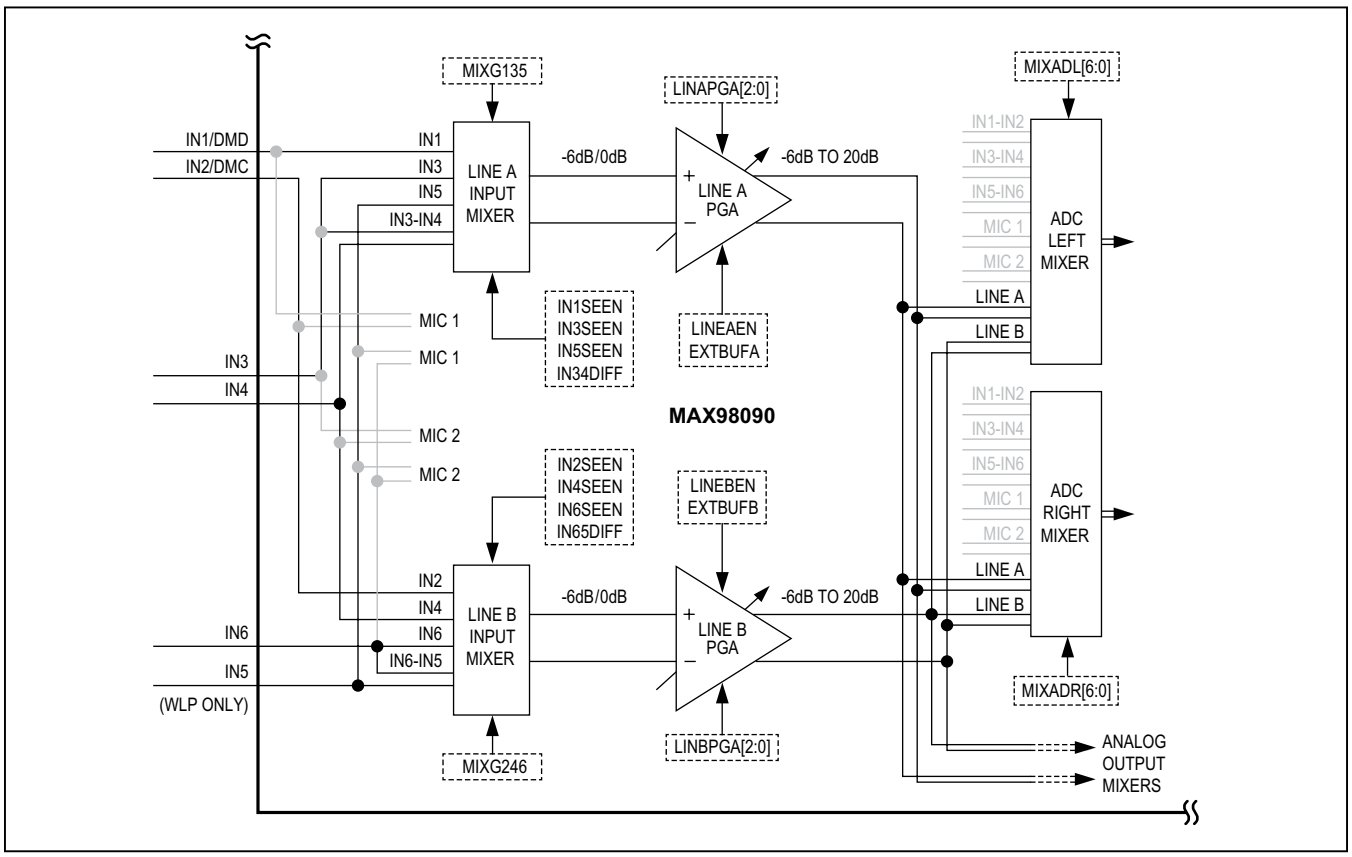



*图 9. 模拟线入功能框图*

## 表21. 线入混音器配置寄存器

| ADDRESS: 0x0D | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | IN34DIFF | R/W | 0 | Selects IN3, IN4 differentially as an input to the line A mixer. |
| 6 | IN65DIFF | R/W | 0 | Selects IN6, IN5 differentially as an input to the line B mixer (WLP only). |
| 5 | IN1SEEN | R/W | 0 | Selects IN1 single ended as an input to the line A mixer. |
| 4 | IN2SEEN | R/W | 0 | Selects IN2 single ended as an input to the line B mixer. |
| 3 | IN3SEEN | R/W | 0 | Selects IN3 single ended as an input to the line A mixer. |
| 2 | IN4SEEN | R/W | 0 | Selects IN4 single ended as an input to the line B mixer. |
| 1 | IN5SEEN | R/W | 0 | Selects IN5 single ended as an input to the line A mixer (WLP only). |
| 0 | IN6SEEN | R/W | 0 | Selects IN6 single ended as an input to the line B mixer (WLP only). |

为差分，单端输入具有+6dB内置基线增益(从单端转换为差分)，差分输入的内置增益为0dB。

线入混音器也可设置为接收和混音两路单端输入。为处理满幅信号，对两路单端输入混音时，可选择-6dB衰减(MIXG135和MIXG246，表23)。只选定一路输入源时，线入混音器设置没有影响；如果使能任一混音器的差分输入，将忽略选定的单端输入，混音器只接收差分输入。

### 模拟线入PGA

为支持宽范围输入信号电平，每路模拟线入包括粗调可编程增益放大器(PGA)，可提供从6dB至20dB信号增益的衰减；然后将线入连接至ADC混音器(录音)或模拟输出(回放)。

如果线入信号超过满幅电平，需要附加衰减，外部增益模式提供微调内部反馈电阻(20kΩ)，以自定义增益电平。线入外部增益模式不用于提供正增益，而是用于优化性能；任何高于-6dB的增益应使用提供的内部PGA进行设置。

差分输入时，外部线入增益由两个高精度(1%或更优)、匹配很好的串联输入电阻进行设置(图10)。使用下式计算正确的差分串联输入电阻：

$$A_{V\_EXTLINE} = 20 \times \log (20k\Omega / R_{S\_EXT})$$

对于单端输入，使用一个高精度(1%或更优)串联输入电阻设置外部线入增益(图10)。然而，由于内部单端至差分转换，该配置形成不平衡差分放大器配置(配置的外部增益与内部+6dB固定增益配对)。表22给出了常见衰减设置所采用的串联电阻值。

## 表22. 外部增益模式串联电阻值

| LINE INPUT EXTERNAL GAIN (dB) | $R_{S\_EXT}$ | |
|---|---|---|
| | DIFFERENTIAL (kΩ) | SINGLE-ENDED (kΩ) |
| $A_{V\_EXTLINE}$ = -9.5 | 60 | 84.5 |
| $A_{V\_EXTLINE}$ = -12.0 | 80 | 115 |
| $A_{V\_EXTLINE}$ = -15.0 | 112 | 165 |
| $A_{V\_EXTLINE}$ = -18.0 | 160 | 237 |

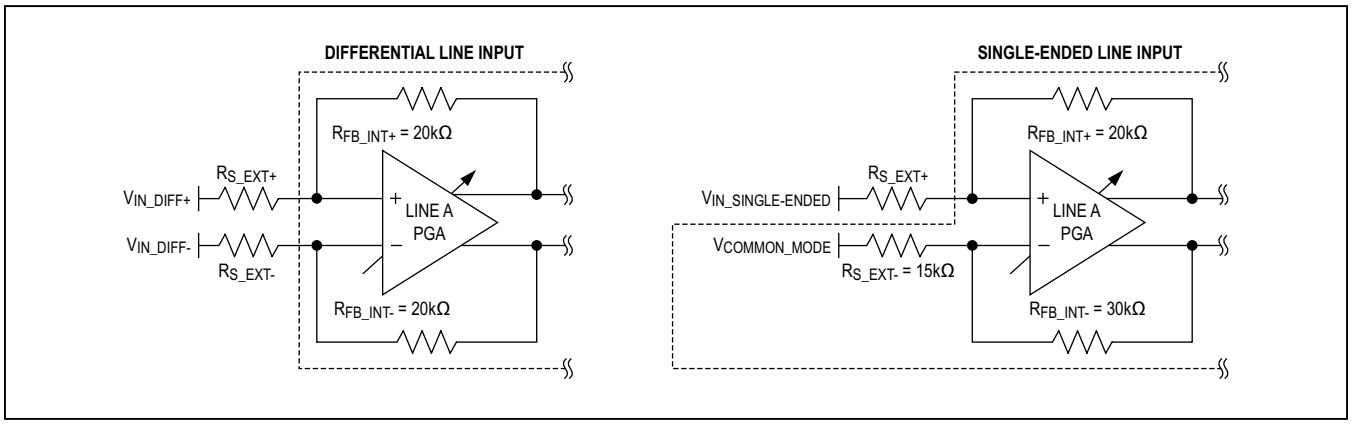



*图10. 模拟线入外部增益配置*

## 表23. 线入电平配置寄存器

| ADDRESS: 0x0E | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | MIXG135 | R/W | 0 | **Enable for a -6dB Reduction for Two Single-Ended Line A Mixer Inputs**<br>0: Normal line A mixer operation.<br>1: Gain is reduced by -6dB when two single-ended inputs are selected. |
| 6 | MIXG246 | R/W | 0 | **Enable for a -6dB Reduction for Two Single-Ended Line B Mixer Inputs**<br>0: Normal line B mixer operation.<br>1: Gain is reduced by -6dB when two single-ended inputs are selected. |
| 5 | LINAPGA[2:0] | R/W | 0 | **Line Input A Programmable Internal Preamp Gain Configuration**<br>000: 20dB 010: 3dB 100: -3dB<br>001: 14dB 011: 0dB 101, 110, 111: -6dB |
| 4 | | | 1 | |
| 3 | | | 1 | |
| 2 | LINBPGA[2:0] | R/W | 0 | **Line Input B Programmable Internal Preamp Gain Configuration**<br>000: 20dB 010: 3dB 100: -3dB<br>001: 14dB 011: 0dB 101, 110, 111: -6dB |
| 1 | | | 1 | |
| 0 | | | 1 | |

## 表24. 模拟输入和源配置寄存器

| ADDRESS: 0x0F | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | EXTBUFA | R/W | 0 | Selects external resistor gain mode for line input A. |
| 6 | EXTBUFB | R/W | 0 | Selects external resistor gain mode for line input B. |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | EXTMIC[1:0] | R/W | 0 | **External Analog Microphone (IN5/IN6) MUX Configuration (WLP Only)**<br>00: External microphone disabled:<br>IN1/IN2 selected for MIC 1<br>IN3/IN4 selected for MIC 2<br>10: External microphone to MIC 2:<br>IN1/IN2 selected for MIC 1<br>IN5/IN6 selected for MIC 2<br>01: External microphone to MIC 1:<br>IN5/IN6 selected for MIC 1<br>IN3/IN4 selected for MIC 2<br>11: Reserved. |
| 0 | | | 0 | |

### 模拟输入PGA至模拟输出混音器

模拟线路输入PGA和模拟麦克风PGA输出可直接连接至任意模拟输出混音器，这种配置允许模拟输入作为线路输入或麦克风电平输入放大器工作，能够驱动耳机、扬声器、接收器或线路输出负载。模拟输入也可与DAC输出混音，连接至任意可用的模拟输出混音器。对应模拟输入和输出部分的图示详细说明了信号连接。

### 模拟满幅信号直接连接至ADC混音器输入

模拟输入也可配置为直接接收，将差分模拟信号连接至ADC混音器(录音通路，图11)。通过禁止和旁路模拟麦克风和线入增益级，该模式降低了满幅(最高1$V_{RMS}$)模拟输入信号时的工作损耗。与模拟麦克风和线入配置不同，该模式不允许输入信号直接连接至模拟输出混音器(回放通路，图32)。

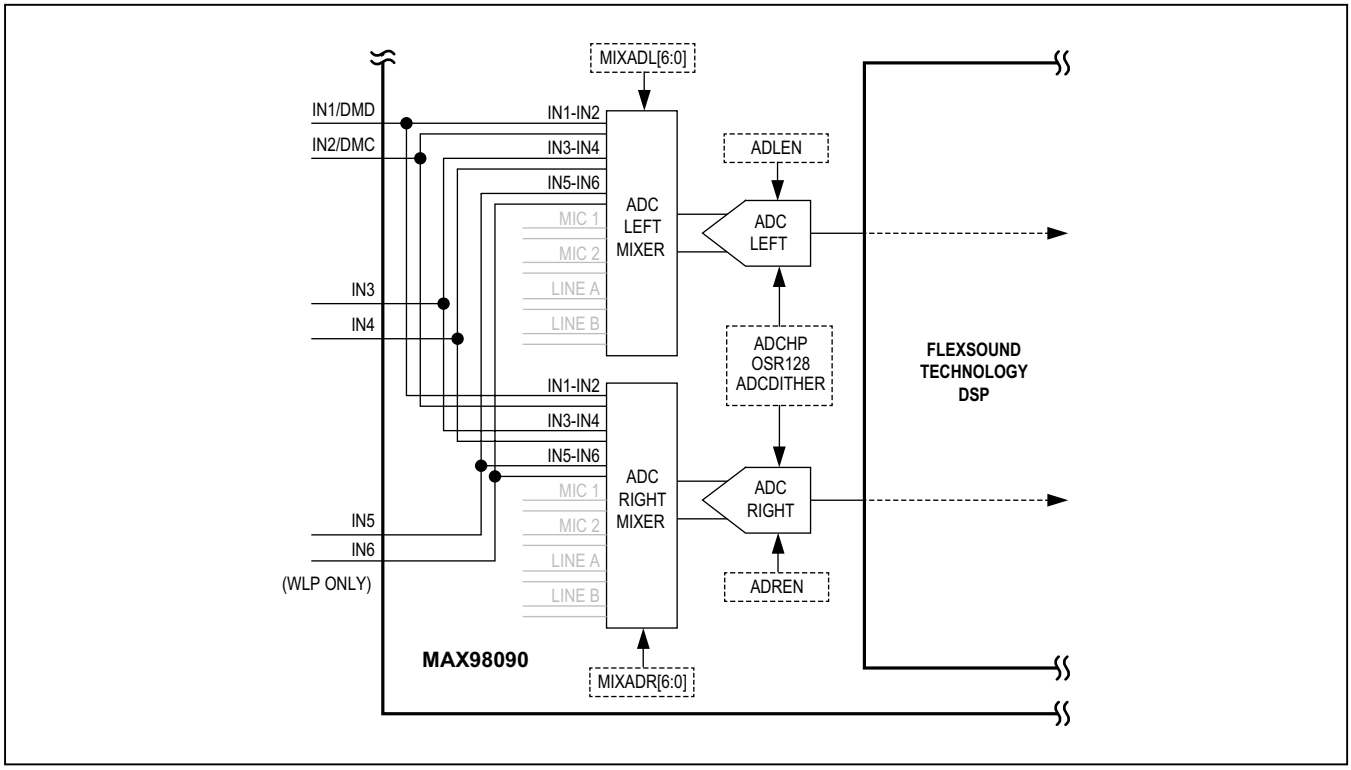



*图11. 模拟输入直接连接至ADC混音器输入的功能框图*

## 录音通路

器件的录音通路由多个分先后顺序的电路组成。第一个电路为立体声ADC，带有可配置混音器，可接收来自于麦克风PGA、线入PGA的信号，或者直接来自于任意模拟输入对的差分信号。数字录音通路在内部具有两个声道(左和右声道)，接收来自于相应数字麦克风或ADC输出通道的数字信号。然后两路通道通过多级DSP，再连接至数字音频接口(DAI，图12)。

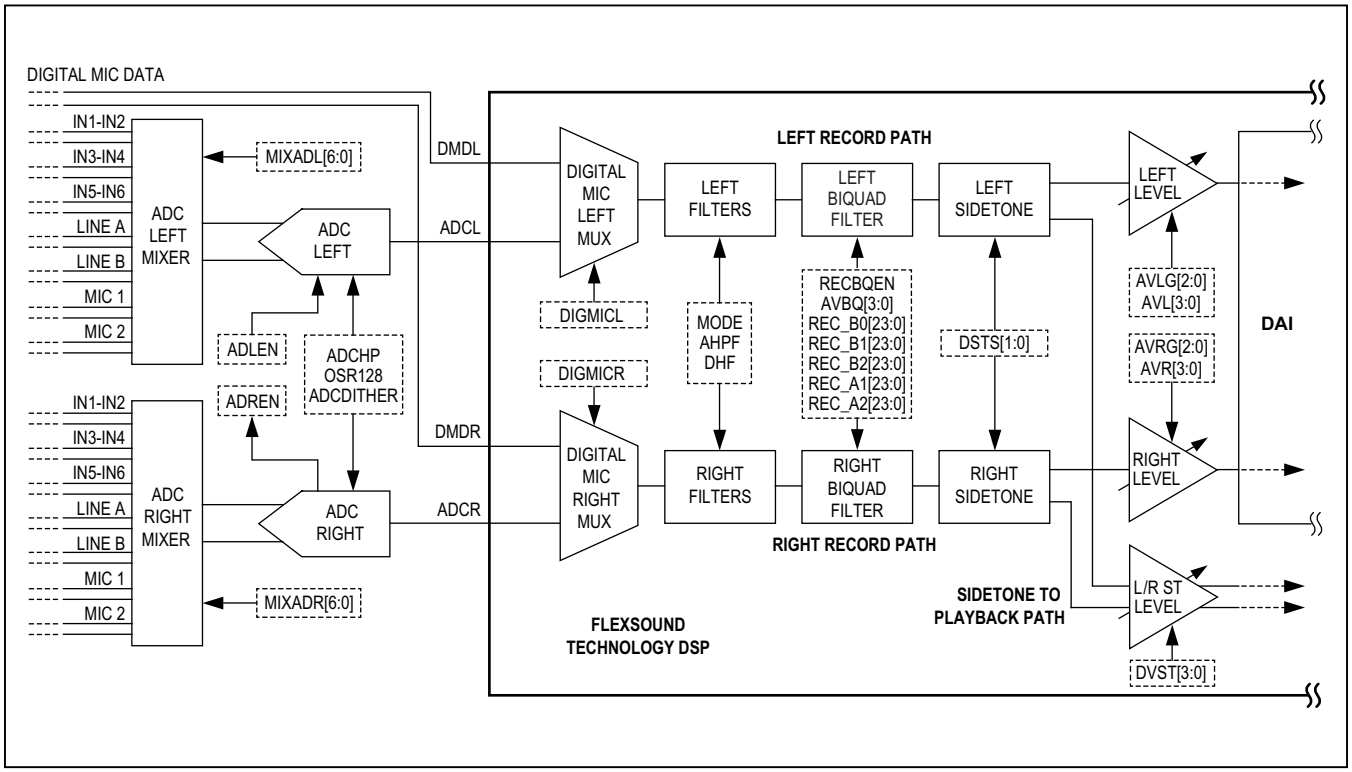



*图12. 录音通路框图*

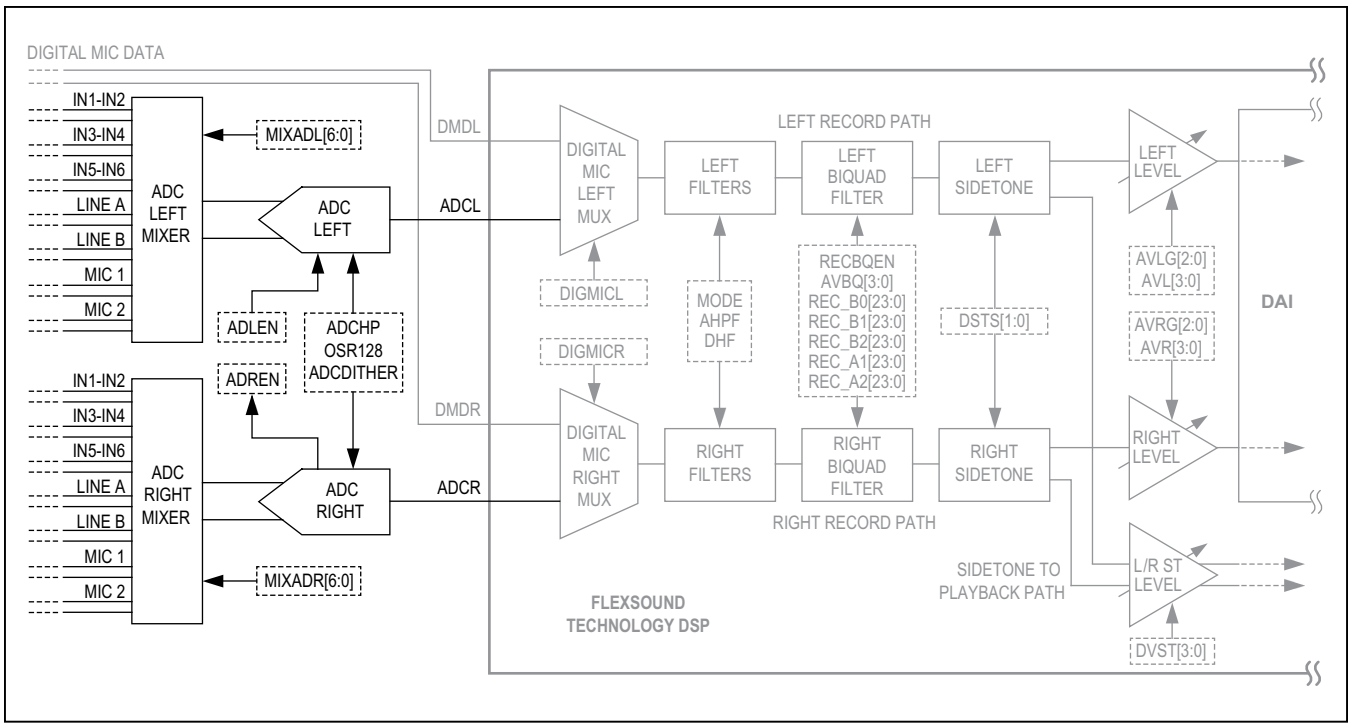



*图13. 录音通路ADC部分*

## 模/数转换器(ADC)

立体声ADC架构包括两条独立音频通路，提供灵活、完全可配置的输入混频器、两种基于性能和功率的配置、过采样率选择以及输入加抖选项(图13)。两路ADC通道可独立使能，允许器件支持立体声和左声道或右声道单声道配置(表7)。

### ADC功能配置

ADC可配置为两种工作模式之一：一种工作模式优化用于提高动态性能，另一种模式优化用于降低功耗(表5)。ADC录音通路也可增加输入加抖，该功能几乎不增加功耗，但在音频频带的高端略微增大了噪底RMS。

ADC支持64倍和128倍采样频率($f_S$)的过采样率(OSR)，128 x $f_S$的OSR提高ADC性能，但比OSR为64 x $f_S$时的功耗略大。

然而，DSP定时对使用的OSR施加限制。对于使用标准($f_S$ = 8kHz)和宽带($f_S$ = 16kHz)采样率的语音应用，DSP通常配置为使用语音滤波器(IIR)。如果使能语音滤波器，OSR自动配置为128 x $f_S$，不能手动重新设置，以满足定时要求。

大多数标准音乐/全音频范围应用中(此时$f_S$ = 32kHz、44.1kHz、48kHz等)，使用音乐滤波器(FIR)。如果使能音乐滤波器，不能手动配置OSR，但预分频主控时钟(PCLK)必须至少为ADC采样时钟频率的两倍；为确保满足这一条件，如果$f_{PCLK}$ < 256 x $f_S$，必须将OSR设为64 x $f_S$。此外，如果采样率超过50kHz (DHF = 1，例如fS = 96kHz)，那么OSR必须配置为64 x $f_S$，与比值无关。在其它任何音乐滤波器配置中，可选择OSR = 128，以优化ADC性能。

### ADC输入混音器配置

器件允许独立配置每个ADC输入混音器，接收有效输入源的任意组合。ADC混音器可接收来自麦克风PGA（1或2)、线入PGA（A或B)的输入，或者直接来自任意模拟输入对(IN1/IN2、IN3/IN4或IN5/IN6)的差分输入。然后ADC输入混音器将所选信号源连接至左声道和右声道ADC输入(表25和表26)。

## 录音通路FlexSound DSP

数字录音通路是基于FlexSound技术的DSP的一部分，由多级DSP电路组成。第一级DSP电路包括数字滤波器：语音滤波器(IIR)、音乐滤波器(FIR)和高通隔直流滤波器；下一级为双二阶数字滤波器，带有前置衰减放大器；其后是数字增益和电平控制级。录音通路DSP也具有数字侧音通路，连接并混音到数字回放通路(图14)。

### 录音通路数字滤波器

录音通路DSP包括数字滤波级。一个滤波器由MODE位设置(表27)，可选择IIR语音滤波和FIR音乐滤波：IIR滤波器优化用于标准($f_S$ = 8kHz)和宽带($f_S$ = 16kHz)语音应用，FIR滤波器优化用于降低较高音频/音乐采样率时的功耗。采样率超过48kHz ($f_{LRCLK}$ > 48kHz)时，使用FIR音频滤波器并将DHF置位。所选MODE配置作用于录音和回放通路DSP的两路通道。

录音通路DSP也具有隔直滤波器，该滤波器可与IIR语音及FIR音乐滤波器配合使用，阻塞低于音频波带低端的低频(包括DC)输入信号。

## 表25. 左声道ADC混音器输入配置寄存器

| ADDRESS: 0x15 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | MIXADL[6:0] | R/W | 0 | Selects microphone input 2 to left ADC mixer. |
| 5 | | R/W | 0 | Selects microphone input 1 to left ADC mixer. |
| 4 | | R/W | 0 | Selects line input B to left ADC mixer. |
| 3 | | R/W | 0 | Selects line input A to left ADC mixer. |
| 2 | | R/W | 0 | Selects IN5/IN6 differential input direct to left ADC mixer (WLP only). |
| 1 | | R/W | 0 | Selects IN3/IN4 differential input direct to left ADC mixer. |
| 0 | | R/W | 0 | Selects IN1/IN2 differential input direct to left ADC mixer. |

## 表26. 右声道ADC混音器输入配置寄存器

| ADDRESS: 0x16 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | MIXADR[6:0] | R/W | 0 | Selects microphone input 2 to right ADC mixer. |
| 5 | | R/W | 0 | Selects microphone input 1 to right ADC mixer. |
| 4 | | R/W | 0 | Selects line input B to right ADC mixer. |
| 3 | | R/W | 0 | Selects line input A to right ADC mixer. |
| 2 | | R/W | 0 | Selects IN5/IN6 differential input direct to right ADC mixer (WLP only). |
| 1 | | R/W | 0 | Selects IN3/IN4 differential input direct to right ADC mixer. |
| 0 | | R/W | 0 | Selects IN1/IN2 differential input direct to right ADC mixer. |

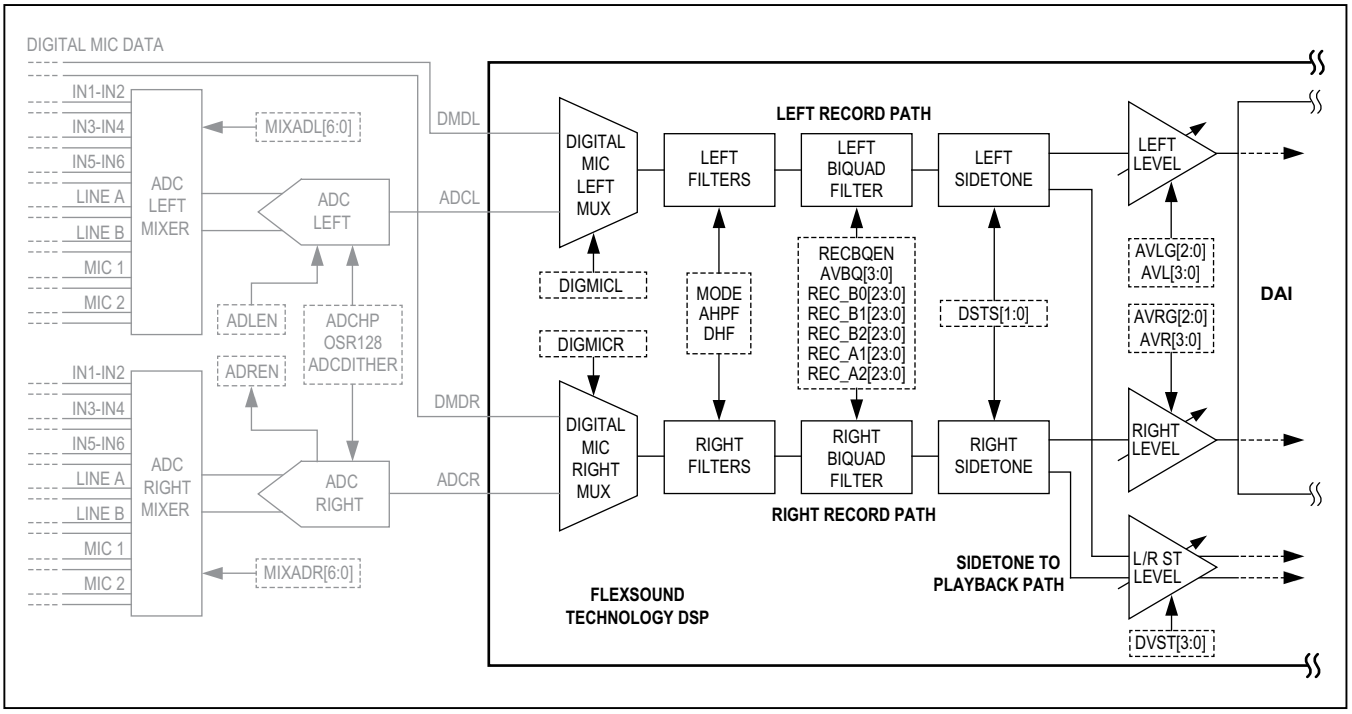



*图14. 录音通路FlexSound技术DSP框图*

## 表27. DSP滤波器配置寄存器

| ADDRESS: 0x26 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | MODE | R/W | 1 | **Enables the Codec DSP FIR Music Filters (Default IIR Voice Filters)**<br>0: The codec DSP filters operate in IIR voice mode with stop band frequencies below the $f_S$/2 Nyquist rate. The voice mode filters are optimized for 8kHz or 16kHz voice application use.<br>1: The codec DSP filters operate in a linear phase FIR audio mode optimized to maintain stereo imaging and operate at higher $f_S$ rates while utilizing lower power. |
| 6 | AHPF | R/W | 0 | **Enables the Record Path DC-Blocking Filter**<br>0: DC-blocking filter disabled.<br>1: DC-blocking filter enabled. |
| 5 | DHPF | R/W | 0 | **Enables the Playback Path DC-Blocking Filter**<br>0: DC-blocking filter disabled.<br>1: DC-blocking filter enabled. |
| 4 | DHF | R/W | 0 | **Enables the DAC High Sample Rate Mode (LRCLK > 48kHz, FIR Only)**<br>0: LRCLK is less than 48kHz. 8x FIR interpolation filter used.<br>1: LRCLK is greater than 48kHz. 4x FIR interpolation filter used. |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | — | — | — | — |
| 0 | — | — | — | — |

### 录音通路双二阶滤波器

录音通路DSP具有一级双二阶数字滤波器，带有可编程前置衰减放大器。数字式两级二阶滤波器配置应用于左、右声道录音。为使能录音通路的双二阶滤波器，将RECBQEN置高(表28)。使能后，可将前置衰减电平调节为0dB至-15dB (表示为$A_{V_BQ}$，见表29)。双二阶数字滤波器不能设置为增益大于±12dB、Q值大于10，或者低于最小$f_C$ (随滤波器类型变化)，请参见*Electrical Characteristics*表。

上电时没有初始化双二阶数字滤波器系数，如果使用滤波器，必须在使能器件和双二阶滤波器之前设置系数。传递函数为：

$$H(z) = \frac{B_0 + B_1 \times Z^{-1} + B_2 \times Z^{-2}}{A_0 + A_1 \times Z^{-1} + A_2 \times Z^{-2}}$$

## 表28. DSP双二阶滤波器使能寄存器

| ADDRESS: 0x41 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | RECBQEN | R/W | 0 | **Enable Biquad Filter in Record Path**<br>0: Biquad filter not used.<br>1: Biquad filter used in record path. |
| 2 | EQ3BANDEN | R/W | 0 | **Enable 3-Band EQ in Playback Path (Bands 4–7 Are Not Used)**<br>0: 3-band EQ disabled.<br>1: 3-band EQ enabled. Only valid if EQ7BANDEN = 0 and EQ5BANDEN = 0. |
| 1 | EQ5BANDEN | R/W | 0 | **Enable 5-Band EQ in Playback Path (Bands 6 and 7 Are Not Used)**<br>0: 5-band EQ disabled.<br>1: 5-band EQ enabled. Only valid if EQ7BANDEN = 0 |
| 0 | EQ7BANDEN | R/W | 0 | **Enable 7-Band EQ in Playback Path**<br>0 : 7-band EQ disabled.<br>1 : 7-band EQ enabled. This makes EQ5BANDEN and EQ3BANDEN redundant. |

## 表29. 录音通路双二阶数字前置放大器电平配置寄存器

| ADDRESS: 0x19 | | | | DESCRIPTION | | | |
|---|---|---|---|---|---|---|---|
| BIT | NAME | TYPE | POR | | | | |
| 7 | — | — | — | — | | | |
| 6 | — | — | — | — | | | |
| 5 | — | — | — | — | | | |
| 4 | — | — | — | — | | | |
| 3 | AVBQ[3:0] | R/W | 0 | **ADC Biquad Digital Preamplifier Gain Configuration** | | | |
| 2 | | | 0 | 0x0: +0dB | 0x4: -4dB | 0x8: -8dB | 0xC: -12dB |
| 1 | | | 0 | 0x1: -1dB | 0x5: -5dB | 0x9: -9dB | 0xD: -13dB |
| 0 | | | 0 | 0x2: -2dB | 0x6: -6dB | 0xA: -10dB | 0xE: -14dB |
| | | | | 0x3: -3dB | 0x7: -7dB | 0xB: -11dB | 0xF: -15dB |

双二阶数字滤波器具有五个用户可编程系数(B0、B1、B2、A1和A2)，每个系数长度为3字节(24位)(A0固定为1)。系数占用连续15个寄存器(表30)，每组三个寄存器(每个系数)必须连续设置才能生效。以二进制补码格式储存系数，前4位为整数部分，后20位为小数部分(所以每个系数的范围大约为+8至-8)。

### 录音通路侧音

提供录音通路侧音，允许将小幅度录音信号拷贝与回放音频信号进行混音。使能时，侧音可连接左声道、右声道，或者一分为二连接到两者，然后在回放通路DSP求和。侧音数字增益可设置为-0.5dB至-60.5dB (表31)。数字侧音功能通常用于通话，使讲话者能够听到自己的声音，提供更逼真的用户体验。

## 表30. 录音通路双二阶滤波器系数

| ADDRESS RANGE | | | NAME | TYPE | COEFFICIENT SEGMENT | | |
|---|---|---|---|---|---|---|---|
| 0xAF | 0xB0 | 0xB1 | RECORD BIQUAD COEFFICIENT B0 | R/W | REC_B0[23:16] | REC_B0[15:8] | REC_B0[7:0] |
| 0xB2 | 0xB3 | 0xB4 | RECORD BIQUAD COEFFICIENT B1 | R/W | REC_B1[23:16] | REC_B1[15:8] | REC_B1[7:0] |
| 0xB5 | 0xB6 | 0xB7 | RECORD BIQUAD COEFFICIENT B2 | R/W | REC_B2[23:16] | REC_B2[15:8] | REC_B2[7:0] |
| 0xB8 | 0xB9 | 0xBA | RECORD BIQUAD COEFFICIENT A1 | R/W | REC_A1[23:16] | REC_A1[15:8] | REC_A1[7:0] |
| 0xBB | 0xBC | 0xBD | RECORD BIQUAD COEFFICIENT A2 | R/W | REC_A2[23:16] | REC_A2[15:8] | REC_A2[7:0] |

## 表31. 录音通路侧音配置寄存器

| ADDRESS: 0x1A | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | DSTS[1:0] | | 0 | **Sidetone Enable and Digital Source Configuration**<br>00: No sidetone selected<br>01: Left channel<br>10: Right channel<br>11: Left + right channel |
| 6 | | | 0 | |
| 5 | — | — | — | — |
| 4 | DVST[4:0] | R/W | 0 | **Sidetone Digital Gain Configuration**<br>0x00: OFF<br>0x01: -0.5dB<br>0x02: -2.5dB<br>0x03: -4.5dB<br>0x04: -6.5dB<br>0x05: -8.5dB<br>0x06: -10.5dB<br>0x07: -12.5dB<br>0x08: -14.5dB<br>0x09: -16.5dB<br>0x0A: -18.5dB<br>0x0B: -20.5dB<br>0x0C: -22.5dB<br>0x0D: -24.5dB<br>0x0E: -26.5dB<br>0x0F: -28.5dB<br>0x10: -30.5dB<br>0x11: -32.5dB<br>0x12: -34.5dB<br>0x13: -36.5dB<br>0x14: -38.5dB<br>0x15: -40.5dB<br>0x16: -42.5dB<br>0x17: -44.5dB<br>0x18: -46.5dB<br>0x19: -48.5dB<br>0x1A: -50.5dB<br>0x1B: -52.5dB<br>0x1C: -54.5dB<br>0x1D: -56.5dB<br>0x1E: -58.5dB<br>0x1F: -60.5dB |
| 3 | | | 0 | |
| 2 | | | 0 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

### 录音通路数字增益和电平控制

立体声录音通路DSP包括数字增益和电平控制级，设置可按通道独立配置，主要用于调节数字麦克风录音电平。粗调数字增益调节可设置为0dB至+42dB，步长为6dB；精调电平控制增益可设置为-12dB至+3dB，步长为1dB (表32和33)。

## 表32. 左声道录音通路数字增益配置寄存器

| ADDRESS: 0x17 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | AVLG[2:0] | R/W | 0 | **Left Record Path Digital Coarse Gain Configuration**<br>000 : 0dB　010 : +12dB　100 : +24dB　110 : +36dB<br>001 : +6dB　011 : +18dB　101 : +30dB　111 : +42dB |
| 5 | | | 0 | |
| 4 | | | 0 | |
| 3 | AVL[3:0] | R/W | 0 | **Left Record Path Digital Fine Adjust Gain Configuration**<br>0x0: +3dB　0x4: -1dB　0x8: -5dB　0xC: -9dB<br>0x1: +2dB　0x5: -2dB　0x9: -6dB　0xD: -10dB<br>0x2: +1dB　0x6: -3dB　0xA: -7dB　0xE: -11dB<br>0x3: +0dB　0x7: -4dB　0xB: -8dB　0xF: -12dB |
| 2 | | | 0 | |
| 1 | | | 1 | |
| 0 | | | 1 | |

## 表33. 右声道录音通路数字增益配置寄存器

| ADDRESS: 0x18 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | AVRG[2:0] | R/W | 0 | **Right Record Path Digital Coarse Gain Configuration**<br>000 : 0dB　010 : +12dB　100 : +24dB　110 : +36dB<br>001 : +6dB　011 : +18dB　101 : +30dB　111 : +42dB |
| 5 | | | 0 | |
| 4 | | | 0 | |
| 3 | AVR[3:0] | R/W | 0 | **Right Record Path Digital Fine Adjust Gain Configuration**<br>0x0: +3dB　0x4: -1dB　0x8: -5dB　0xC: -9dB<br>0x1: +2dB　0x5: -2dB　0x9: -6dB　0xD: -10dB<br>0x2: +1dB　0x6: -3dB　0xA: -7dB　0xE: -11dB<br>0x3: +0dB　0x7: -4dB　0xB: -8dB　0xF: -12dB |
| 2 | | | 0 | |
| 1 | | | 1 | |
| 0 | | | 1 | |

## 数字音频接口(DAI)配置

数字音频接口(DAI)包含两个主要部分(图15)。第一部分为时钟控制和配置部分。器件支持主、从工作模式，支持256 x $f_S$或10MHz至60MHz范围的主控时钟，支持8kHz至96kHz范围的任意数字音频采样率($f_S$)。器件配置作为数字音频主机时，有多种工作模式，包括简单快速配置模式、整数采样模式和手动时钟分频模式；器件配置作为从机模式时，内部PLL快速锁定到外部LRCLK频率。

第二部分为数字音频数据通路控制和信号连接，该部分支持各种立体声数据通路配置，包括串行音频输入和输出、音频从录音通路至回放通路，以及音频从串行数据输入至串行数据输出环回。串行数据接口也支持多种标准数字音频格式(PCM)，包括$I^2S$、左对齐、右对齐和时分复用(TDM)。

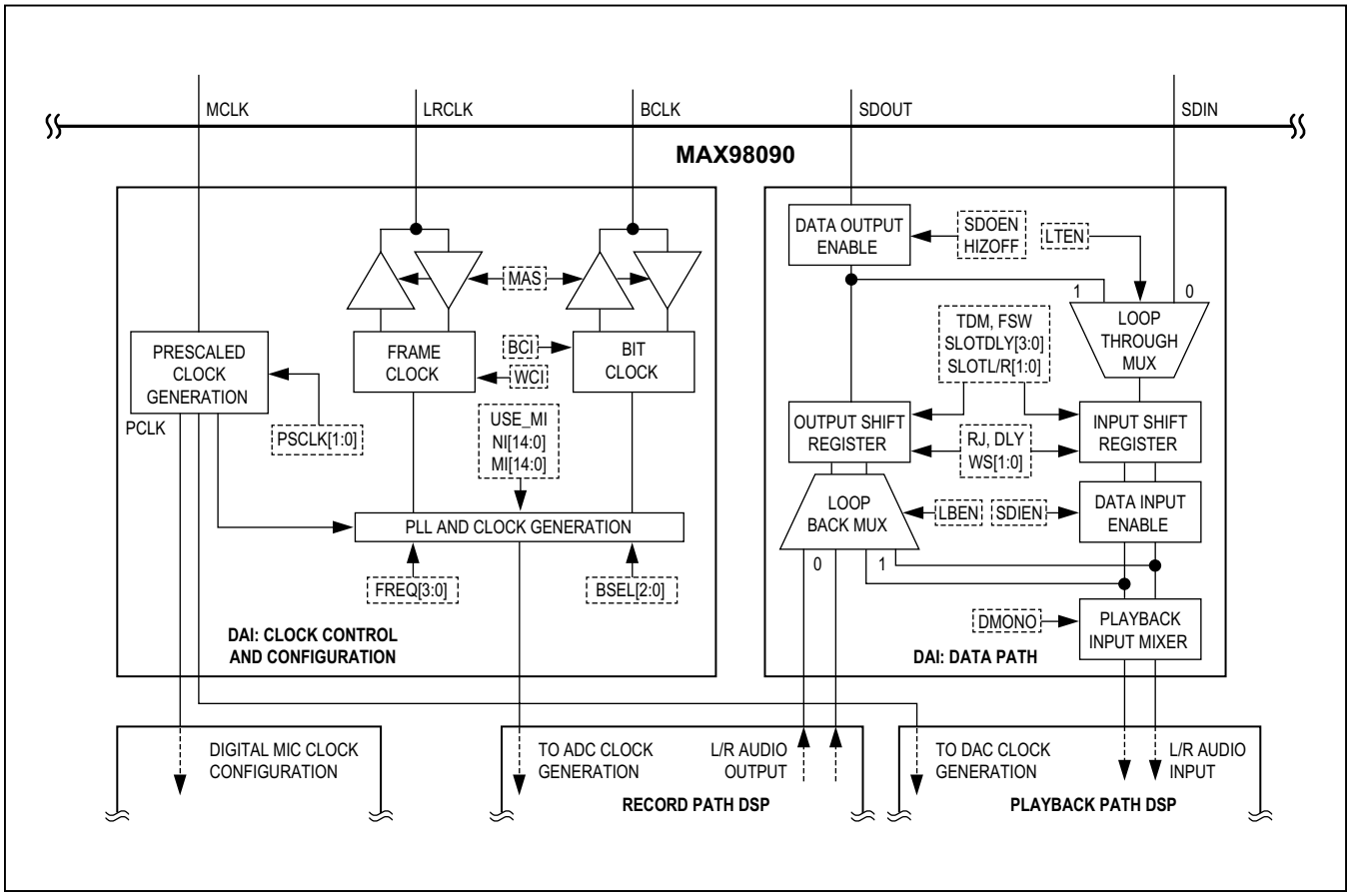



*图15. 数字音频接口简化方框图*

## DAI时钟控制和配置

时钟控制和配置部分是数字音频接口的两个主要电路之一。这部分负责接收和分频器件的主控时钟，用于产生内部数字时钟，以及用于数字音频接口数据时钟和定时。

器件支持频率范围为10MHz至60MHz的外部主控时钟(MCLK)。然而，对于数字操作、信号处理和数据转换，器件要求10MHz至20MHz范围的内部时钟。为产生该频率范围的内部主控时钟，使用内部时钟分频器(表34)。内部时钟分频器可设置为对MCLK进行1、2或4分频，以产生内部预分频主控时钟(PCLK)；然后直接或通过附加分频器/倍频器电路利用PCLK为全部内部数字部分提供时钟。

数字音频接口信号通路支持从8kHz至96kHz的任意采样率。器件只有一个DAI，所以录音(输出)和回放(输入)数字音频通路使用相同的采样率。

器件的数字音频接口支持主和从工作模式(表35)。为正确定时串行数据输入(SDIN)和输出(SDOUT)，DAI需要左、右声道帧时钟(LRCLK)和位时钟(BCLK)。主机模式下，器件使用几种模式之一由内部预分频主控时钟(PCLK)产生LRCLK和BCLK；然后在从机模式下，必须由外部提供LRCLK和BCLK。

## 主机模式时钟配置

器件配置为数字音频主机时，帧时钟(LRCLK)和位时钟(BCLK)配置作为输出，由器件利用内部预分频主控时钟(PCLK)产生。

如果在LRCLK和/或BCLK上没有时钟输出或非预期时钟输出，检查确认器件未处于关断状态，以及全部三个时钟均配置正确。如果未选择主控时钟预分频值(PSCLK[1:0])、未完整配置分频比(工作模式)，或者如果未设置位时钟速率(BSEL[2:0])，则不会输出有效时钟。除此之外，只有至少使能一路有效数据音频通路(ADC录音、DAC回放、数字麦克风输入等)时，器件才产生时钟。

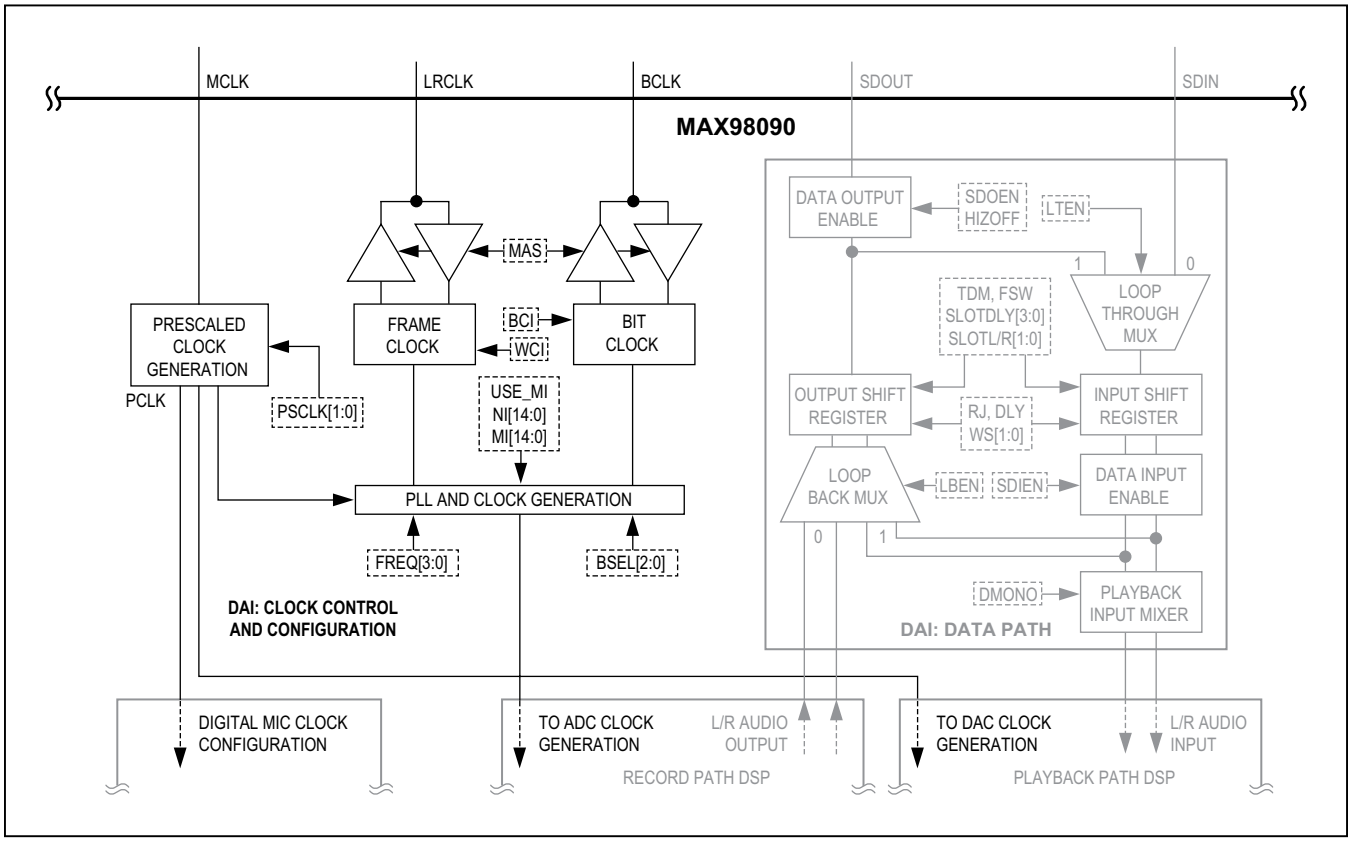



*图16. DAI时钟控制和配置部分*

## 表34. 系统主机模式时钟(MCLK)预分频配置寄存器

| ADDRESS: 0x1B | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | PSCLK[1:0] | R/W | 0 | **Master Clock (MCLK) Prescaler Configuration**<br>00: Internal master clock generation disabled<br>01: $f_{PCLK} = f_{MCLK}/1$, 10MHz ≤ $f_{MCLK}$ ≤ 20MHz<br>10: $f_{PCLK} = f_{MCLK}/2$, 20MHz < $f_{MCLK}$ ≤ 40MHz<br>11: $f_{PCLK} = f_{MCLK}/4$, 40MHz < $f_{MCLK}$ ≤ 60MHz |
| 4 | | | 0 | |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | — | — | — | — |
| 0 | — | — | — | — |

## 表35. 主机模式时钟配置寄存器

| ADDRESS: 0x21 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | MAS | R/W | 0 | Master Mode Enable<br>0: Slave mode<br>(LRCLK/BCLK are inputs and accept external clock sources).<br>1: Master mode<br>(LRCLK/BCLK are outputs and timing signals are generated internally). |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | BSEL[2:0] | R/W | 0 | **Bit Clock (BCLK) Configuration (Master Mode/Slave Right Justified Only)**<br>000: Bit clock disabled<br>001: $f_{BCLK} = 32 \times f_S$<br>010: $f_{BCLK} = 48 \times f_S$<br>011: $f_{BCLK} = 64 \times f_S$<br>100: $f_{BCLK} = f_{PCLK}/2$<br>101: $f_{BCLK} = f_{PCLK}/4$<br>110: $f_{BCLK} = f_{PCLK}/8$<br>111: $f_{BCLK} = f_{PCLK}/16$ |
| 1 | | | 0 | |
| 0 | | | 0 | |

主机模式下，器件分别利用两个整数值(NI和MI)作为倍频和分频器，将PCLK预分频为LRCLK。然后利用PCLK分频器或LRCLK倍频器产生BCLK(表35)。根据所选的过采样率(OSR，见*ADC功能配置*部分)和配置的NI/MI比，用下式计算输出LRCLK频率：

$$f_{LRCLK} = f_{PCLK} \times \frac{NI}{MI \times OSR}$$

该式说明，在主机模式下，LRCLK和PCLK频率(以及BCLK)之间的关系基于整数比；所以，MCLK的周期间抖动或绝对频率变动首先传递到PCLK，然后传递到LRCLK (以及BCLK)，取决于所选的时钟比。

主机模式下，器件提供三种时钟工作模式。实际上，全部三种模式的工作方式完全相同(使用内部MI和NI比值产生LRCLK)。然而，前两种模式在内部自动设置NI和MI，是配置常用PCLK与LRCLK比值的快捷方式。下文按照激活优先级顺序详细介绍三种工作模式。

### 快速配置模式

快速配置模式下，从常用频率列表中选择主控时钟频率(表36)和采样率(表37)。在任意给定时间只能使能每个快速设置寄存器中的一个位。同时使能主控时钟频率快速设置位和采样率快速设置位时，激活快速配置模式。一旦使能，该模式将取代其它两种工作模式，利用内部预设的NI和MI之比产生LRCLK；所以，使能快速配置模式时，保存但忽略整数模式设置(表32)和手动比值模式设置(表40至43)。如果随后禁止该模式，则较低优先级的工作模式设置重新生效。

为确保DSP配置最优且满足定时要求，在使用快速配置模式时，自动配置主控时钟分频器(PSCLK，表34)、数字滤波器(MODE，表27)和ADC过采样率(OSR128，表5)。处于快速配置模式时，这些寄存器固定，不能手动更改。该模式下，当采样率设置为8kHz或16kHz时，自动选择语音滤波器(IIR)，ADC过采样率固定为128；如果选择其它采样率，选择音乐滤波器(FIR)，配置ADC过采样率，以确保预分频主控时钟频率高于或等于256 x $f_S$。如果$f_{PCLK} \geq 256 \times f_S$，过采样率(OSR)设为128；否则，OSR设为64。表38列出了快速配置模式设置的完整查找表。

## 表36. 主控时钟快速设置寄存器

| ADDRESS: 0x04 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | 26M | R/W | 0 | Setup device for operation with a 26MHz master clock (MCLK). |
| 6 | 19P2M | R/W | 0 | Setup device for operation with a 19.2MHz master clock (MCLK). |
| 5 | 13M | R/W | 0 | Setup device for operation with a 13MHz master clock (MCLK). |
| 4 | 12P288M | R/W | 0 | Setup device for operation with a 12.288MHz master clock (MCLK). |
| 3 | 12M | R/W | 0 | Setup device for operation with a 12MHz master clock (MCLK). |
| 2 | 11P2896M | R/W | 0 | Setup device for operation with a 11.2896MHz master clock (MCLK). |
| 1 | — | — | — | — |
| 0 | $256F_S$ | R/W | 0 | Setup device for operation with a 256 x $f_S$ MHz master clock (MCLK) |

## 表37. 采样率快速设置寄存器

| ADDRESS: 0x05 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | SR_96K | R/W | 0 | Setup clocks and filters for a 96kHz sample rate. |
| 4 | SR_32K | R/W | 0 | Setup clocks and filters for a 32kHz sample fate. |
| 3 | SR_48K | R/W | 0 | Setup clocks and filters for a 48kHz sample rate. |
| 2 | SR_44K1 | R/W | 0 | Setup clocks and filters for a 44.1kHz sample rate. |
| 1 | SR_16K | R/W | 0 | Setup clocks and filters for a 16kHz sample rate. |
| 0 | SR_8K | R/W | 0 | Setup clocks and filters for an 8kHz sample rate. |

**整数模式**

整数模式下，主控时钟频率和采样率可设置为八种预编程组合之一(表39)。有四种不同的主控时钟频率(12MHz/13MHz/16MHz/19.2MHz)，每种可选择8kHz或16kHz采样率($f_S$)。选择配置之后，在内部将NI和MI位设置为正确比值。这些组合主要用于标准或宽带语音应用。

## 表38. 快速配置模式查找

| SELECTED MASTER CLOCK FREQUENCY | | | SELECTED SAMPLE RATE (kHz) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 8 | 16 | 32 | 44.1 | 48 | 96 |
| $f_{MCLK}$ | DIVIDER | $f_{PCLK}$ | VOICE FILTER (IIR) | | MUSIC FILTER (FIR) | | | |
| 26MHz | 2 | 13Mhz | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 64 |
| 19.2MHz | 1 | 19.2Mhz | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 64 |
| 13MHz | 1 | 13Mhz | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 64 |
| 12.288MHz | 1 | 12.288Mhz | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 64 |
| 12MHz | 1 | 12MHz | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 64 |
| 11.2896MHz | 1 | 11.2896MHz | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 64 | OSR = 64 |
| 256 x $f_S$ | 1 | 256 x $f_S$ | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 128 | OSR = 64 | — |
| | 2 | 128 x $f_S$ | — | — | — | — | — | OSR = 64 |

## 表39. 时钟模式配置寄存器

| ADDRESS: 0x1C | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | FREQ[3:0] | R/W | 0 | **Exact Integer Sampling Frequency (LRCLK) Configuration**<br>Configure the DAI for specific PCLK to LRCLK ratios for $f_S$ = 8kHz/16kHz operation (voice modes). Any setting other than 0x0 overrides manual ratio mode settings.<br>0000: Disabled 1XXX: Enabled Other combinations are reserved<br>When enabled, the following PCLK to LRCLK ratios are available:<br>1000: $f_{PCLK}$ = 12MHz, $f_{LRCLK}$ = 8kHz 1001: $f_{PCLK}$ = 12MHz, $f_{LRCLK}$ = 16kHz<br>1010: $f_{PCLK}$ = 13MHz, $f_{LRCLK}$ = 8kHz 1011: $f_{PCLK}$ = 13MHz, $f_{LRCLK}$ = 16kHz<br>1100: $f_{PCLK}$ = 16MHz, $f_{LRCLK}$ = 8kHz 1101: $f_{PCLK}$ = 16MHz, $f_{LRCLK}$ = 16kHz<br>1110: $f_{PCLK}$ = 19.2MHz, $f_{LRCLK}$ = 8kHz 1111: $f_{PCLK}$ = 19.2MHz, $f_{LRCLK}$ = 16kHz |
| 6 | | | 0 | |
| 5 | | | 0 | |
| 4 | | | 0 | |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | — | — | — | — |
| 0 | USE_MI | R/W | 0 | **Use MI[15:0] in Addition to NI[14:0] to set an Accurate Frequency Ratio**<br>0 : MI = 65536; NI = ($f_{LRCLK}$ / $f_{PCLK}$) x 65536 x 96<br>1 : MI is set to the value of MI[15:0] (Table 42 and Table 43). |

FREQ[3:0]寄存器设置为0 (FREQ[3:0] = 0000)时，禁止整数模式；MSB置1 (FREQ[3:0] = 1XXX)时，使能整数模式，其余位决定所选设置(表39)。如果使能整数模式，保存但忽略手动比值模式设置(表33至36)。然而，如果随后禁止该模式，手动比值配置模式重新生效。

### 手动比值配置模式

手动比值配置模式下，直接将NI和MI寄存器(表40至表43)配置为时钟比。只有禁止快速配置模式和整数模式时，手动比值配置模式才有效。手动比值配置模式下，如果USE_MI (表39)置0，MI则固定为其最大值0xFFFF (65536)，编程值无影响。为优化性能(尤其PCLK与LRCLK比值为非整数时)，将USE_MI置1并计算MI和NI。

采用以下方法计算正确的NI和MI值：

1) 选择过采样率(OSR)。如果$f_{PCLK} < 256 \times f_{LRCLK}$，则必须将OSR设置为64；否则，可将OSR设置为128或64。为优化新能，尽量选择OSR = 128。
2) 利用LRCLK频率以及所选的过采样率计算过采样频率：

$$f_{OSR} = f_{LRCLK} \times OSR.$$

3) 利用预分频主控时钟频率，以及预分频主控时钟频率和计算得到的过采样频率的最大公分母(GCD)，计算MI：

$$MI = f_{PCLK} / GCD(f_{PCLK}, f_{OSR})$$

4) 利用计算得到的过采样频率和MI值计算NI：

$$NI = f_{OSR} \times MI / f_{PCLK}$$

### 从机模式时钟配置

器件配置作为数字音频从机时，帧时钟(LRCLK)和位时钟(BCLK)配置作为外部输入。这些输入接收外部产生的帧和位时钟，然后内部PLL确定正确的PCLK与LRCLK频率比。在很少几个LRCLK周期内，内部PLL锁定至时钟比，然后自动正确设置内部分频比。

从机模式下，时钟发生寄存器设置没有影响(快速配置、整数模式和手动比值模式设置无影响)，仍然需要设置正确的MCLK至PCLK分频比、模式(语音/音频)和过采样率；然而其它全部时钟配置设置仅适用于主机模式。唯一例外是数字音频格式设置为从机模式采用右对齐数据时，在这一配置下，BCLK设置(BSEL[2:0]，表29)确定发送/接收每帧数据之前插入的前导位的数量(BCLK周期)。

## 表40. 手动时钟比配置寄存器(NI MSB)

| ADDRESS: 0x1D | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | NI[14:8] | R/W | 0 | Upper half of the PLL N value used in master mode clock generation to calculate the frequency ratio (manual ratio master mode). |
| 5 | | | 0 | |
| 4 | | | 0 | |
| 3 | | | 0 | |
| 2 | | | 0 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

表41. 手动配置时钟比寄存器(NI LSB)

| ADDRESS: 0x1E | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | NI[7:0] | R/W | 0 | Lower half of the PLL N value used in master mode clock generation to calculate the frequency ratio (manual ratio master mode). |
| 6 | | | 0 | |
| 5 | | | 0 | |
| 4 | | | 0 | |
| 3 | | | 0 | |
| 2 | | | 0 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

表42. 手动配置时钟比寄存器(MI MSB)

| ADDRESS: 0x1F | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | MI[15:8] | R/W | 0 | Upper half of the PLL M value used in master mode clock generation to calculate an accurate noninteger frequency ratio (manual ratio master mode). |
| 6 | | | 0 | |
| 5 | | | 0 | |
| 4 | | | 0 | |
| 3 | | | 0 | |
| 2 | | | 0 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

表43. 手动配置时钟比寄存器(MI MSB)

| ADDRESS: 0x20 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | MI[7:0] | R/W | 0 | Lower half of the PLL M value used in master mode clock generation to calculate an accurate noninteger frequency ratio (manual ratio master mode). |
| 6 | | | 0 | |
| 5 | | | 0 | |
| 4 | | | 0 | |
| 3 | | | 0 | |
| 2 | | | 0 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

### DAI数字音频数据通路控制和连接

数字音频数据通路部分支持各种立体声数据通路配置和格式(图17)。

标准配置是将录音通路数字音频输出连接到串行数据输出(录音通路至SDOUT)，或者将串行数据输入连接到数字音频回放通路(SDIN至回放通路)。这两种主要配置可单独使用或一起使用，取决于应用需要。

DAI数据通路也支持两种环路配置。环回模式接收数字音频串行数据输入，并将其连接至串行数据输出(SDIN至SDOUT)。环回模式允许录音通路的音频数据输出环回到数字音频播放通路(如果需要，可与录音通路组合为SDOUT配置)。表44详细列出了所有有效数据通路的组合设置，参见图18。

SDOUT可配置成在发送完所有数据位后变为高阻态，或驱动有效逻辑电平(LSB)。使能高阻模式时，SDOUT在LSB的BCLK沿之后快速变为高阻态，避免潜在的总线冲突。SDIN/环回音频数据可通过回放通路输入混音器，作为立体声音频数据或作为输入音频数据的单声道拷贝。默认设置下，禁止回放单声道模式，左、右声道输入音频数据分别连接至左、右回放通道。如果使能播放单声道模式，输入音频数据通道的幅值减小6dB (混音在一起，求和)，然后连接至左声道和右声道录音通路。表45详细列出了DAI数据通路配置控制位的完整清单。

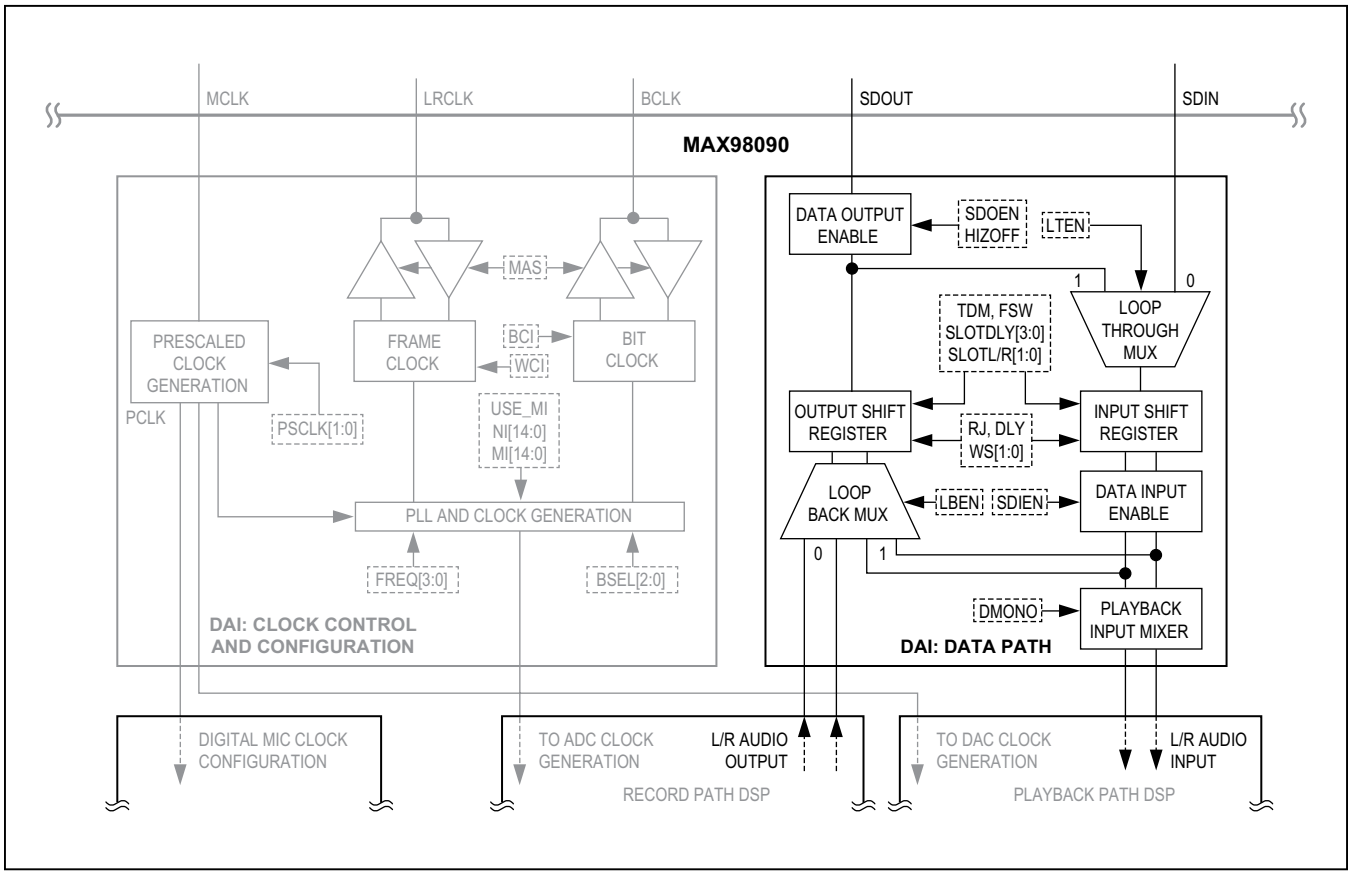



*图17. DAI数字数据通路配置*

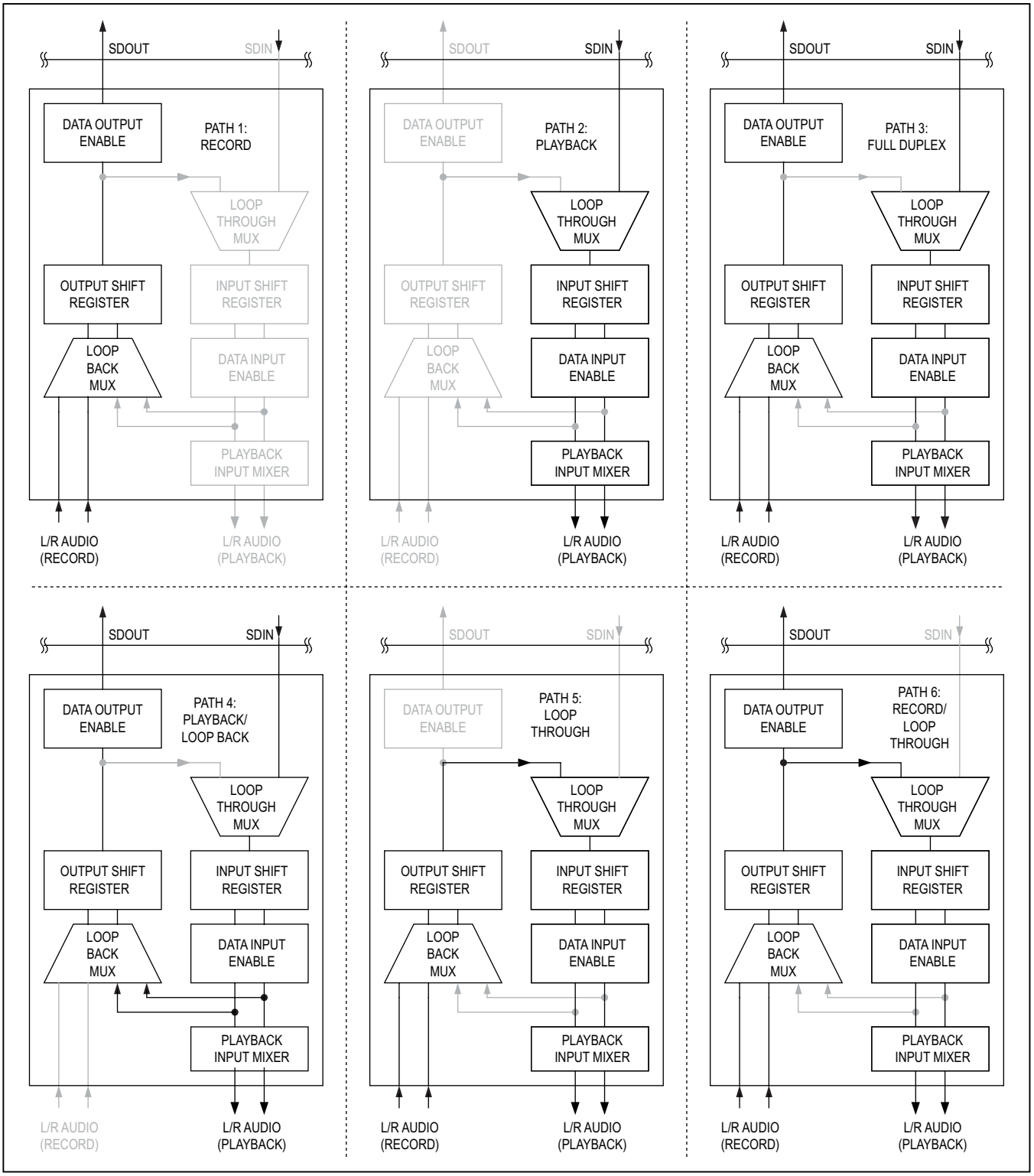



*图18. 数字音频接口(DAI)数据通路配置*

表44. 数字音频接口(DAI)数据通路配置

| DAI DATA PATH CONFIGURATION | | | | | |
|---|---|---|---|---|---|
| **PATH** | **DESCRIPTION** | **SDOEN** | **SDIEN** | **LTEN** | **LBEN** |
| — | DAI data path disabled | 0 | 0 | 0 | 0 |
| 1 | Record path to serial data output | 1 | 0 | 0 | 0 |
| 2 | Serial data input to playback path | 0 | 1 | 0 | 0 |
| 3 | Record path to serial data output/serial data input to playback path | 1 | 1 | 0 | 0 |
| 4 | Serial data input loop back to serial data output | 1 | 1 | 0 | 1 |
| 5 | Record path loop through to playback path | 0 | 1 | 1 | 0 |
| 6 | Record path to serial data output and loop through to playback path | 1 | 1 | 1 | 0 |
| — | Invalid configurations | All other combinations | | | |

表45. 数字音频接口(DAI)输入/输出配置寄存器

| ADDRESS: 0x25 | | | | DESCRIPTION |
|---|---|---|---|---|
| **BIT** | **NAME** | **TYPE** | **POR** | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | LTEN | R/W | 0 | **Enables Data Loop Through (Playback Path to Record Path)**<br>1: ADC to DAC loop-through enabled.<br>0: ADC to DAC loop-through disabled. |
| 4 | LBEN | R/W | 0 | **Enables Data Loop Back (SDIN to SDOUT)**<br>1: DAI SDIN used as SDOUT data source.<br>0: ADC used as SDOUT data source. |
| 3 | DMONO | R/W | 0 | **Enables Playback Mono Mode (SDIN L/2 + R/2 to Playback Path)**<br>1: The left- and right-channel SDIN audio input data are reduced in gain by 6dB, mixed together (summed), and routed to both the left and right record paths.<br>0: The left- and right-channel SDIN audio input data are routed to the left and right record path channels. |
| 2 | HIZOFF | R/W | 0 | **Disables Hi-Z Mode for SDOUT**<br>1: SDOUT drives a valid logic level after all data bits have been transmitted.<br>0: SDOUT goes to a high-impedance state after all data bits have been transmitted, allowing the SDOUT bus to be shared by other devices. |
| 1 | SDOEN | R/W | 0 | **Enables the Serial Data Output (SDOUT)**<br>1: Serial data output enabled.<br>0: Serial data output disabled. |
| 0 | SDIEN | R/W | 0 | **Enables the Serial Data Input (SDIN/Loop-Through)**<br>1: Serial data input enabled.<br>0: Serial data input disabled. |

### DAI数字音频数据格式

串行数据接口支持多种脉冲编码调制(PCM)数字音频格式，包括I²S、左对齐、右对齐和时分复用(TDM)。如果使能TDM模式，其优先级最高，DAI数据为TDM格式；这种情况下，所有非TDM数字音频数据格式配置寄存器无影响。

如果禁止TDM模式，数据格式由控制位所选的配置决定，详细信息请参见表46。这些设置可用于将DAI数据格式改为多种支持的标准，例如I²S (图19)、左对齐(图20)或右对齐(图21)。此外，配置设置可独立使能或禁止，允许器件支持多种非标准数据格式。

## 表46. 数字音频接口(DAI)格式配置寄存器

| ADDRESS: 0x22 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | RJ | R/W | 0 | **Configures the DAI for Right Justified Mode (No Data Delay)**<br>0: Left justified mode enabled with optional data delay.<br>1: Right justified mode enabled. DLY register is not used and BSEL[2:0] is used to determine the timing (see the *DAI Clock Control* and *Configuration* section for details).<br>**Note:** TDM has priority over all other data formats. |
| 4 | WCI | R/W | 0 | **Configures the DAI for Frame Clock (LRCLK) Inversion**<br>TDM = 0:<br>1: Right-channel data is transmitted while LRCLK is low.<br>0: Left-channel data is transmitted while LRCLK is low.<br>TDM = 1:<br>0: Start of a new frame is signified by the rising edge of the LRCLK pulse.<br>1: Start of a new frame is signified by the falling edge of the LRCLK pulse. |
| 3 | BCI | R/W | 0 | **Configures the DAI for Bit Clock (BCLK) Inversion**<br>1: SDIN is accepted on the falling edge of BCLK.<br>0: SDIN is accepted on the rising edge of BCLK.<br>Master Mode:<br>1: LRCLK transitions occur on the rising edge of BCLK.<br>0: LRCLK transitions occur on the falling edge of BCLK. |
| 2 | DLY | R/W | 0 | **Configures the DAI for Data Delay (I²S Standard)**<br>1: The most significant bit of an audio word is latched at the second BCLK edge after the LRCLK transition.<br>0: The most significant bit of an audio word is latched at the first BCLK edge after the LRCLK transition.<br>Set DLY = 1 to conform to the I²S standard. DLY is only effective when TDM = 0. |
| 1 | WS[1:0] | R/W | 0 | **DAI Input Data Word Size (TDM = 0)**<br>If RJ = 1:<br>00: 16 bits 01: 20 bits 10: 24 bits 11: Reserved<br>If RJ = 0:<br>00: 16 bits 01, 10, 11: 20 bits |
| 0 | | | 0 | |

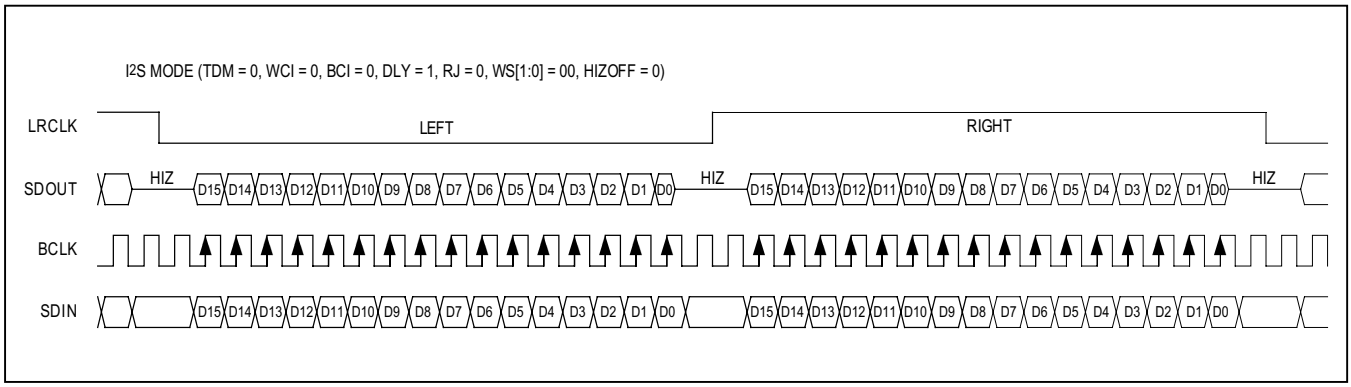



*图19. DAI时序，I2S数据格式*

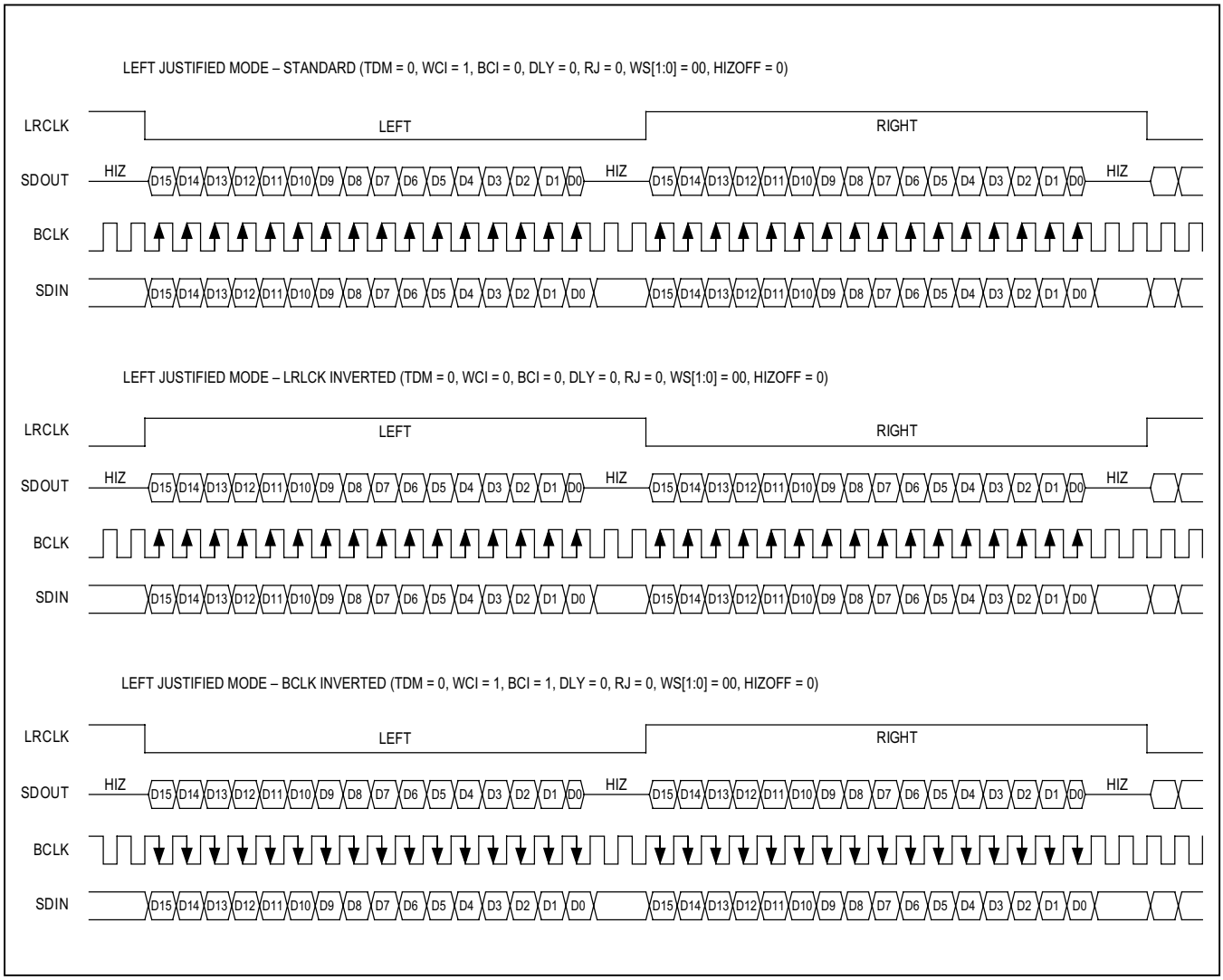



*图20. DAI时序，左对齐数据格式*

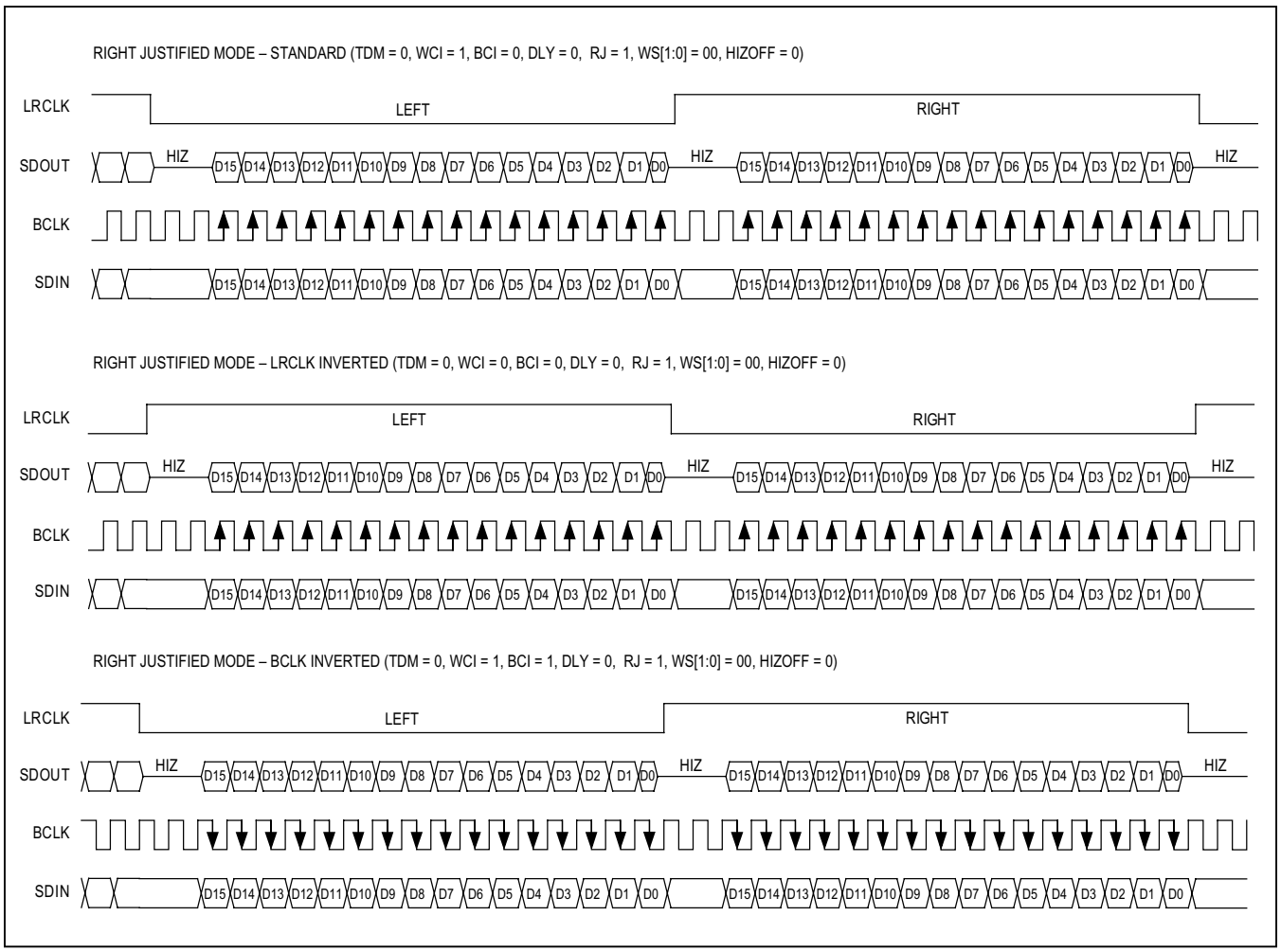



*图21. DAI时序，右对齐数据格式*

### TDM模式数据格式

如果使能TDM模式(表47)，表39中的寄存器设置没有影响。TDM模式支持每帧多达4个单声道音频时隙的格式。然而，器件内部只有2个数字音频通道(左声道和右声道)，可分配给4个可用时隙帧中的任意2个(图48)。其余两个时隙保持空闲，可供另一器件使用。可为每个时隙帧独立设置数据延时；工作在主机模式时，可设置为每个位或整个字发送帧同步脉冲。图22中详细给出了常用配置选项的TDM模式时序。

## 表47. 数字音频接口(DAI) TDM控制寄存器

| ADDRESS: 0x23 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | FSW | R/W | 0 | **Configures the DAI Frame Sync Pulse Width (TDM = 1 and MAS = 1)**<br>1: Frame sync pulse has a 50% duty cycle.<br>0: Frame sync pulse is one bit wide.<br>**Note:** In slave mode, the device accepts a frame sync pulse width up to frame width - 1. |
| 0 | TDM | R/W | 0 | **Enable for Time Division Multiplex (TDM) Mode**<br>1: Enable TDM mode and configures the DAI to transmit and receive TDM data.<br>0: Disable TDM mode. |

## 表48. 数字音频接口(DAI) TDM格式寄存器

| ADDRESS: 0x24 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | SLOTL[1:0] | R/W | 0 | **Selects the Time Slot to use for Left-Channel Data in TDM Mode**<br>00: Time slot 1 10: Time slot 3<br>01: Time slot 2 11: Time slot 4 |
| 6 | | | 0 | |
| 5 | SLOTR[1:0] | R/W | 0 | **Selects the Time Slot to use for Right-Channel Data in TDM Mode**<br>00: Time slot 1 10: Time slot 3<br>01: Time slot 2 11: Time slot 4 |
| 4 | | | 0 | |
| 3 | SLOTDLY[3:0] | R/W | 0 | Enables data delay for slot 4 in TDM mode. |
| 2 | | | 0 | Enables data delay for slot 3 in TDM mode. |
| 1 | | | 0 | Enables data delay for slot 2 in TDM mode. |
| 0 | | | 0 | Enables data delay for slot 1 in TDM mode. |

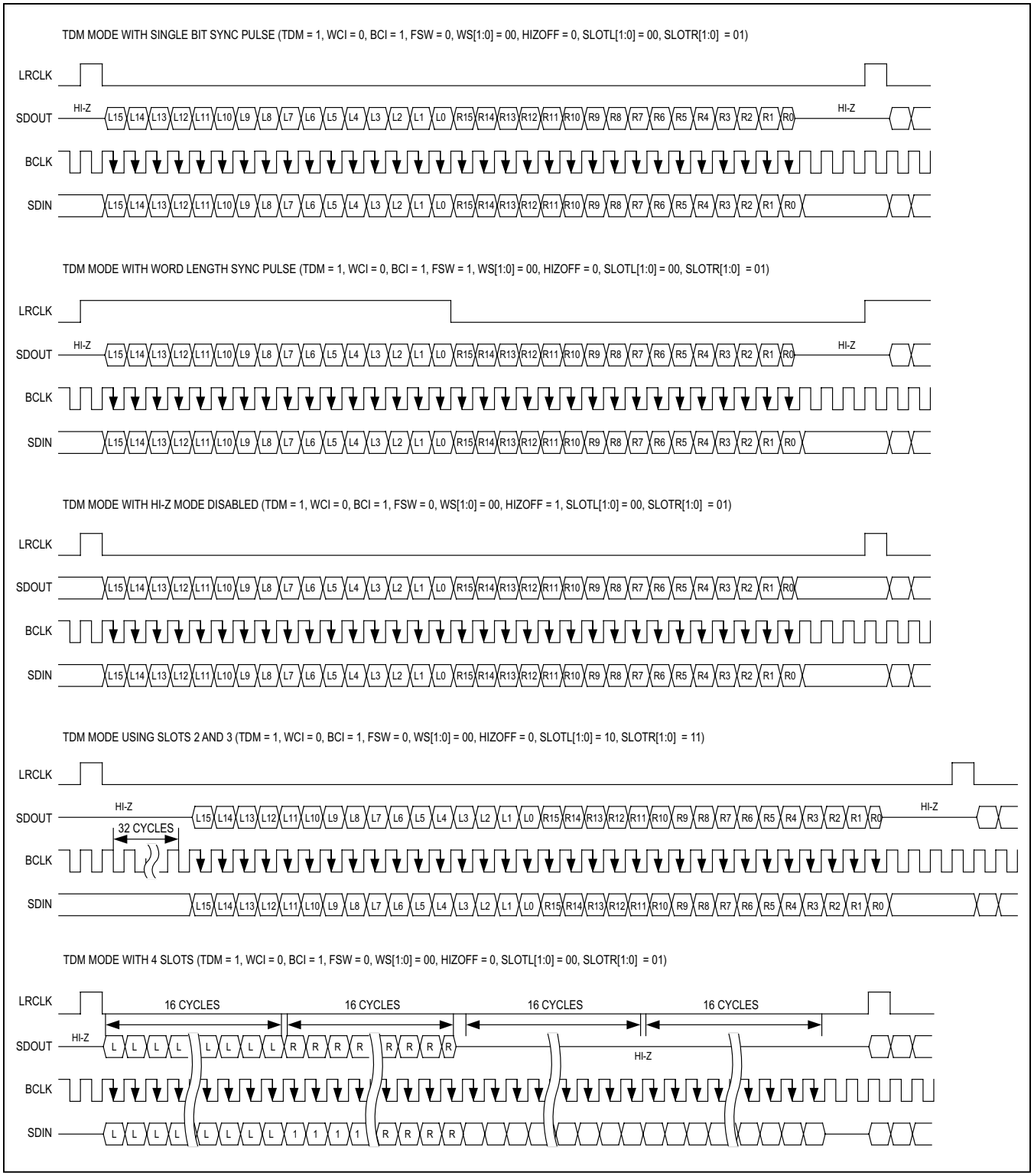



*图22. DAI时序，TDM数据格式*

## 音频回放通路

器件回放通路具有两个通道(左声道和右声道)，可接收来自DAI和/或录音通路侧音的数字音频输入；然后使数字音频通过FlexSound DSP的几级电路，最终连接到数/模转换器(图23)。

### 回放通路FlexSound DSP

回放通路的第一级采用Maxim FlexSound DSP技术，第一级接收DAI输入并将其与录音通路侧音(如使能)混音，包括独立的数字增益和数字电平控制电路。该级之后是三级立体声DSP，包括7波段参数均衡器、动态范围控制(DRC)和数字滤波器。回放通路数字输出连接至DAC，在此转换成模拟格式后再送至模拟输出混音器。

### 回放通路数字增益和电平控制

立体声回放通路DSP包括独立的数字增益和电平控制电路(图24)。与录音通路不同，回放通路的两个通道(左声道和右声道)共用相同的数字增益和电平控制设置。粗调数字增益级接收来自DAI的数字输出，可设置为0dB至+18dB，步长6dB。微调电平控制级的输入是粗调增益级输出与录音通路测试信号之和，可在-15dB至0dB之间调节，步长1dB(表49)。回放通路增益和电平控制级也包括静音使能。

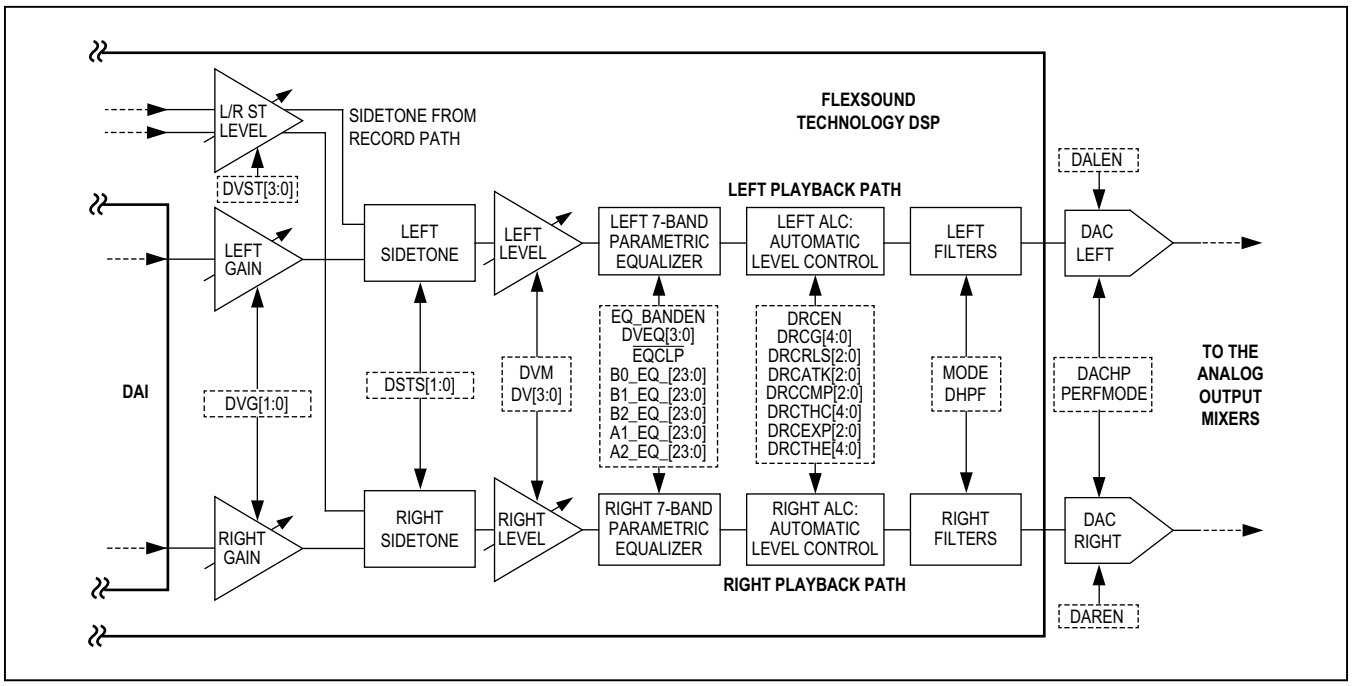



*图23. 回放通路框图*

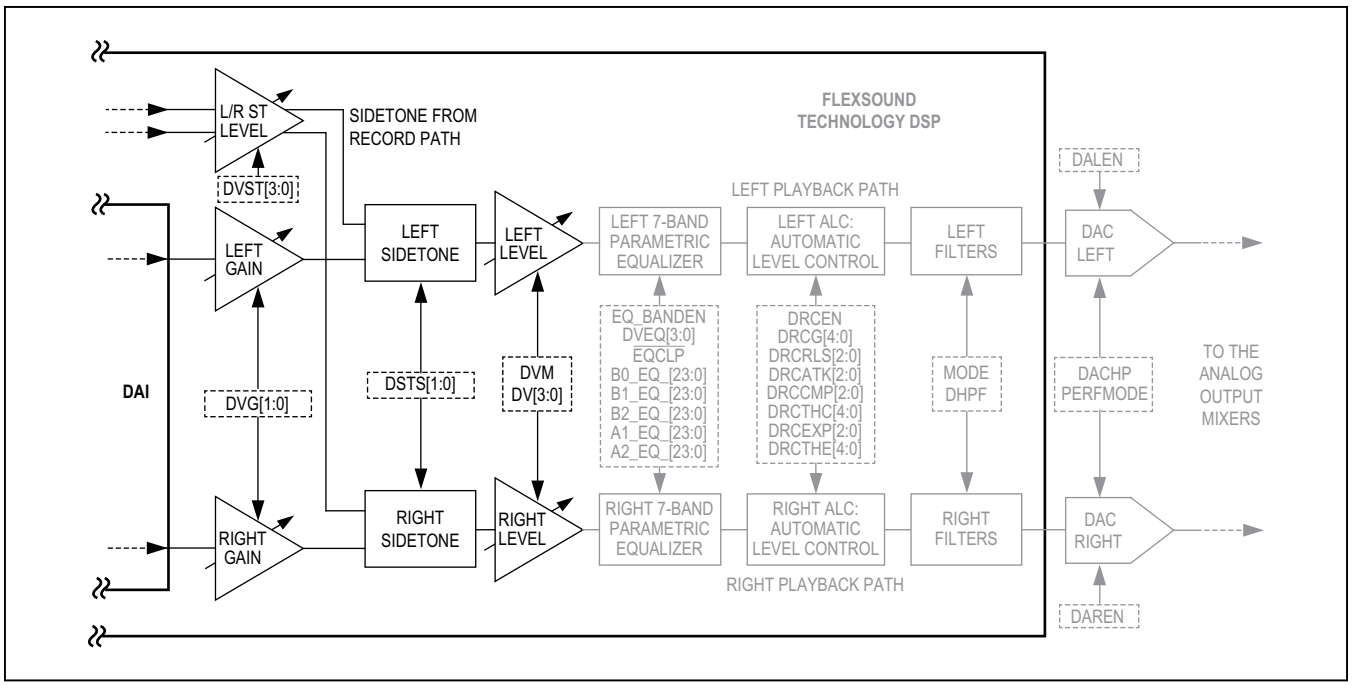



*图24. 回放通路侧音和电平控制*

## 表49. 回放增益和电平配置寄存器

| ADDRESS: 0x27 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | DVM | R/W | 0 | Enables the playback path data input mute. |
| 6 | — | — | — | — |
| 5 | DVG[1:0] | R/W | 0 | **Playback Path Coarse Adjust Gain Configuration**<br>00: 0dB 10: +12dB<br>01: +6dB 11: +18dB |
| 4 | | | 0 | |
| 3 | DV[3:0] | R/W | 0 | **Playback Path Fine Level Control Configuration**<br>0x0: 0dB 0x4: -4dB 0x8: -8dB 0xC: -12dB<br>0x1: -1dB 0x5: -5dB 0x9: -9dB 0xD: -13dB<br>0x2: -2dB 0x6: -6dB 0xA: -10dB 0xE: -14dB<br>0x3: -3dB 0x7: -7dB 0xB: -11dB 0xF: -15dB |
| 2 | | | 0 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

### 回放通路7波段参数均衡器

回放通路DSP具有7波段参数均衡器，带有削波检测和可编程前置衰减放大器(图25)。7个波段中的每个波段均为完备、可独立编程的双二阶数字滤波器。给定波段的配置作用于左、右播放声道。

参数均衡器可在3波段、5波段或完整7波段配置下使能(表50)。使能参数均衡器后，即可设置削波检测，前置衰减电平可调节为0dB至-15dB (表示为AV_EQ，见表51)。单波段双二阶滤波器不能设置在增益> ±12dB、Q值> 10，或者低于最小$f_C$ (随滤波器类型变化)，参见*电气特性*表。

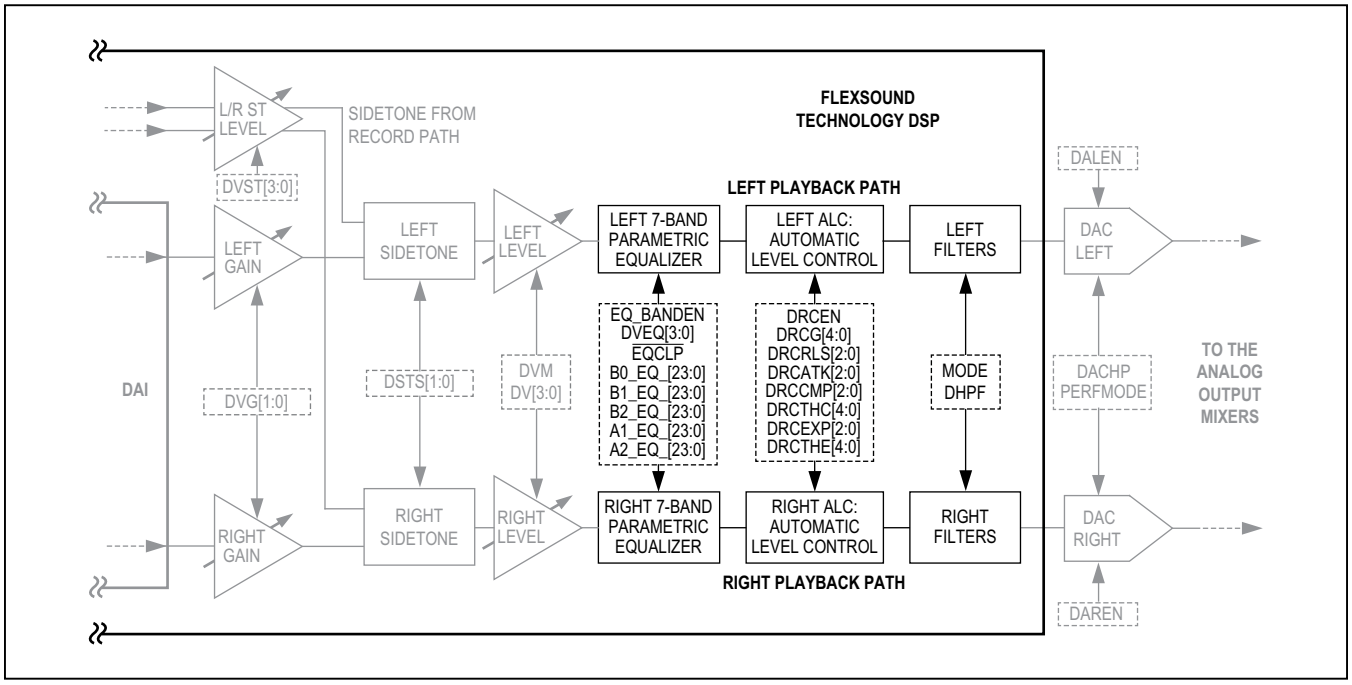



*图25. 回放通路DSP*

## 表50. DSP双二阶滤波器使能寄存器

| ADDRESS: 0x41 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | RECBQEN | R/W | 0 | **Enable Biquad Filter in Record Path**<br>0: Biquad filter not used.<br>1: Biquad filter used in ADC path. |
| 2 | EQ3BANDEN | R/W | 0 | **Enable 3-Band EQ in DAC Path (Bands 4–7 Are Not Used)**<br>0: 3-band EQ disabled.<br>1: 3-band EQ enabled. Only valid if EQ7BANDEN == 0 and EQ5BANDEN == 0. |
| 1 | EQ5BANDEN | R/W | 0 | **Enable 5-Band EQ in DAC Path (Bands 6 and 7 Are Not Used)**<br>0: 5-band EQ disabled.<br>1: 5-band EQ enabled. Only valid if EQ7BANDEN == 0 |
| 0 | EQ7BANDEN | R/W | 0 | **Enable 7-Band EQ in DAC Path**<br>0: 7-band EQ disabled.<br>1: 7-band EQ enabled. This makes EQ5BANDEN and EQ3BANDEN redundant. |

## 表51. 参数均衡回放电平配置寄存器

| ADDRESS: 0x28 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | EQCLP | R/W | 0 | **Enables DAI Digital Input Equalizer Clipping Detection**<br>1: Equalizer clip detect disabled.<br>0: Equalizer clip detect enabled. |
| 3 | DVEQ[3:0] | R/W | 0 | **DAI Digital Input Equalizer Attenuation Level Configuration ($A_{V\_EQ}$)**<br>0x0: 0dB 0x4: -4dB 0x8: -8dB 0xC: -12dB<br>0x1: -1dB 0x5: -5dB 0x9: -9dB 0xD: -13dB<br>0x2: -2dB 0x6: -6dB 0xA: -10dB 0xE: -14dB<br>0x3: -3dB 0x7: -7dB 0xB: -11dB 0xF: -15dB |
| 2 | | | 0 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

上电时不对参数均衡器系数进行初始化，如果需要，应在使能器件和均衡器之前设置系数。每个波段的传递函数定义为：

$$H(z) = \frac{B_0 + B_1 \times Z^{-1} + B_2 \times Z^{-2}}{A_0 + A_1 \times Z^{-1} + A_2 \times Z^{-2}}$$

每一波段中的双二阶滤波器均具有五个用户可编程系数(B0、B1、B2、A1和A2)，每个系数长度为3字节(24位)(A0固定为1)，每个波段的系数占用连续15个寄存器，全部7个波段共占用连续105个寄存器(表52)。每组三个寄存器(每个系数)必须连续设置才能生效。以二进制补码格式储存系数，前4位为整数部分，后20位为小数部分(所以每个系数的范围大约为+8至-8)。

## 表52. 参数均衡器波段N (1–7)的双二阶滤波器系数寄存器

| ADDRESS RANGE (BY BAND) | | | | | | | NAME | TYPE | COEFFICIENT SEGMENT |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | |
| 0x46 | 0x55 | 0x64 | 0x73 | 0x82 | 0x91 | 0xA0 | Equalizer Band N Coefficient B0 | R/W | B0_N[23:16] |
| 0x47 | 0x56 | 0x65 | 0x74 | 0x83 | 0x92 | 0xA1 | | R/W | B0_N[15:8] |
| 0x48 | 0x57 | 0x66 | 0x75 | 0x84 | 0x93 | 0xA2 | | R/W | B0_N[7:0] |
| 0x49 | 0x58 | 0x67 | 0x76 | 0x85 | 0x94 | 0xA3 | Equalizer Band N Coefficient B1 | R/W | B1_N[23:16] |
| 0x4A | 0x59 | 0x68 | 0x77 | 0x86 | 0x95 | 0xA4 | | R/W | B1_N[15:8] |
| 0x4B | 0x5A | 0x69 | 0x78 | 0x87 | 0x96 | 0xA5 | | R/W | B1_N[7:0] |
| 0x4C | 0x5B | 0x6A | 0x79 | 0x88 | 0x97 | 0xA6 | Equalizer Band N Coefficient B2 | R/W | B2_N[23:16] |
| 0x4D | 0x5C | 0x6B | 0x7A | 0x89 | 0x98 | 0xA7 | | R/W | B2_N[15:8] |
| 0x4E | 0x5D | 0x6C | 0x7B | 0x8A | 0x99 | 0xA8 | | R/W | B2_N[7:0] |
| 0x4F | 0x5E | 0x6D | 0x7C | 0x8B | 0x9A | 0xA9 | Equalizer Band N Coefficient A1 | R/W | A1_N[23:16] |
| 0x50 | 0x5F | 0x6E | 0x7D | 0x8C | 0x9B | 0xAA | | R/W | A1_N[15:8] |
| 0x51 | 0x60 | 0x6F | 0x7E | 0x8D | 0x9C | 0xAB | | R/W | A1_N[7:0] |
| 0x52 | 0x61 | 0x70 | 0x7F | 0x8E | 0x9D | 0xAC | Equalizer Band N Coefficient A2 | R/W | A2_N[23:16] |
| 0x53 | 0x62 | 0x71 | 0x80 | 0x8F | 0x9E | 0xAD | | R/W | A2_N[15:8] |
| 0x54 | 0x63 | 0x72 | 0x81 | 0x90 | 0x9F | 0xAE | | R/W | A2_N[7:0] |

### 回放通路动态范围控制

回放通路包括动态范围控制(DRC)电路(图25)。DRC配置具有很高灵活性，带有数字补偿增益、动态范围压缩和扩展，以及可编程响应和释放时间。

器件的动态范围由配置的信号通路满幅值与RMS噪底幅值之差决定。为避免降低性能，动态范围一般小于所选信号通路的动态范围。禁止动态范围控制时，输入动态范围等于输出动态范围(图26)。使能压缩时，如果输入信号幅值超过压缩门限，则以所选择的压缩比减小增益，使得经过压缩的输出动态范围比输入动态范围小。使能扩展模式时，如果输入信号幅值下降至扩展门限以下，则以所选择的扩展比减小增益，得到较大的输出动态范围扩展。

DRC也具有数字补偿增益控制(表54)，可设置为0dB至12dB，步长1dB。图27所示为使能DRC时，采用或没有采用数字补偿增益的效果。

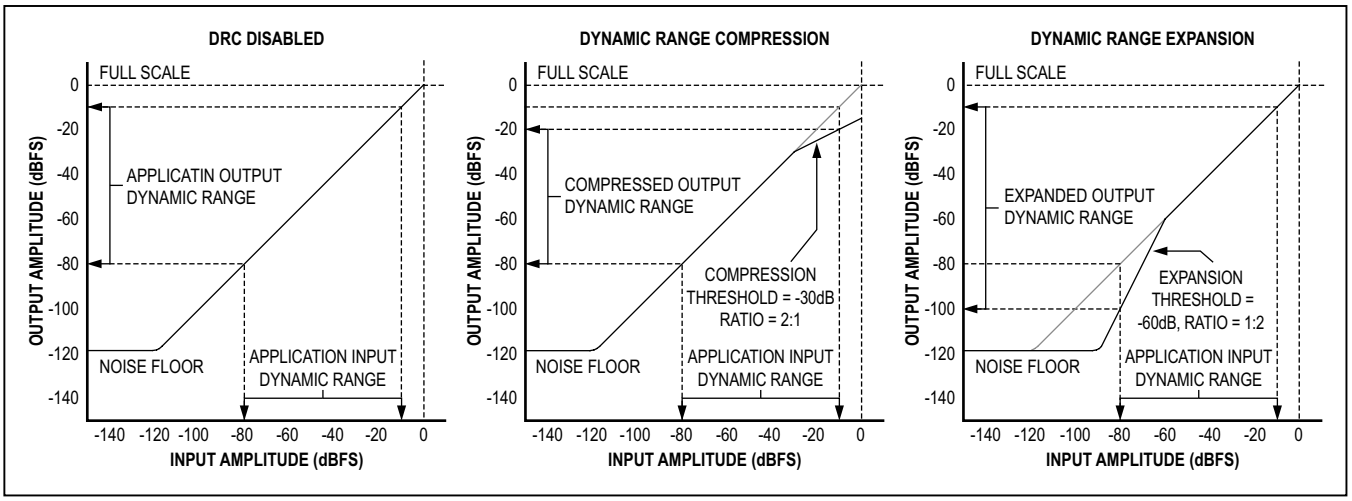



*图26. 动态范围压缩和扩展*

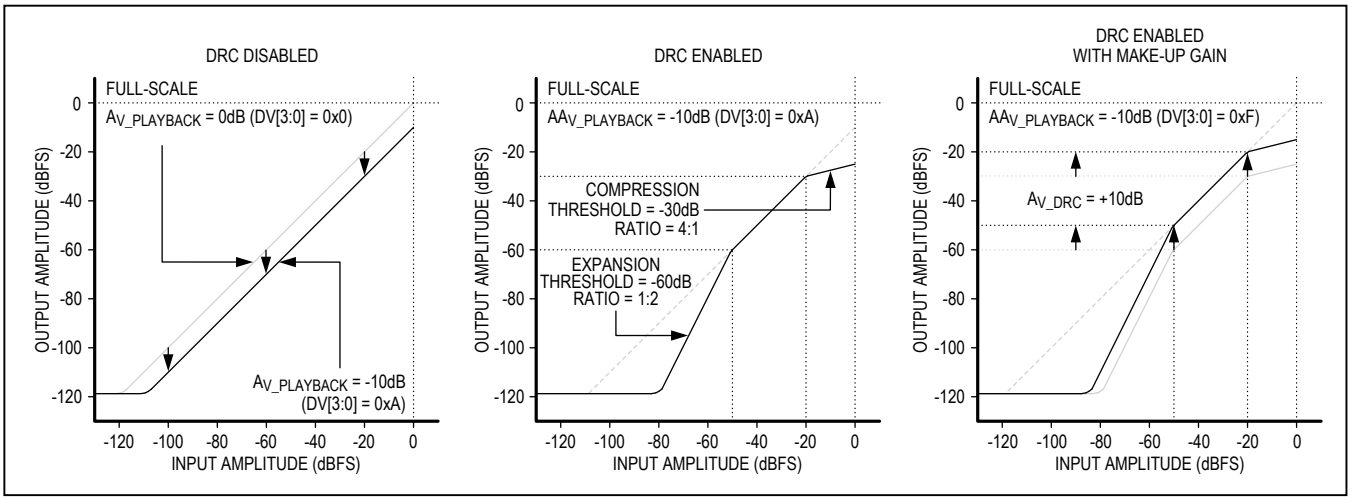



*图27. DRC使能和补偿增益*

DRC具有两个可编程信号门限。高幅值压缩门限用于确保最大信号幅值不会发生音频削波。压缩比可设置为5个选项之一，比值1:1到无穷大比1 (或者当输入幅值增大时使输出幅值扁平化)；压缩门限可配置为-31dB至0dB。压缩比和门限范围如图28所示。

低幅值压缩门限可避免放大背景噪声。信号电平降至扩展门限以下时，DRC减小增益，直到信号上升至门限以上。扩展比可设置为1:1、1:2或1:3，门限可配置为35dB至66dB。扩展比和门限范围如图29所示。

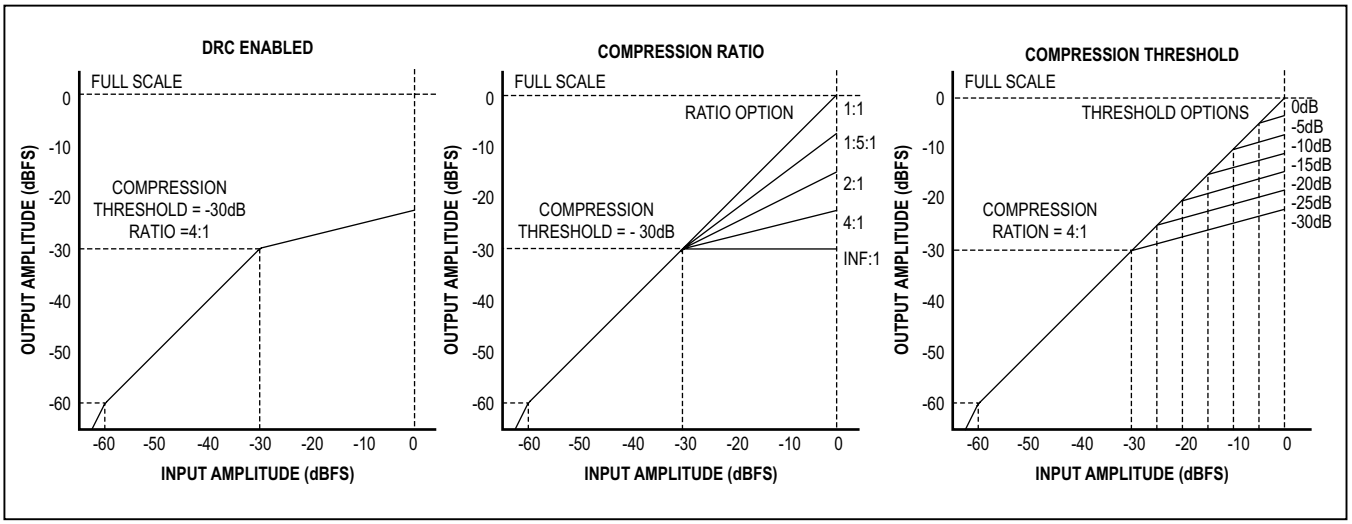



*图28. DRC压缩比和门限*

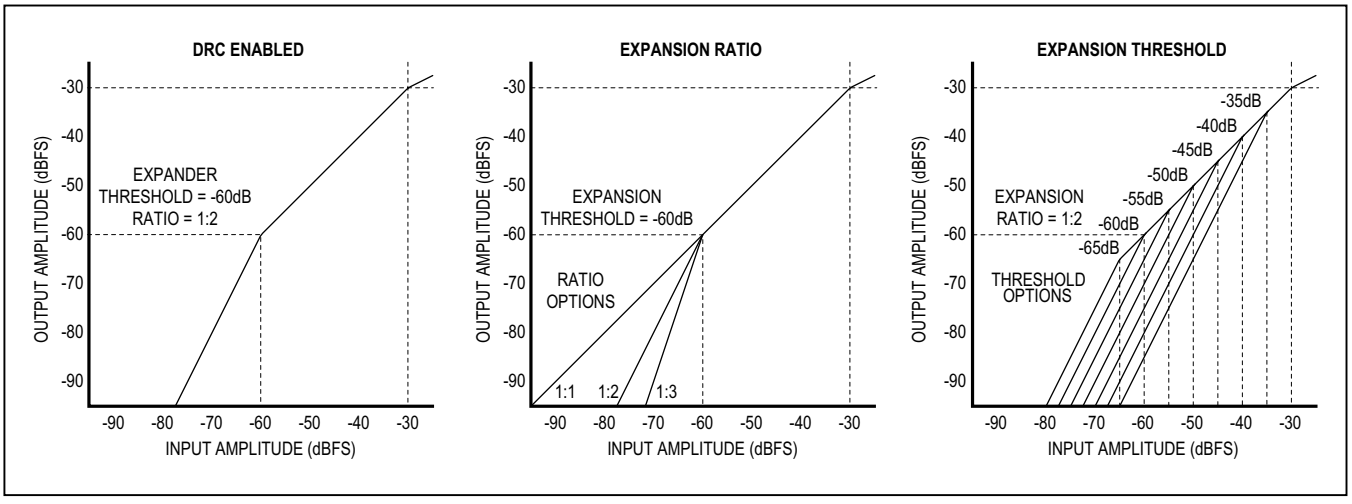



*图29. DRC扩展比和门限*

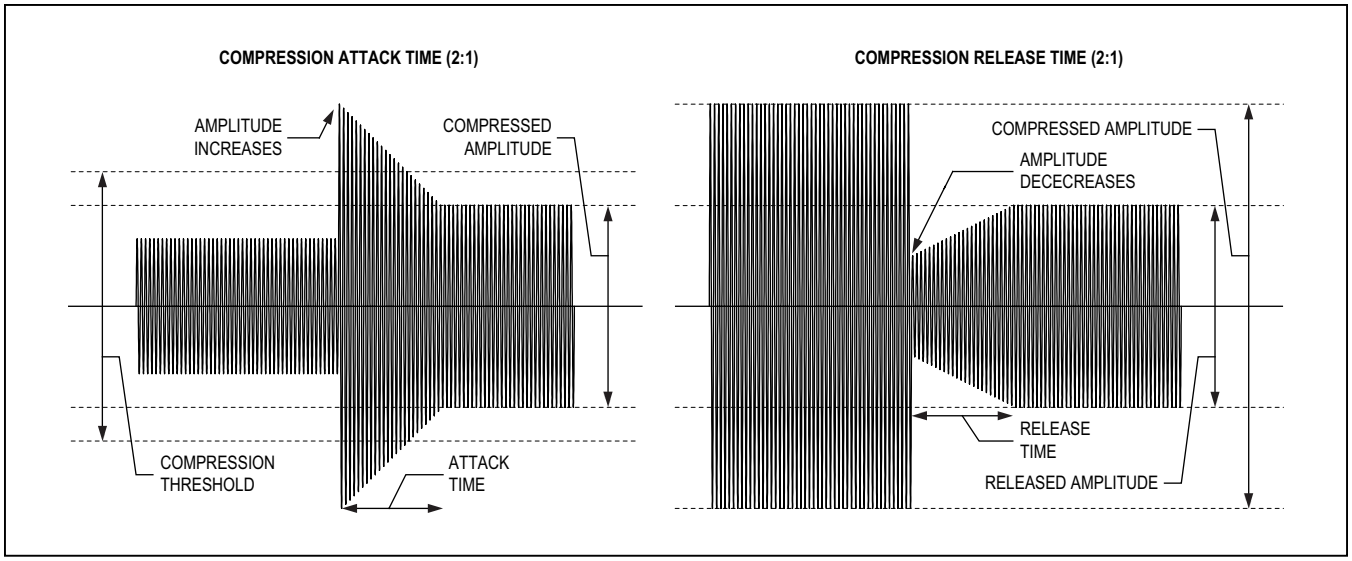



*图30. DRC响应和释放时间波形*

DRC提供宽范围的可编程响应、释放时间(表53)。使能压缩时，如果信号幅值增大至超过压缩门限，响应时间将决定实际所选压缩比的使能速度；信号幅值降低至压缩门限以下时，释放时间将决定恢复常规增益的速度(图30)。

使能扩展时，如果信号幅值降低至扩展门限以下，释放时间则决定所选扩展比的使能速度；信号幅值增大到压缩门限以下时，响应时间决定恢复常规增益的速度。

响应和释放时间不是绝对的，而是用于设置信号幅值高于或低于相应门限时调节增益的速率；因此，所选响应/释放时间与新信号幅值与所选压缩或扩展门限之比有关。表53中所列数值均假设输入信号幅值超过相应门限达到12dB(高于压缩门限及低于扩展门限)。如果超过相应门限的比值较大或较小，响应时间会相应增大或减小，变化量与以dB为单位的变化比成比例。例如，变化比为6dB时，释放时间减小50%。

对于压缩，如果信号幅值超过门限12dB，进入压缩时的响应时间与所选配置严格一致；同样，退出压缩时，释放时间由幅值下降之前超过门限的比值决定。

除两点区别之外，扩展工作方式也完全相同：信号幅值下降至扩展门限以下(而非高于压缩门限)时，使能扩展比，释放时间(而非响应时间)决定进入扩展所需的时间(以扩展门限以下12dB为中心)；同样，退出扩展模式时将使用响应时间。此外，进入扩展时，初始输入幅值与扩展门限之比决定了使能扩展比之前的延时；该延时以扩展门限以上12dB为中心，由所选释放时间决定。退出扩展时，响应时间之前没有延迟。

## 表53. 动态范围控制(DRC)定时寄存器

| ADDRESS: 0x33 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | DRCEN | R/W | 0 | **PLAYBACK DRC Enable**<br>0: DRC disabled.<br>1: DRC enabled. |
| 6 | DRCRLS[2:0] | R/W | 0 | **PLAYBACK DRC Release Time Configuration (12dB Relative to Threshold)**<br>0x0: 8s 0x2: 2s 0x4: 0.5s 0x6: 0.125s<br>0x1: 4s 0x3: 1s 0x5: 0.25s 0x7: 0.0625s |
| 5 | | R/W | 0 | |
| 4 | | R/W | 0 | |
| 3 | — | — | — | — |
| 2 | DRCATK[2:0] | R/W | 0 | **PLAYBACK DRC Attack Time Configuration (12dB Relative to Threshold)**<br>0x0: 0.125ms 0x2: 1.25ms 0x4: 6.25ms 0x6: 25ms<br>0x1: 0.25ms 0x3: 2.5ms 0x5: 12.5ms 0x7: 50ms |
| 1 | | R/W | 0 | |
| 0 | | R/W | 0 | |

## 表54. 动态范围控制(DRC)增益配置寄存器

| ADDRESS: 0x36 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | DRCG[4:0] | R/W | 0 | **PLAYBACK DRC Make-Up Gain Configuration**<br>0x0: +0dB 0x4: +4dB 0x8: +8dB 0xC: +12dB<br>0x1: +1dB 0x5: +5dB 0x9: +9dB 0xD: reserved<br>0x2: +2dB 0x6: +6dB 0xA: +10dB 0xE: reserved<br>0x3: +3dB 0x7: +7dB 0xB: +11dB 0xF: reserved |
| 3 | | | 0 | |
| 2 | | | 0 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

## 表55. 动态范围控制(DRC)压缩寄存器

| ADDRESS: 0x34 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | DRCCMP[2:0] | R/W | 0 | **PLAYBACK DRC Compression Ratio Configuration**<br>0x0: 1:1 0x3: 4:1<br>0x1: 1.5:1 0x4: INF:1<br>0x2: 2:1 0x5–0x7: Reserved |
| 6 | | | 0 | |
| 5 | | | 0 | |
| 4 | DRCTHC[4:0] | R/W | 0 | **PLAYBACK DRC Compression Threshold Configuration**<br>0x00: 0 0x08: -8dB 0x10: -16dB 0x18: -24dB<br>0x01: -1dB 0x09: -9dB 0x11: -17dB 0x19: -25dB<br>0x02: -2dB 0x0A: -10dB 0x12: -18dB 0x1A: -26dB<br>0x03: -3dB 0x0B: -11dB 0x13: -19dB 0x1B: -27dB<br>0x04: -4dB 0x0C: -12dB 0x14: -20dB 0x1C: -28dB<br>0x05: -5dB 0x0D: -13dB 0x15: -21dB 0x1D: -29dB<br>0x06: -6dB 0x0E: -14dB 0x16: -22dB 0x1E: -30dB<br>0x07: -7dB 0x0F: -15dB 0x17: -23dB 0x1F: -31dB |
| 3 | | | 0 | |
| 2 | | | 0 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

表56. 动态范围控制(DRC)扩展寄存器

| ADDRESS: 0x35 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | DRCEXP[2:0] | R/W | 0 | **PLAYBACK DRC Expansion Ratio Configuration**<br>0x0: 1:1 0x2: 1:3<br>0x1: 1:2 0x3–0x7: Reserved |
| 5 | | | 0 | |
| 4 | DRCTHE[4:0] | R/W | 0 | **PLAYBACK DRC Expansion Threshold Configuration**<br>0x00: -35dB 0x08: -43dB 0x10: -51dB 0x18: -59dB<br>0x01: -36dB 0x09: -44dB 0x11: -52dB 0x19: -60dB<br>0x02: -37dB 0x0A: -45dB 0x12: -53dB 0x1A: -61dB<br>0x03: -38dB 0x0B: -46dB 0x13: -54dB 0x1B: -62dB<br>0x04: -39dB 0x0C: -47dB 0x14: -55dB 0x1C: -63dB<br>0x05: -40dB 0x0D: -48dB 0x15: -56dB 0x1D: -64dB<br>0x06: -41dB 0x0E: -49dB 0x16: -57dB 0x1E: -65dB<br>0x07: -42dB 0x0F: -50dB 0x17: -58dB 0x1F: -66dB |
| 3 | | | 0 | |
| 2 | | | 0 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

**回放通路数字滤波器**

回放通路DSP包括数字滤波器。滤波电路配合MODE位设置(表57)，提供IIR语音滤波和FIR音乐滤波：IIR滤波器优化用于标准($f_S$ = 8kHz)和宽带($f_S$ = 16kHz)语音处理，FIR滤波器则优化用于降低高音频/音乐采样率下的功耗。采样率超过50kHz ($f_{LRCLK}$ > 50kHz)时，必须使用FIR音频滤波器，并将DHF置位，以正确设置FIR插值滤波器。所选MODE配置用于录音和回放DSP的两个通道。

回放DSP也具有隔直滤波器，该滤波器可与IIR语音及FIR音乐滤波器配合使用，阻止音频频段下限以内的低频(包括DC)输入信号。

## 数/模转换器(DAC)配置

立体声DAC架构包括两个独立的音频通路，模拟输出可连接至任意模拟输出混音器的模拟输出；具有两种工作模式(表4)：一种工作模式优化用于提高动态性能，另一种模式优化用于降低功耗。两路DAC可独立使能，允许器件支持立体声和左声道或右声道单声道配置(表8)。

## 表57. DSP滤波器配置寄存器

| ADDRESS: 0x26 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | MODE | R/W | 1 | **Enables the CODEC DSP FIR Music Filters (Default IIR Voice Filters)**<br>0: The codec DSP filters operate in IIR voice mode with stop band frequencies below the $f_S/2$ Nyquist rate. The voice mode filters are optimized for 8kHz or 16kHz voice application use.<br>1: The codec DSP filters operate in a linear phase FIR audio mode optimized to maintain stereo imaging and operate at higher $f_S$ rates while utilizing lower power. |
| 6 | AHPF | R/W | 0 | **Enables the Record Path DC Blocking Filter**<br>0: DC-blocking filter disabled.<br>1: DC-blocking filter enabled. |
| 5 | DHPF | R/W | 0 | **Enables the Playback Path DC Blocking Filter**<br>0: DC-blocking filter disabled.<br>1: DC-blocking filter enabled. |
| 4 | DHF | R/W | 0 | **Enables the DAC High Sample Rate Mode (LRCLK > 50kHz, FIR Only)**<br>0: LRCLK is less than 50kHz. 8x FIR interpolation filter used.<br>1: LRCLK is greater than 50kHz. 4x FIR interpolation filter used. |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | — | — | — | — |
| 0 | — | — | — | — |

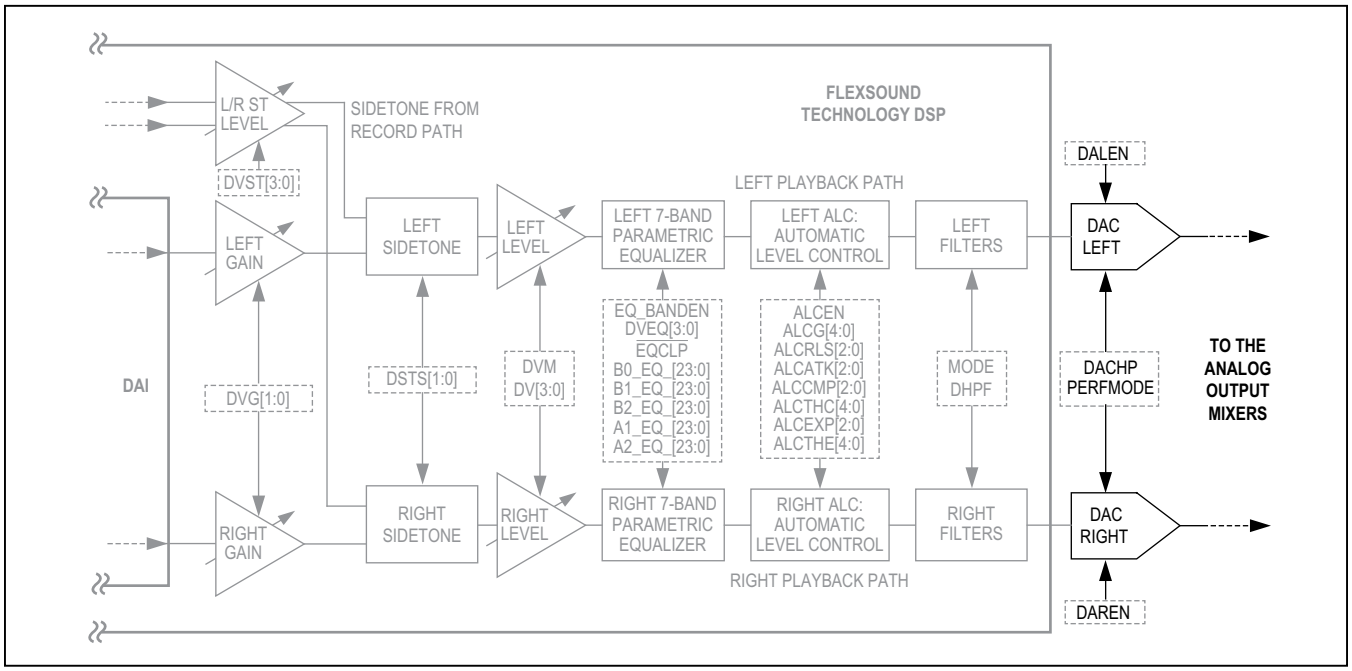



*图31. 回放通路数/模转换器*

## 模拟音频输出配置

器件具有三个独立的集成模拟音频输出驱动器(图32)：接收器/线出驱动器可配置为差分接收器/听筒输出或作为立体声单端线出驱动器；立体声扬声器输出驱动器为无滤波D类差分放大器，能够驱动4Ω和8Ω扬声器；耳机输出驱动器采用Maxim的DirectDrive架构，带有集成电荷泵，提供可配置的耳机和耳麦插孔检测。每个模拟音频输出驱动器都具有可编程增益输入混音器和输出放大器。每个混音器支持来自于回放DAC、模拟麦克风放大器和线入驱动器的信号组合。

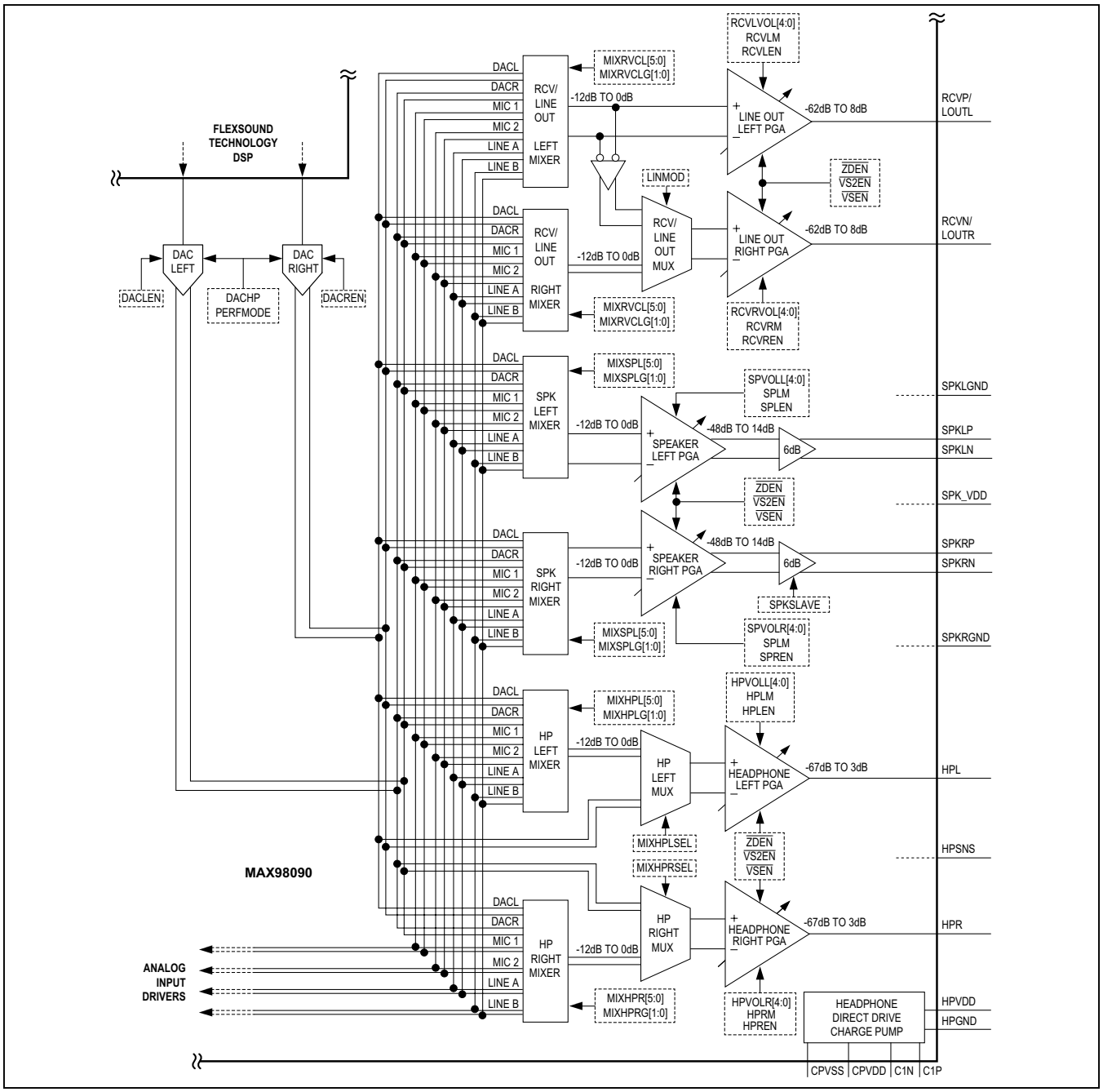



*图32. 模拟音频输出功能框图*

### 模拟AB类可配置接收器/线出

器件具有可配置的模拟AB类可编程增益放大器输出，可配置作为单声道差分输出或作为立体声单端输出。配置作为差分模拟输出(LINEMOD = 0，表61)时，驱动器是理想的接收器驱动器，能够驱动16Ω和32Ω差分负载(例如听筒扬声器)。接收器配置下，左声道接收器/线出混音器的单声道输出连接至桥接负载(BTL)配置的左/右声道输出驱动器(图33)。该配置下，混音器输入信号源及混音器、输出放大器增益设置由左声道寄存器决定。所有右声道输出寄存器设置在接收器/听筒模式下不受影响。

配置作为立体声单端模拟输出(LINEMOD = 1，表61)时，驱动器优化用作标准的以地为参考的高阻线出。线出配置下，左声道和右声道混音输出分别连接至各自的输出驱动器(图34)。该配置下，两个声道由左/右声道寄存器独立配置。

### 接收器/听筒混音器和增益控制

配置作为差分接收器输出时，只使用左声道输出配置寄存器。接收器混音器可配置为接收来自回放DAC、模拟麦克风放大器和线入驱动器的信号组合(表58)。接收器输入混音器也提供多种衰减选项(表59)，混音器衰减选项有-6dB、-9.5dB和-12dB，以防止选择多个满幅输入源时发生削波。

接收器输出为可编程增益放大器(PGA)，能够驱动宽范围差分负载(包括标准16Ω和32Ω听筒扬声器)。接收器PGA具有较宽的音量调节范围，从-62dB至+8dB，提供高衰减静音控制(表60)，具有可编程咔嗒/噼噗声抑制选项，详细信息请参考*咔嗒/噼噗声抑制*部分。接收器PGA输出共模电压为$V_{AVDD}$的一半(电阻分压器BIAS模式)或大约0.78V (带隙BIAS模式)。

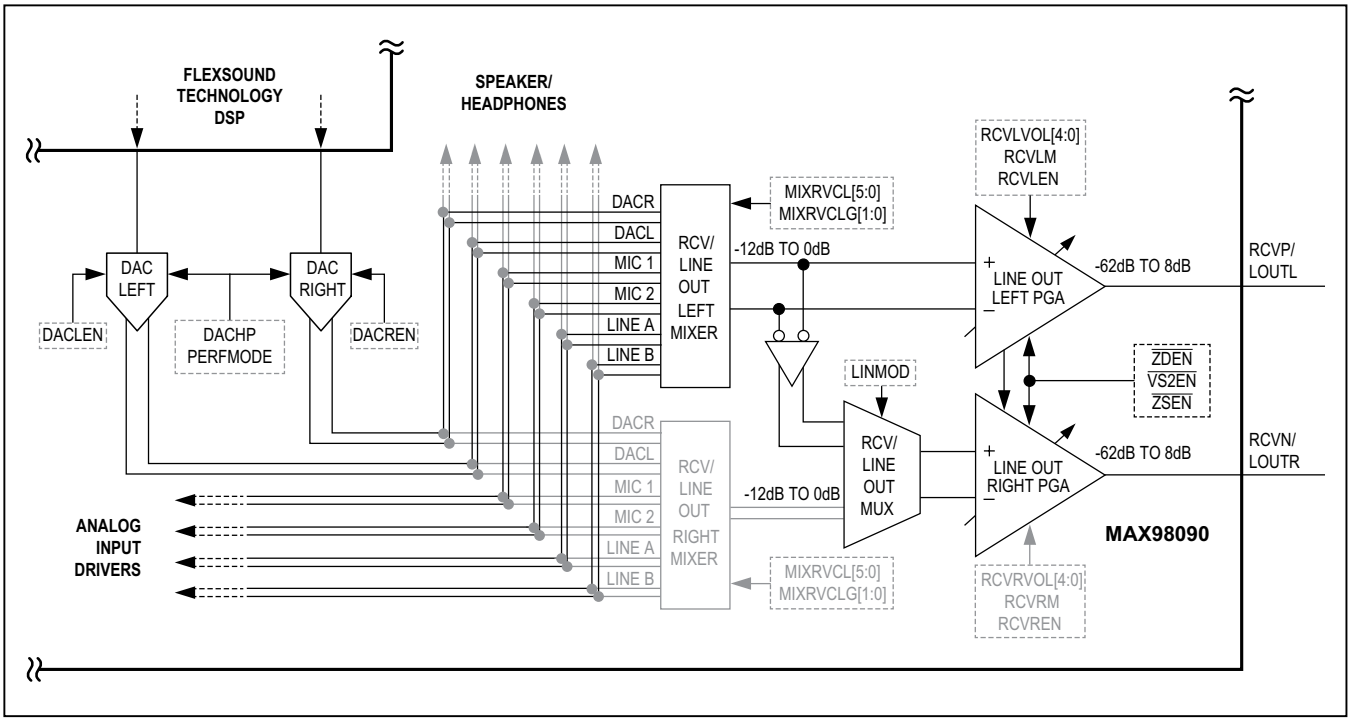



*图33. 接收器输出功能框图*

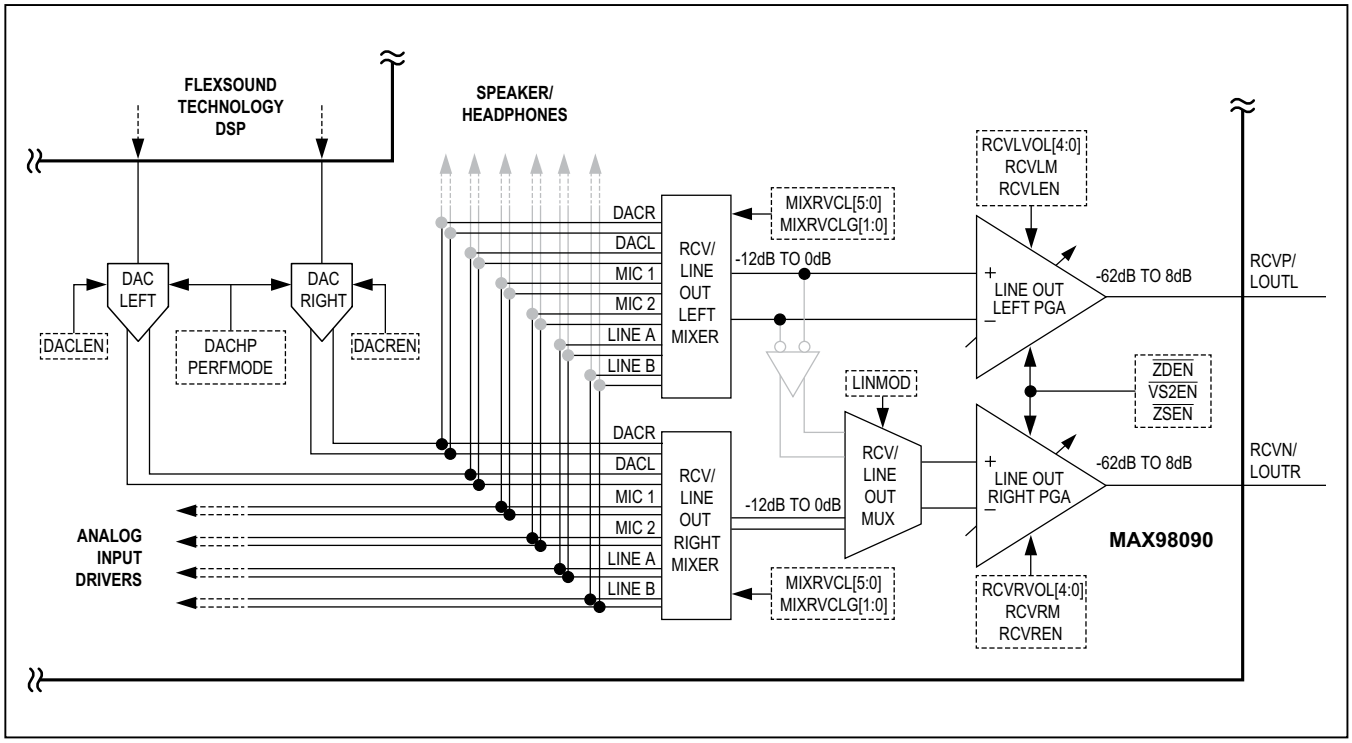



*图34. 立体声单端线出功能框图*

## 表58. 接收器和左声道线出混音器信号源配置寄存器

| ADDRESS: 0x37 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | MIXRCVL[5:0] | R/W | 0 | Selects MIC 2 as the input to the receiver/line out left mixer. |
| 4 | | | 0 | Selects MIC 1 as the input to the receiver/line out left mixer. |
| 3 | | | 0 | Selects line B as the input to the receiver/line out left mixer. |
| 2 | | | 0 | Selects line A as the input to the receiver/line out left mixer. |
| 1 | | | 0 | Selects DAC right as the input to the receiver/line out left mixer. |
| 0 | | | 0 | Selects DAC left as the input to the receiver/line out left mixer. |

### 线出混音器和增益控制

配置为立体声单端线出时，左声道和右声道配置寄存器可独立设置。每个声道混音器可配置为接收来自回放DAC、模拟麦克风放大器和线入驱动器的信号组合(表58和61)。输入混音器也提供多种衰减选项(表59和62)，混音器衰减选项有-6dB、-9.5dB和-12dB，以防止选择多个满幅输入源时发生削波。

左声道和右声道线出驱动器为独立可编程增益放大器(PGA)，能够驱动高阻、以地为参考的负载。线出PGA具有较宽的音量调节范围，从-62dB至+8dB，提供高衰减静音控制(表60和62)，具有可编程咔嗒/噼噗声抑制选项，详细信息请参见*咔嗒/噼噗声抑制*部分。输出共模电压为$V_{AVDD}$的一半(电阻分压器BIAS模式)或大约0.78V (带隙BIAS模式)。由于内部架构的原因，左声道和右声道各有-3dB的内置基线增益(全部可编程增益选项设置为0dB时)。

## 表59. 接收器和左声道线出混音器增益控制寄存器

| ADDRESS: 0x38 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | MIXRCVLG[1:0] | R/W | 0 | **Receiver/Line Output Left Mixer Gain Configuration**<br>00: 0dB 10: -9.5dB<br>01: -6dB 11: -12dB |
| 0 | | | 0 | |

## 表60. 接收器和左声道线出音量控制寄存器

| ADDRESS: 0x39 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | RCVLM | R/W | 0 | **Left Receiver/Line Output Mute**<br>0: Left output amplifier not muted.<br>1: Left output amplifier is muted. |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | RCVLVOL[4:0] | R/W | 1 | **Receiver/Line Output Left PGA Volume Configuration**<br>0x1F: +8dB 0x17: +2dB 0x0F: -12dB 0x07: -35dB<br>0x1E: +7.5dB 0x16: +1dB 0x0E: -14dB 0x06: -38dB<br>0x1D: +7dB 0x15: +0dB 0x0D: -17dB 0x05: -42dB<br>0x1C: +6.5dB 0x14: -2dB 0x0C: -20dB 0x04: -46dB<br>0x1B: +6dB 0x13: -4dB 0x0B: -23dB 0x03: -50dB<br>0x1A: +5dB 0x12: -6dB 0x0A: -26dB 0x02: -54dB<br>0x19: +4dB 0x11: -8dB 0x09: -29dB 0x01: -58dB<br>0x18: +3dB 0x10: -10dB 0x08: -32dB 0x00: -62dB |
| 3 | | | 0 | |
| 2 | | | 1 | |
| 1 | | | 0 | |
| 0 | | | 1 | |

## 表61. 右声道线出混音器信号源配置寄存器

| ADDRESS: 0x3A | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | LINMOD | R/W | 0 | **Selects Between Receiver BTL Mode and Line Output mode**<br>0: Receiver BTL mode. All control of the output is from the left-channel registers.<br>1: Line Output mode. Left and right channels are programmed independently. |
| 6 | — | — | — | — |
| 5 | MIXRCVR[5:0] | R/W | 0 | Selects MIC 2 as the input to the line out right mixer |
| 4 | | | 0 | Selects MIC 1 as the input to the line out right mixer |
| 3 | | | 0 | Selects Line B as the input to the line out right mixer |
| 2 | | | 0 | Selects Line A as the input to the line out right mixer |
| 1 | | | 0 | Selects DAC Right as the input to the line out right mixer |
| 0 | | | 0 | Selects DAC Left as the input to the line out right mixer |

## 表62. 右声道线出混音器增益控制寄存器

| ADDRESS: 0x3B | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | MIXRCVRG[1:0] | R/W | 0 | **Line Output Right Mixer Gain Configuration**<br>00: 0dB 10: -9.5dB<br>01: -6dB 11: -12dB |
| 0 | | | 0 | |

## 表63. 右声道线出音量控制寄存器

| ADDRESS: 0x3C | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | RCVRM | R/W | 0 | **Right Receiver/Line Output Mute**<br>0: Right output amplifier not muted.<br>1: Right output amplifier is muted. |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | RCVRVOL[4:0] | R/W | 1 | **Line Output Right PGA Volume Configuration**<br>0x1F: +8dB 0x17: +2dB 0x0F: -12dB 0x07: -35dB<br>0x1E: +7.5dB 0x16: +1dB 0x0E: -14dB 0x06: -38dB<br>0x1D: +7dB 0x15: +0dB 0x0D: -17dB 0x05: -42dB<br>0x1C: +6.5dB 0x14: -2dB 0x0C: -20dB 0x04: -46dB<br>0x1B: +6dB 0x13: -4dB 0x0B: -23dB 0x03: -50dB<br>0x1A: +5dB 0x12: -6dB 0x0A: -26dB 0x02: -54dB<br>0x19: +4dB 0x11: -8dB 0x09: -29dB 0x01: -58dB<br>0x18: +3dB 0x10: -10dB 0x08: -32dB 0x00: -62dB |
| 3 | | | 0 | |
| 2 | | | 1 | |
| 1 | | | 0 | |
| 0 | | | 1 | |

## 模拟D类扬声器输出

器件具有集成立体声差分扬声器放大器。模拟立体声扬声器输出由三部分组成，包括灵活的输入混音器、可编程增益放大器和差分D类输出驱动器(图35)。扬声器输出能够驱动4Ω和8Ω负载，采用高效率D类架构，满足EMI辐射标准，驱动无滤波扬声器负载。

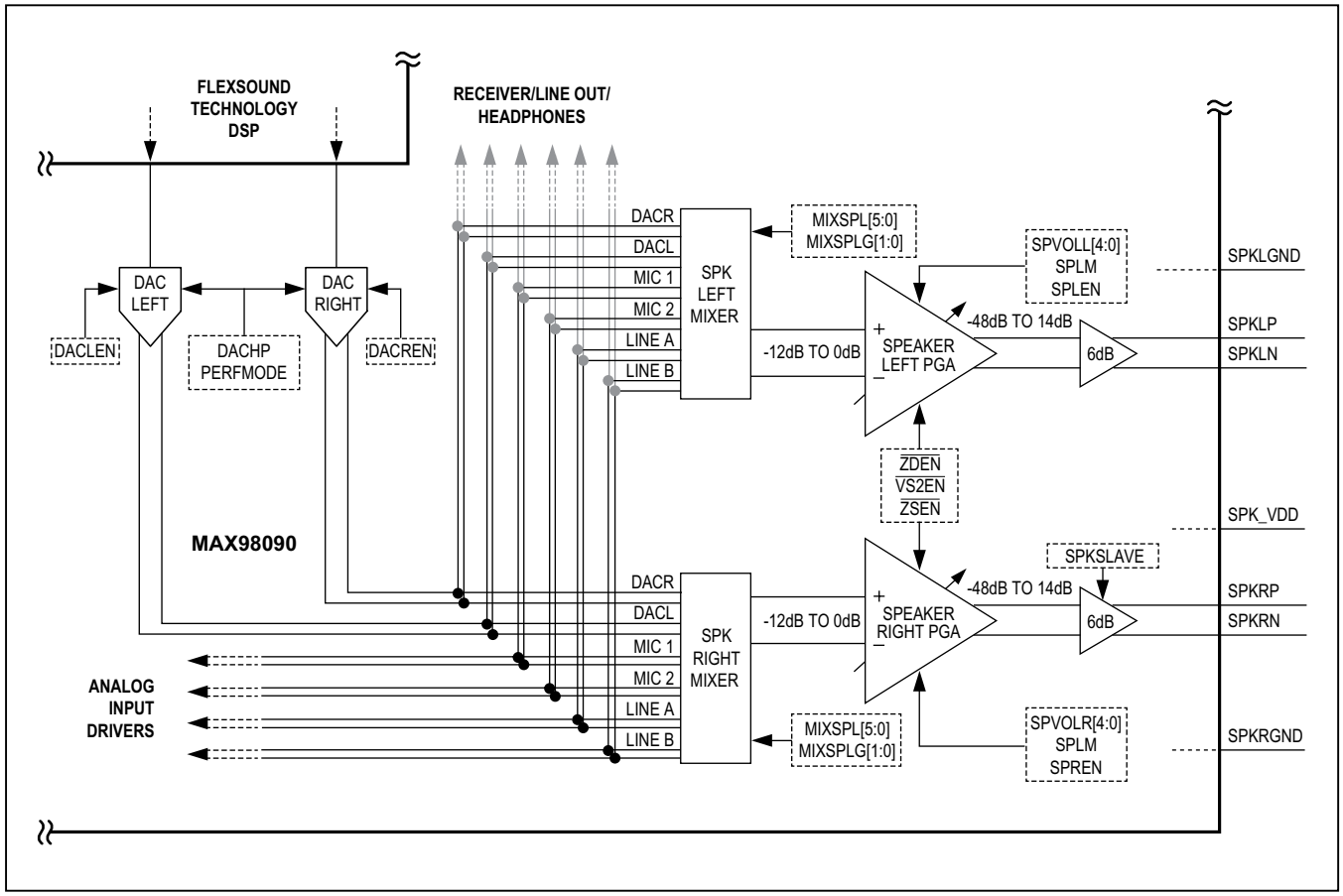



*图35. D类扬声器输出功能框图*

### 扬声器输出混音器和增益控制

扬声器混音器可配置为接收来自回放DAC、模拟麦克风放大器和线入驱动器的信号组合(表64和65)。输入混音器也提供多种衰减选项(表66)，混音器衰减选项有-6dB、-9.5dB和-12dB，以防止选择多个满幅输入源时发生削波。

## 表64. 左声道扬声器混音器配置寄存器

| ADDRESS: 0x2E | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | MIXSPL[5:0] | R/W | 0 | Selects microphone input 2 to left speaker mixer |
| 4 | | | 0 | Selects microphone Input 1 to left speaker mixer |
| 3 | | | 0 | Selects line input B to left speaker mixer |
| 2 | | | 0 | Selects line input A to left speaker mixer |
| 1 | | | 0 | Selects right DAC output to left speaker mixer |
| 0 | | | 0 | Selects left DAC output to left speaker mixer |

## 表65. 右声道扬声器混音器配置寄存器

| ADDRESS: 0x2F | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | SPK_SLAVE | — | — | **Speaker Slave Mode Enable**<br>0: Right-channel clock always generated independently.<br>1: Right channel uses left-channel clock if both channels are enabled. |
| 5 | MIXSPR[5:0] | R/W | 0 | Selects microphone input 2 to right speaker mixer. |
| 4 | | | 0 | Selects microphone input 1 to right speaker mixer. |
| 3 | | | 0 | Selects line input B to Right speaker mixer. |
| 2 | | | 0 | Selects line input A to right speaker mixer. |
| 1 | | | 0 | Selects right DAC output to right speaker mixer. |
| 0 | | | 0 | Selects left DAC output to right speaker mixer. |

## 表66. 扬声器混音器增益控制寄存器

| ADDRESS: 0x30 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | MIXSPRG[1:0] | R/W | 0 | **Right-Speaker Mixer Gain Configuration**<br>00: +0dB 10: -9.5dB<br>01: -6dB 11: -12dB |
| 2 | | | 0 | |
| 1 | MIXSPLG[1:0] | R/W | 0 | **Left-Speaker Mixer Gain Configuration**<br>00: +0dB 10: -9.5dB<br>01: -6dB 11: -12dB |
| 0 | | | 0 | |

扬声器输出可编程增益放大器(PGA)具有较宽的音量调节范围，从-48dB至+14dB，提供高衰减静音控制(表67和表68)，具有可编程咔嗒/噼噗声抑制选项。详细信息请参见*咔嗒/噼噗声抑制*部分。除可编程增益范围外，D类输出驱动器也提供另外6dB的内置增益。

## 表67. 左声道扬声器放大器音量控制寄存器

| ADDRESS: 0x31 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | SPLM | R/W | 0 | **Left Speaker Output Mute Enable**<br>0 : Speaker output volume set by the volume control bits.<br>1 : Left speaker output muted. |
| 6 | — | — | — | — |
| 5 | SPVOLL[5:0] | R/W | 1 | **Left Speaker Output Amplifier Volume Control Configuration** |
| 4 | | | 0 | 0x3F: +14dB　0x35: +9dB　0x2B: -1dB　0x21: -17dB<br>0x3E: +13.5dB　0x34: +8dB　0x2A: -2dB　0x20: -20dB<br>0x3D: +13dB　0x33: +7dB　0x29: -3dB　0x1F: -23dB<br>0x3C: +12.5dB　0x32: +6dB　0x28: -4dB　0x1E: -26dB<br>0x3B: +12dB　0x31: +5dB　0x27: -5dB　0x1D: -29dB<br>0x3A: +11.5dB　0x30: +4dB　0x26: -6dB　0x1C: -32dB<br>0x39: +11dB　0x2F: +3dB　0x25: -8dB　0x1B: -36dB<br>0x38: +10.5dB　0x2E: +2dB　0x24: -10dB　0x1A: -40dB<br>0x37: +10dB　0x2D: +1dB　0x23: -12dB　0x19: -44dB<br>0x36: +9.5dB　0x2C: +0dB　0x22: -14dB　0x18: -48dB |
| 3 | | | 1 | |
| 2 | | | 1 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

## 表68. 右声道扬声器放大器音量控制寄存器

| ADDRESS: 0x32 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | SPRM | R/W | 0 | **Right Speaker Output Mute Enable**<br>0 : Speaker output volume set by the volume control bits.<br>1 : Right-speaker output muted. |
| 6 | — | — | — | — |
| 5 | SPVOLR[5:0] | R/W | 1 | **Right Speaker Output Amplifier Volume Control Configuration** |
| 4 | | | 0 | 0x3F: +14dB　0x35: +9dB　0x2B: -1dB　0x21: -17dB<br>0x3E: +13.5dB　0x34: +8dB　0x2A: -2dB　0x20: -20dB<br>0x3D: +13dB　0x33: +7dB　0x29: -3dB　0x1F: -23dB<br>0x3C: +12.5dB　0x32: +6dB　0x28: -4dB　0x1E: -26dB<br>0x3B: +12dB　0x31: +5dB　0x27: -5dB　0x1D: -29dB<br>0x3A: +11.5dB　0x30: +4dB　0x26: -6dB　0x1C: -32dB<br>0x39: +11dB　0x2F: +3dB　0x25: -8dB　0x1B: -36dB<br>0x38: +10.5dB　0x2E: +2dB　0x24: -10dB　0x1A: -40dB<br>0x37: +10dB　0x2D: +1dB　0x23: -12dB　0x19: -44dB<br>0x36: +9.5dB　0x2C: +0dB　0x22: -14dB　0x18: -48dB |
| 3 | | | 1 | |
| 2 | | | 1 | |
| 1 | | | 0 | |
| 0 | | | 0 | |

### 高效率D类扬声器驱动器

D类放大器的效率比AB类放大器高得多，高效率得益于输出级晶体管的开关工作模式。D类放大器中，输出晶体管作为电流驱动开关，所消耗的功率可忽略不计。与D类放大器输出级相关的功率损耗主要源于MOSFET导通电阻的损耗和静态电流损耗。

为便于比较，线性放大器的理论最高效率为78%；但它只有在峰值输出功率条件下才能达到这一效率，常规工作水平(典型的音乐再现水平)下，效率往往低于30%。相同条件下，差分D类扬声器输出放大器仍可保持80%的效率。

默认设置下，为左声道和右声道分别产生D类输出开关时钟。使能从机模式时，右声道称为左声道的从机，使用相同时钟(表65)。从机模式下，开关同步。所以，从机工作模式避免了异步立体声D类开关中常见的差拍效应。

D类放大器往往要求使用外部LC滤波和/或屏蔽，以满足EN55022B和FCC电磁干扰(EMI)规范要求。Maxim拥有专利的有源辐射抑制、摆率控制电路降低了EMI辐射，允许器件驱动4Ω和8Ω负载，无需任何附加输出滤波。无滤波D类输出设计用于扬声器走线长度较短、串联电阻较低的典型应用。关于应用的详细信息，请参见*无滤波D类扬声器工作*部分。

### 模拟H类耳机输出

立体声耳机输出驱动器具有灵活的输入混音器、可编程增益级、集成电荷泵，以及以地为参考的DirectDrive H类放大器(图36)。耳机输出放大器能够驱动16Ω和32Ω以地为参考的耳机负载。

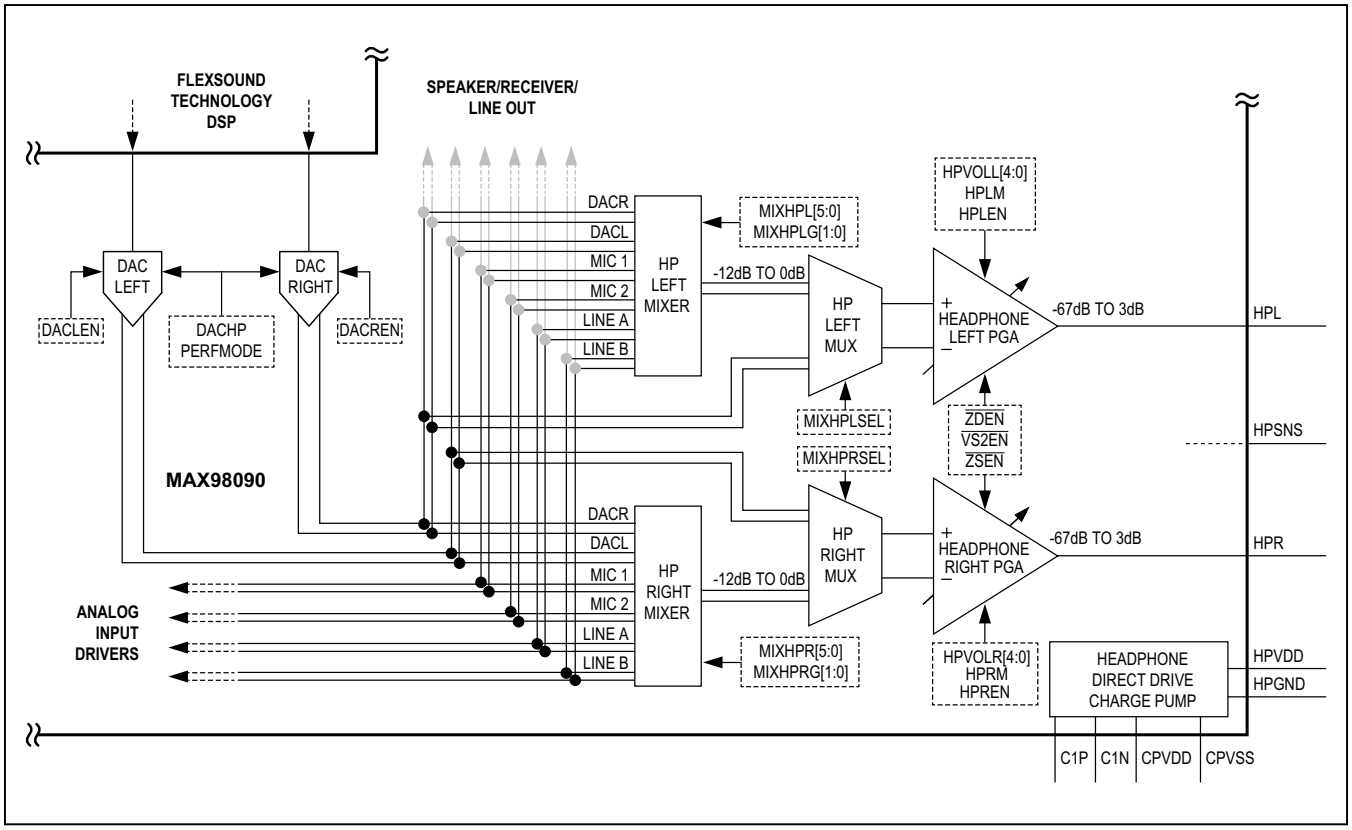



*图36. DirectDrive耳机输出功能框图*

### 耳机输出混音器和增益控制

耳机混音器可配置为接收来自回放DAC、模拟麦克风放大器和线入驱动器的信号组合(表69和表70)。输入混音器也提供多种衰减选项(表71)，混音器衰减选项有-6dB、-9.5dB和-12dB，避免选择多个输入源时发生削波。

## 表69. 左声道耳机混音器配置寄存器

| ADDRESS: 0x29 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | MIXHPL[5:0] | R/W | 0 | Selects microphone input 2 to left headphone mixer. |
| 4 | | | 0 | Selects microphone input 1 to left headphone mixer. |
| 3 | | | 0 | Selects line input B to left headphone mixer. |
| 2 | | | 0 | Selects line input A to left headphone mixer. |
| 1 | | | 0 | Selects right DAC output to left headphone mixer. |
| 0 | | | 0 | Selects left DAC output to left headphone mixer. |

## 表70. 右声道耳机混音器配置寄存器

| ADDRESS: 0x2A | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | MIXHPR[5:0] | R/W | 0 | Selects microphone input 2 to right headphone mixer. |
| 4 | | | 0 | Selects microphone input 1 to right headphone mixer. |
| 3 | | | 0 | Selects line input B to right headphone mixer. |
| 2 | | | 0 | Selects line input A to right headphone mixer. |
| 1 | | | 0 | Selects right DAC output to right headphone mixer. |
| 0 | | | 0 | Selects left DAC output to right headphone mixer. |

## 表71. 耳机混音器控制和增益寄存器

| ADDRESS: 0x2B | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | MIXHPRSEL | R/W | 0 | **Select Headphone Mixer as Right Input Source (Default DAC Right Direct)**<br>0: DAC only source (best dynamic range and power consumption)<br>1: Headphone mixer source |
| 4 | MIXHPLSEL | R/W | 0 | **Select Headphone Mixer as Left Input Source (Default DAC Left Direct)**<br>0: DAC only source (best dynamic range and power consumption)<br>1: Headphone mixer source |
| 3 | MIXHPRG[1:0] | R/W | 0 | **Right-Headphone Mixer Gain Configuration**<br>00: +0dB 10: -9.5dB<br>01: -6dB 11: -12dB |
| 2 | | | 0 | |
| 1 | MIXHPLG[1:0] | R/W | 0 | **Left-Headphone Mixer Gain Configuration**<br>00: +0dB 10: -9.5dB<br>01: -6dB 11: -12dB |
| 0 | | | 0 | |

此外，耳机输出具有低功耗直接DAC回放模式(图37)。这种配置下，来自回放通路的立体声DAC输出在耳机混音器附近直接连接到耳机输出放大器。与低功耗耳机回放模式配合使用时(表4)，该组合是功耗最低的数/模回放配置。

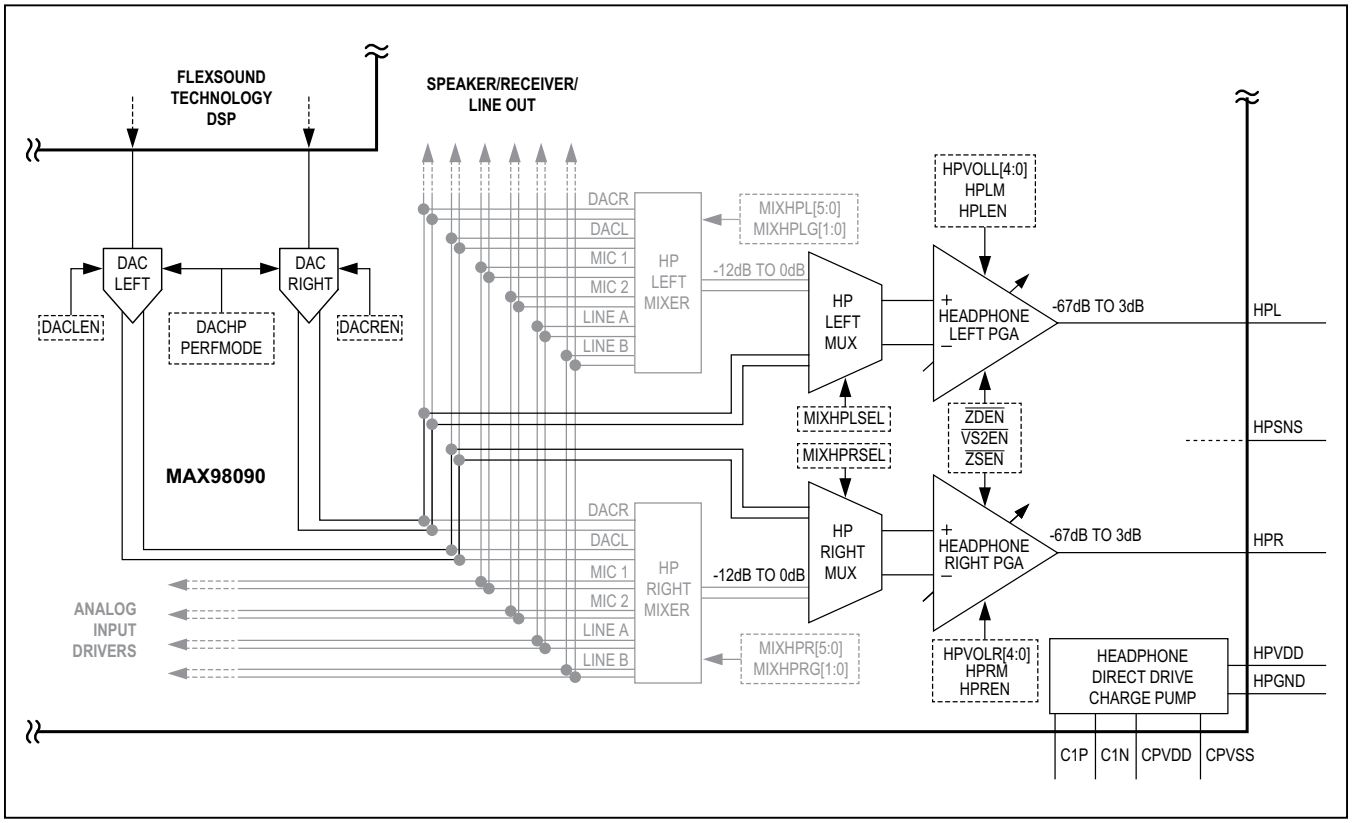



*图37. 降低功耗的DAC回放至耳机输出配置*

耳机输出可编程增益放大器(PGA)具有较宽的音量调节范围，从-67dB至+3dB，提供高衰减静音控制(表72和表73)，具有可编程咔嗒/噼噗声抑制选项，详细信息参见*咔嗒/噼噗声抑制*部分。

## 表72. 左声道耳机放大器音量控制寄存器

| ADDRESS: 0x2C | | | | DESCRIPTION |
|---|---|---|---|---|
| **BIT** | **NAME** | **TYPE** | **POR** | |
| 7 | HPLM | R/W | 0 | **Left Headphone Output Mute Enable**<br>0 : Headphone output volume set by the volume control bits.<br>1 : Headphone output muted. |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | HPVOLL[4:0] | R/W | 1 | **Left Headphone Output Amplifier Volume Control Configuration**<br>0x1F: +3dB 0x17: -3dB 0x0F: -17dB 0x07: -40dB<br>0x1E: +2.5dB 0x16: -4dB 0x0E: -19dB 0x06: -43dB<br>0x1D: +2dB 0x15: -5dB 0x0D: -22dB 0x06: -47dB<br>0x1C: +1.5dB 0x14: -7dB 0x0C: -25dB 0x04: -51dB<br>0x1B: +1dB 0x13: -9dB 0x0B: -28dB 0x03: -55dB<br>0x1A: +0dB 0x12: -11dB 0x0A: -31dB 0x02: -59dB<br>0x19: -1dB 0x11: -13dB 0x09: -34dB 0x01: -63dB<br>0x18: -2dB 0x10: -15d 0x08: -37dB 0x00: -67dB |
| 3 | | | 1 | |
| 2 | | | 0 | |
| 1 | | | 1 | |
| 0 | | | 0 | |

## 表73. 右声道耳机放大器音量控制寄存器

| ADDRESS: 0x2D | | | | DESCRIPTION |
|---|---|---|---|---|
| **BIT** | **NAME** | **TYPE** | **POR** | |
| 7 | HPRM | R/W | 0 | **Right Headphone Output Mute Enable**<br>0 : Headphone output volume set by the volume control bits.<br>1 : Headphone output muted. |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | HPVOLR[4:0] | R/W | 1 | **Right Headphone Output Amplifier Volume Control Configuration**<br>0x1F: +3dB 0x17: -3dB 0x0F: -17dB 0x07: -40dB<br>0x1E: +2.5dB 0x16: -4dB 0x0E: -19dB 0x06: -43dB<br>0x1D: +2dB 0x15: -5dB 0x0D: -22dB 0x06: -47dB<br>0x1C: +1.5dB 0x14: -7dB 0x0C: -25dB 0x04: -51dB<br>0x1B: +1dB 0x13: -9dB 0x0B: -28dB 0x03: -55dB<br>0x1A: +0dB 0x12: -11dB 0x0A: -31dB 0x02: -59dB<br>0x19: -1dB 0x11: -13dB 0x09: -34dB 0x01: -63dB<br>0x18: -2dB 0x10: -15dB 0x08: -37dB 0x00: -67dB |
| 3 | | | 1 | |
| 2 | | | 0 | |
| 1 | | | 1 | |
| 0 | | | 0 | |

### 耳机地检测

为提高通道隔离，器件具有低边耳机检测(HPSNS)，检测耳机负载的地回路。为优化性能，通过隔离线将麦克风检测连接至尽量靠近耳机插孔地的某个点(图38)。如果无法实现以上条件，或者不使用麦克风检测，将其连接至模拟接地区域；这种配置下，通道隔离会受到影响，造成通道间串扰增大。

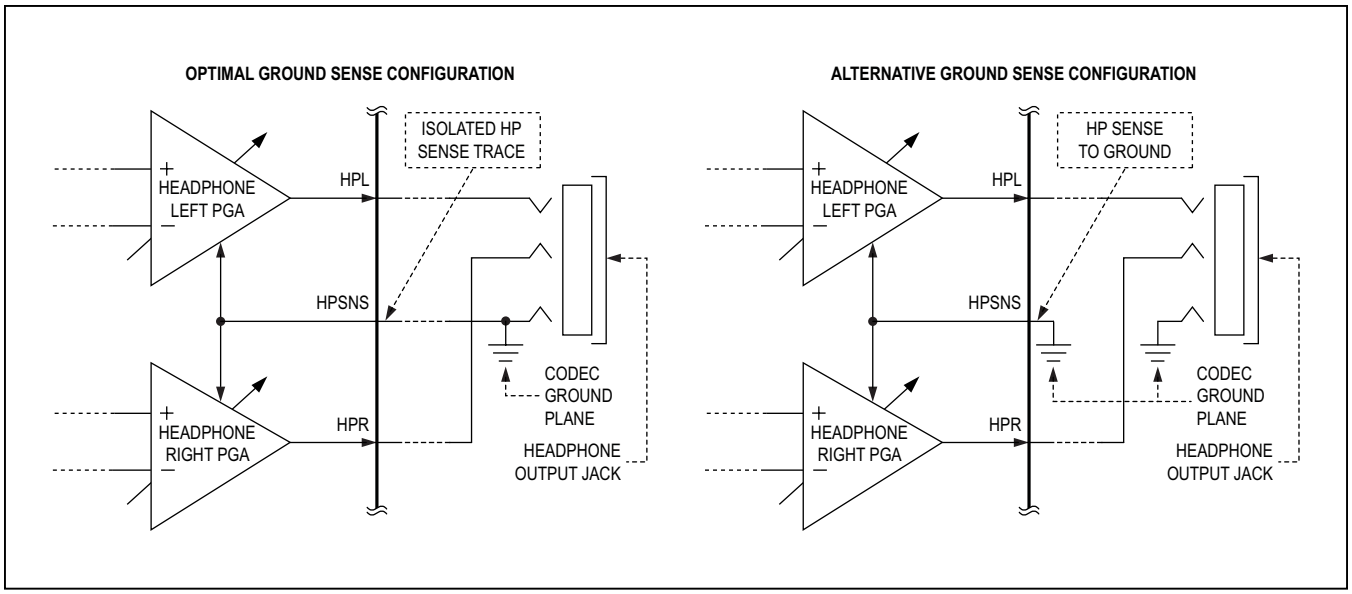



*图38.耳机输出地检测连接*

### DirectDrive耳机输出放大器

传统的单电源耳机放大器输出偏置在标称直流电压(通常为高边电源的一半，或者为带隙基准共模电平)，所以需要较大的耦合电容，以阻塞直流偏置，将音频输入交流耦合到耳机负载。如果没有这些电容，较大的直流电流将通过以地为参考的耳机负载，结果造成不必要的功耗，并且可能损坏耳机负载和放大器。

Maxim的第二代DirectDrive架构采用电荷泵产生内部负电源，从根本上解决了这一问题；增大了总体输出信号摆幅，同时即使工作在单电源也允许耳机输出偏置在GND (图39)。由于没有直流偏置分量，省去了大尺寸交流耦合电容。与需要两个大电容(典型值为220µF)的传统设计相比，电荷泵只需要三个小尺寸陶瓷电容，从而节省电路板空间、降低成本，并改善耳机放大器的频率响应。

### H类放大器电荷泵

H类放大器的输出架构与AB类放大器相同，但H类放大器的电源受输出信号控制。集成耳机电荷泵产生正、负电源，为耳机输出放大器供电。为提高效率，电荷泵的开关频率和输出电压及格式均根据耳机输出信号电平变化。

电荷泵具有三种不同的工作范围，每个范围具有不同的开关频率。两种功率较低的范围利用三电平开关方法产生$\pm V_{HPVDD}/2$的半幅电源轨，大功率范围使用标准的两电平开关方法产生满幅电源轨$\pm V_{HPVDD}$。每个范围的开关频率和电压都经过优化，既能保持高效率，又能满足不同的输出功率要求(表74)。

## 表74. 电荷泵工作范围

| RANGE | HEADPHONE OUTPUT LEVEL (% of $V_{HPVDD}$) | CHARGE PUMP CONFIGURATION | | |
|---|---|---|---|---|
| | | FREQUENCY (kHz) | $V_{CPVDD/CPVSS}$ | WAVEFORM |
| 1 | < 10 | ~82 | $\pm V_{HPVDD}/2$ | Range 1 |
| 2 | 10 to 25 | ~660 | $\pm V_{HPVDD}/2$ | Range 2 |
| 3 | > 25 | ~500 | $\pm V_{HPVDD}$ | Range 3 |

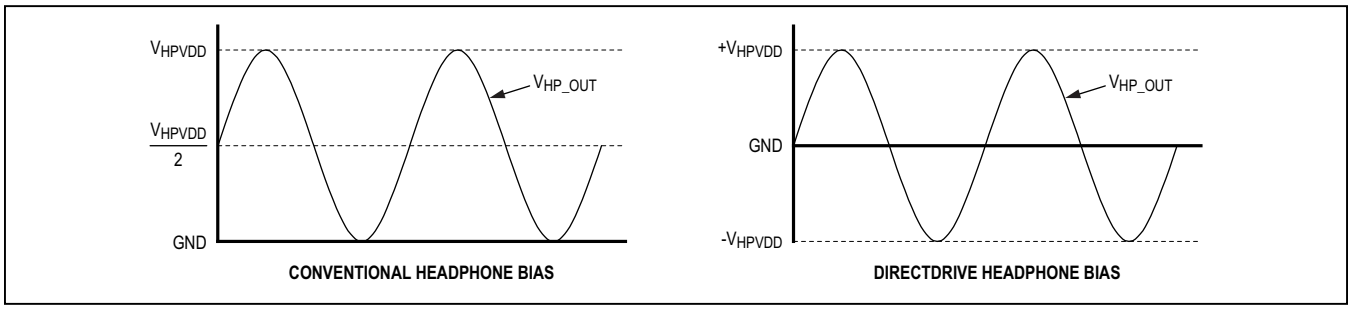



*图39. 传统耳机与DirectDrive耳机输出偏置的比较*

**范围1 ($V_{HP\_OUT}$ < 10% $V_{HPVDD}$)：**输出信号电平小于HPVDD的10%时，输出信号摆幅较低；相对于电荷泵静态功耗和开关损耗，驱动耳机负载的功耗较低。所以，为降低开关损耗，电荷泵频率降至最低(约82kHz)，双极性输出电源轨设置为HPVDD的一半或±$V_{HPVDD}$/2 (图40，范围1)。

**范围2 (10% $V_{HPVDD}$ ≤ $V_{HP\_OUT}$ < 25% $V_{HPVDD}$)：**输出信号电平介于10%和25% HPVDD之间时，输出信号摆幅仍低于HPVDD的一半。然而，此时的负载功耗要求比电荷泵的静态功耗和开关损耗高得多。为满足增大的负载功率要求，电荷泵开关频率增大(约660kHz)，而双极性输出电源轨保持为HPVDD的一半或±$V_{HPVDD}$/2 (图40，范围2)。

**范围3 (25% $V_{HPVDD}$ ≤ $V_{HP\_OUT}$)：**输出信号电平超过25% HPVDD时，输出信号摆幅大得多。所以，此时电荷泵产生双极性满幅HPVDD输出电源轨(±$V_{HPVDD}$)。该范围下的开关频率略低(约500kHz)。然而，增加的电压差允许耳机输出驱动器达到其最大电压摆幅和负载驱动能力(图40，范围3)。

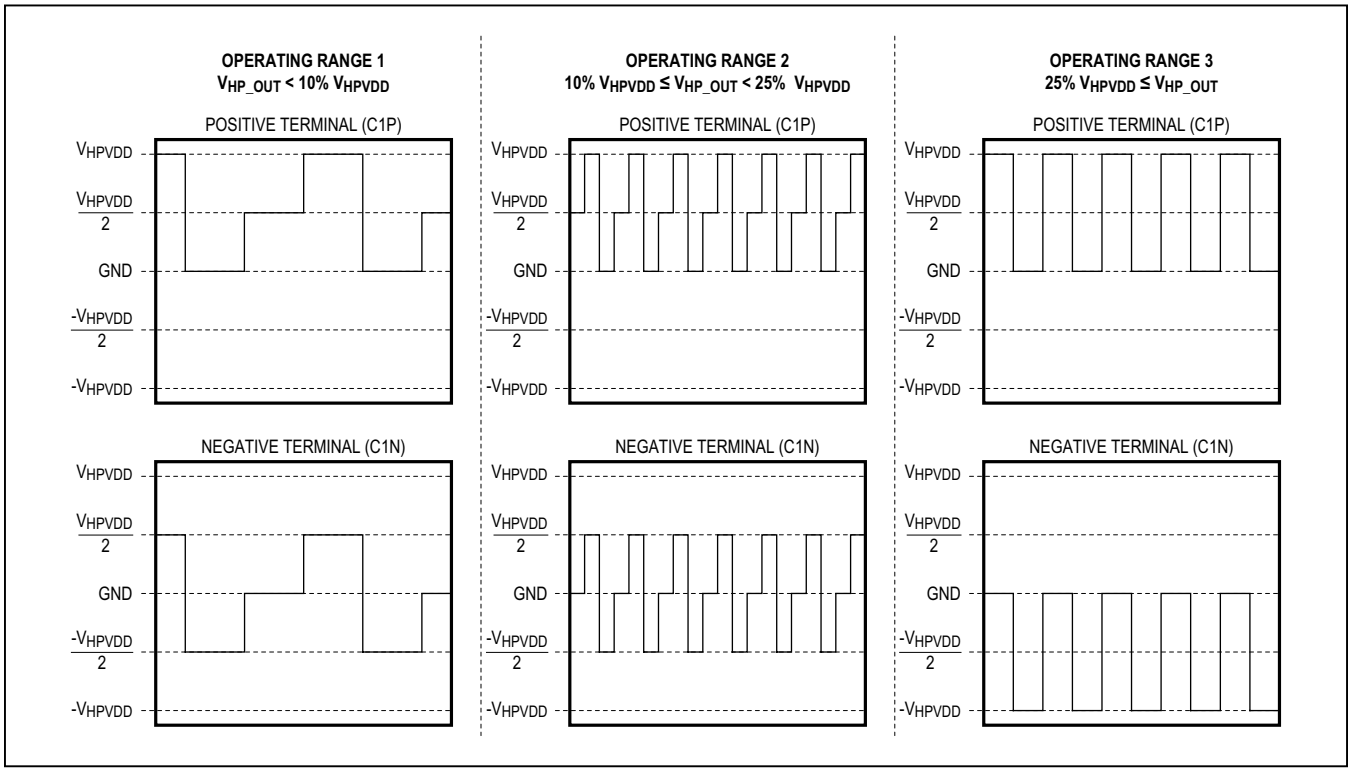



*图40. H类放大器电荷泵工作范围*

为防止音频串扰，全部三种电荷泵范围下的开关频率正好超出音频带宽。此外，为防止供电范围变化期间的音频失真，电荷泵非常快地从一个输出电源范围跳变至另一个范围。从半幅电源范围($\pm V_{HPVDD}/2$)改变为满幅电源范围($\pm V_{HPVDD}/2$)时，如果超过门限，则立即发生跳变(避免音频输出快速升高产生削波)；向下变化时，门限检测和供电范围跳变之间有32ms的延迟。快速供电电平跳变从HPVDD吸入显著的瞬态电流。为防止HPVDD电压下垂/尖峰脉冲，必须使用正确的旁路电容，以提供必需的瞬态电流(图53和54)。

### 咔嗒/噼噗声抑制

器件具有全面的咔嗒/噼噗声抑制电路，使得开启、关断及音量变化时的咔嗒/噼噗声降至最小。这些功能包括：过零检测、音量平滑变化、音量阶跃变化(表75)。

在模拟麦克风输入PGA和全部模拟输出PGA及音量控制电路采用过零检测，防止音量变化时产生较大的尖峰脉冲。器件在音频信号穿过中心点时改变音量，而不是收到指令时立即改变音量(图)。如果在超时窗口(100ms)内未发生过零，则改变音量，不考虑信号电平。

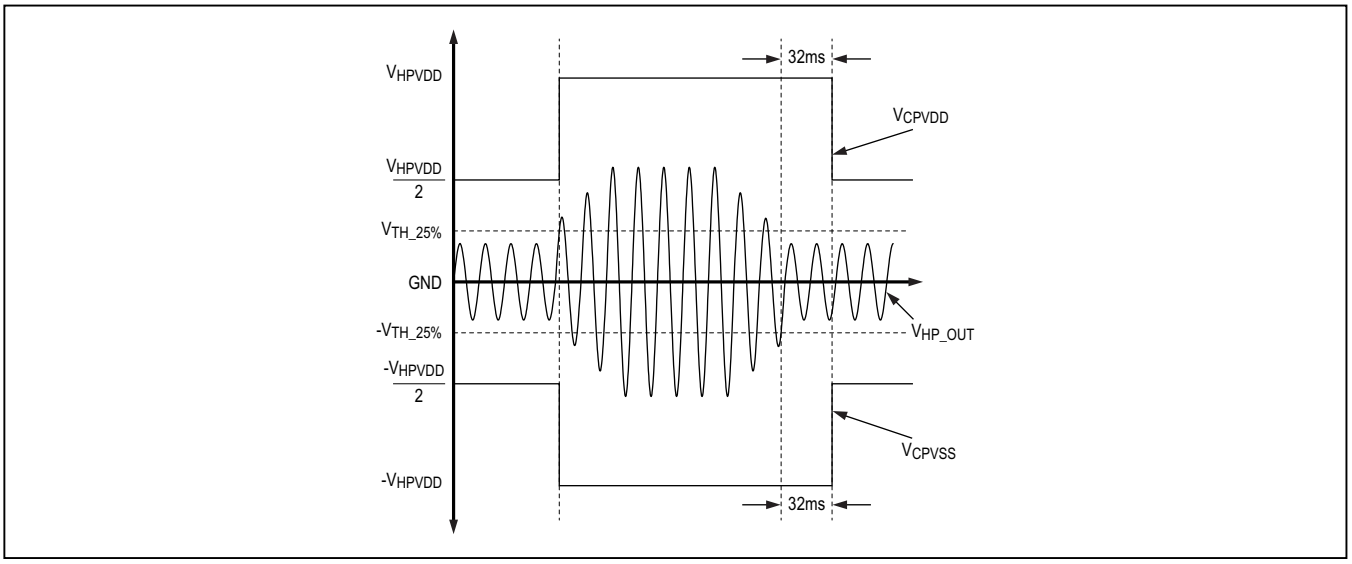



*图41. H类放大器供电范围跳变*

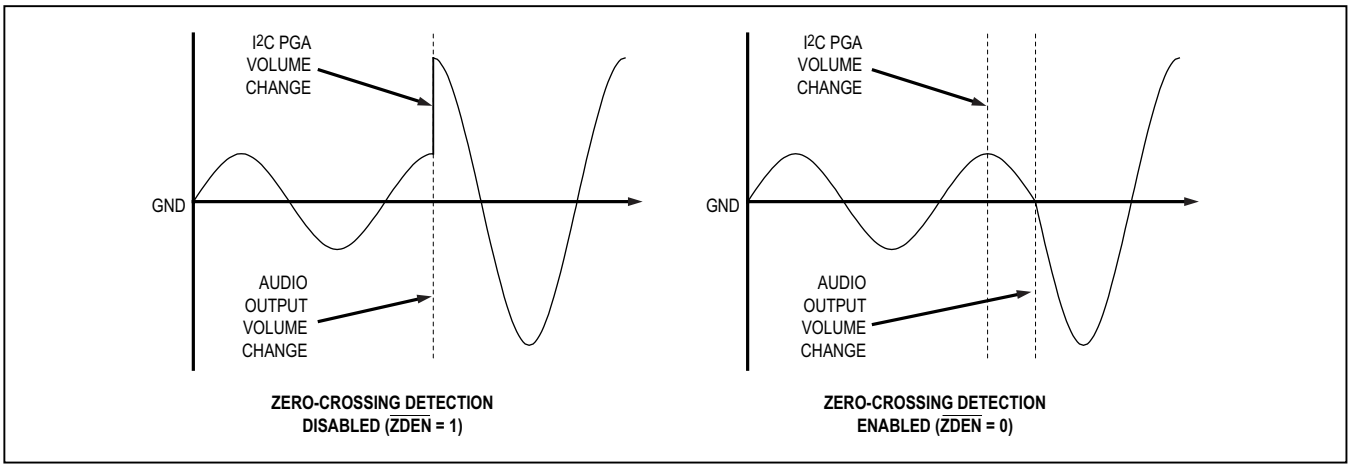



*图42. 过零检测*

表75. 过零检测和音量平滑配置寄存器

| ADDRESS: 0x40 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | $\overline{\text{ZDEN}}$ | R/W | 0 | **Zero-Crossing Detection**<br>0: Volume changes made only at zero crossings or after approximately 100ms.<br>1: Volume changes made immediately upon request. |
| 1 | $\overline{\text{VS2EN}}$ | R/W | 0 | **Enhanced Volume Smoothing**<br>Only valid is volume adjustment smoothing is enabled ($\overline{\text{VSEN}}$ = 0).<br>0: Each volume change waits until the previous volume step has been applied to the output. Allows volume smoothing to function with zero-crossing timeout.<br>1: Volume smoothing enhancement is disabled. |
| 0 | $\overline{\text{VSEN}}$ | R/W | 0 | **Volume Adjustment Smoothing**<br>0: Volume changes are smoothed by stepping through intermediate levels.<br>1: Volume changes are made directly in a single step. |

全部模拟输出PGA均可使用音量平滑。使能时，音量变化均分到最小步长，然后,音量从初始状态到最终音量设置逐步缓变，变化速率每ms一个步长。在器件开启和关断时同样进行音量平滑。使能输出之前，首先将音量设置在静音状态。一旦使能，首先关闭静音，然后音频信号缓变到所设置的音量等级。关断期间，在禁止输出之前控制音量缓变到最小增益，然后静音。如果使能过零检测，每次音量变化均发生在过零时刻。

没有音频信号时，过零检测会超时，以避免音量平滑。使能音量平滑增强控制电路，可以防止音量控制器在建立前期设置的音量之前，发出另一音量调整请求。由此，每一步音量调整均发生在音频信号过零之后或超出超时窗口之后。关断期间，禁用音量平滑增强控制。

## 插孔检测

器件具有灵活、软件可配置的插孔检测接口。使能时，插孔检测接口利用两个内部比较器检测插孔的插入/拔出，并判断插入插孔的类型(耳机或耳麦)。器件关断或禁止麦克风偏置时，比较器门限以$V_{SPKLVDD}$为基准；器件有效工作或使能麦克风偏置时，比较器门限以$V_{MICBIAS}$为基准。

无插孔插入动作时，插孔检测工作依赖于上拉电阻设置的偏置电压。器件处于关断模式或禁止麦克风偏置时(MICBIAS为高阻态)，使能JACKSNS的内部上拉，以SPKLVDD电源为基准；器件未处于关断状态且使能麦克风偏置时，禁止内部上拉(JACKSNS为高阻态)，此时需要通过外部将JACKSNS上拉至MICBIAS，才能正确进行插孔检测。插孔检测的内部接口结构及典型外部应用电路如图43所示。

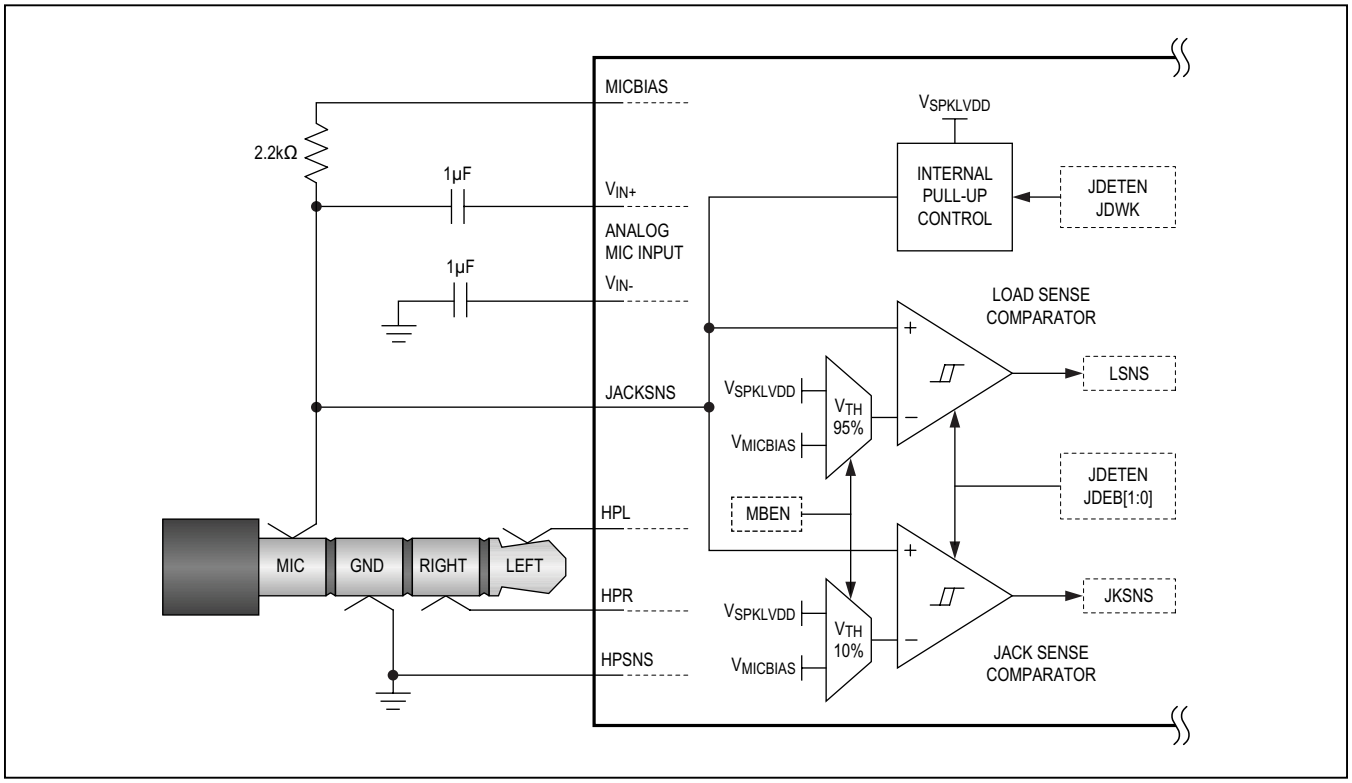



*图43. 插孔检测方框图及典型应用电路*

表76. 插孔检测状态结果

| JACKSNS VOLTAGE | JACK DETECTION RESULTS | | |
|---|---|---|---|
| | LSNS | JKSNS | STATE |
| $V_{TH\_95\%} \le V_{JACKSNS}$ | 1 | 1 | No jack detected |
| $V_{TH\_10\%} \le V_{JACKSNS} < V_{TH\_95\%}$ | 0 | 1 | Headset detected |
| $V_{JACKSNS} < V_{TH\_10\%}$ | 0 | 0 | Headphones detected |
| No condition | 1 | 0 | Not possible/reserved |

### 插孔检测内部比较器

使能时，器件通过使用两个内部比较器监测JACKSNS电压，检测插孔插入和拔出。负载检测比较器的门限为基准电压的95%，用于确定是否有插孔插入或拔出；插孔检测比较器的门限为基准电压的10%，用于判断插入的插孔类型(耳机/耳麦) (图78)。

无插孔插入动作时(开路)，通过上拉电阻提供高电平；这种状态下，VJACKSNS高于负载检测比较器门限，LSNS置高，表示无插孔插入。插孔插入时，对JACKSNS加载，将电压拉低至负载检测比较器门限以下，LSNS则置低，表示有插孔插入；拔出插孔时，上拉电阻再次回到高电平，LSNS置高，表示拔出插孔。

插入插孔时，对JACKSNS加载，将电压拉低至负载检测比较器门限以下；然而，根据所连接插孔类型的不同，电压拉低至可能低于、也可能不低于插孔检测比较器门限。如果插入的是耳机(3极)，JACKSNS短路至地，这就将电压拉低至插孔检测比较器门限(基准电压的10%)以下，JKSNS置低，表示插入的是耳机；相反，如果插入的是耳麦(4极，如图44所示)，JACKSNS偏置至介于基准电压和地之间的某个电压，VJACKSNS此时高于插孔检测比较器门限，但低于负载检测比较器门限，这种状态表示插入的是耳麦。表76详细列出了三种可能的插孔检测状态结果。

这些比较器只有在JDETEN置高时才有效。禁止插孔检测时，JACKSNS处于高阻态，接口完全关断。器件处于关断状态时，JDETEN为逻辑低，LSNS和JKSNS维持其前一状态，与插孔状态无关。

### 插孔检测可编程去抖

负载检测和插孔检测比较器也具有可编程去抖超时。去抖超时确保在新状态持续时间达到超时之前不改变插孔检测状态，可防止LSNS和JKSNS在插孔插入/拔出瞬间发生快速变化，以及确保不产生错误的插孔检测中断。去抖超时可设置为从25ms至200ms的四种设置之一(表77)。

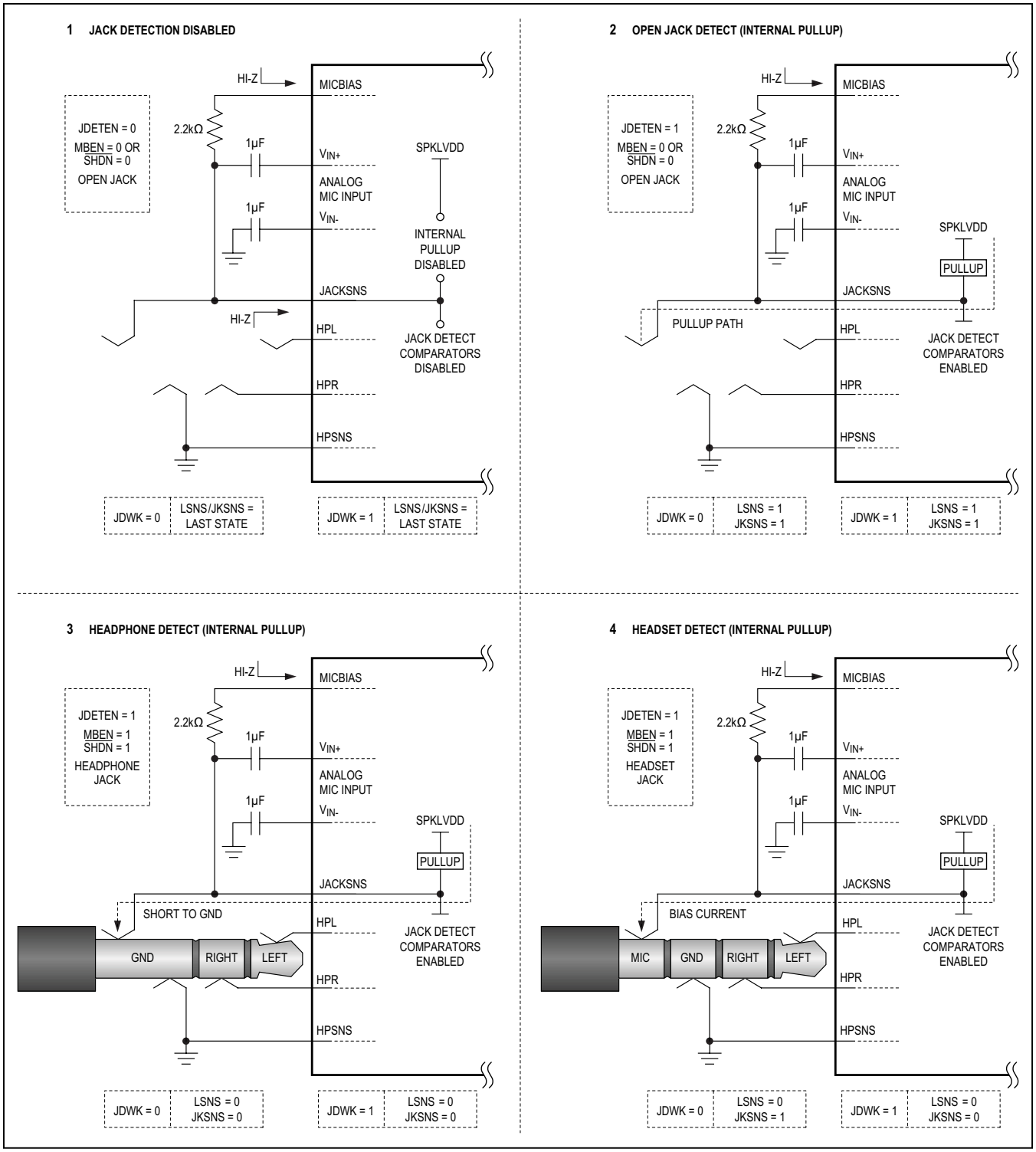



*图44. 利用内部上拉电阻进行插孔检测的示例*

### 插孔检测中断

插入或拔出插孔以及LSNS或JKSNS的状态变化时，利用插孔配置变化标识(JDET，表85)表示插孔检测事件。如果未屏蔽插孔检测事件(IJDET，表86)，事件也在$\overline{IRQ}$产生中断。插孔检测事件位(JDET)为读清除。I²C读操作清除JDET位状态和$\overline{IRQ}$上的中断(如果有)。在每次插孔检测事件后，除非发生读操作，JDET位和$\overline{IRQ}$中断将保持有效状态，不能检测到新事件或中断。

从LSNS = 1到LSNS = 0的状态变化表示插孔已插入，从LSNS = 0到LSNS = 1的状态变化表示插孔已拔出。发生插入时，如果JKSNS无变化，仍然保持JKSNS = 1，表示耳麦插入；如果状态从JKSNS = 1变为JKSNS = 0，表示插入的是耳机。状态跳变以及产生的中断事件理想用于插孔检测软件驱动中的状态机控制。

### 使用内部上拉电阻

器件具有内部强上拉和弱上拉选项。只有器件处于关断状态($\overline{SHDN}$ = 0，表6)或禁止MICBIAS时(MBEN = 0，表7)，内部上拉电阻才有效，允许在这些状态下正常进行插孔检测和识别。该功能理想用于器件处于休眠或关断状态，但需要利用插入操作触发器件或系统级中断信号进行唤醒时。

JDWK为逻辑低(默认，表77)，使用内部强上拉(约2.4kΩ，以SPKLVDD为基准)，该配置能够检测和识别耳机和耳麦插入；JDWK为逻辑高时，使用内部弱上拉(约5µA至SPKLVDD)。内部弱上拉降低了插孔检测之后的供电电流，适合在系统不会立即唤醒的状态下插入。内部弱上拉不能偏置麦克风负载，所以不能识别耳麦插入或按下附件按钮的情况。

图44详细说明利用内部上拉电阻进行插孔检测的工作情况。示例1中，禁止插孔检测，MICBIAS和JACKSNS均为高阻；此时，LSNS和JKSNS维持上次有效的插孔检测结果。示例2中，无插孔插入，连接至SPKLVDD的内部上拉电阻将JACKSNS拉高至负载和插孔检测比较器门限以上；此时，插孔开路，内部强上拉和弱上拉电阻均产生正确的插孔检测结果，唯一的功耗是偏置内部比较器。示例3中，耳机插孔插入，将JACKSNS短路至地，正好低于负载和插孔检测比较器门限；此时，内部强上拉和弱上拉均产生正确的插孔检测结果，但内部强上拉的耗流显著高于内部弱上拉。示例4中，耳麦插孔插入，此时，内部强上拉和弱上拉产生不同的插孔检测结果；内部强上拉将耳麦MIC (及JACKSNS)偏置至介于负载检测和插孔检测比较器门限之间的某个电平，产生正确的插孔检测结果；然而，内部弱上拉不足以偏置耳麦MIC，所以错误检测为插入的是耳机。

### 使用外部上拉电阻

内部上拉电阻足以满足中断唤醒或基本的插孔检测和识别，但为了对耳麦麦克风进行正确偏置和限流，需要连接至MICBIAS的外部上拉电阻(图43)。使能插孔检测、器件活跃($\overline{SHDN}$ = 1，表6)且使能MICBIAS时(MBEN = 1，表7)，JACKSNS处于高阻态，禁止内部上拉电阻；此时，外部上拉电阻决定JACKSNS的偏置电压。

图45详细说明利用外部上拉电阻进行插孔检测的工作情况。示例1中，禁止插孔检测，所以禁止内部插孔检测比较器，LSNS/JKSNS维持其上次有效的插孔检测结果。示例2中，无插孔插入，连接至MICBIAS的外部上拉电阻将JACKSNS拉高至负载和插孔检测比较器门限以上。示例3中，耳机插孔插入，将JACKSNS短路至地，正好低于负载和插孔检测比较器门限。示例4中，耳麦插孔插入，外部上拉电阻将耳麦MIC (及JACKSNS)偏置至介于负载检测和插孔检测比较器门限之间的某个电平。

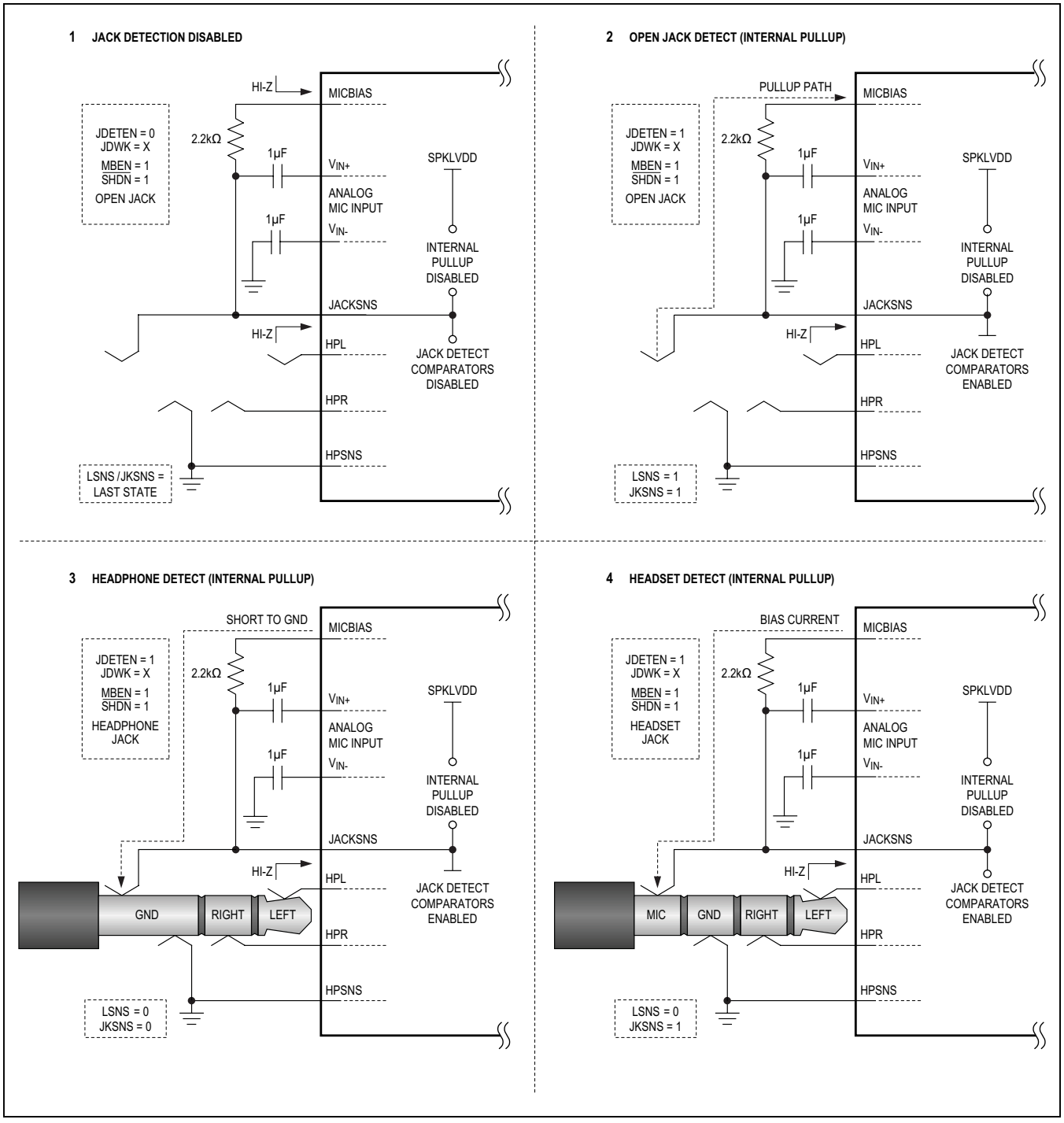



*图45. 利用外部上拉电阻进行插孔检测的示例*

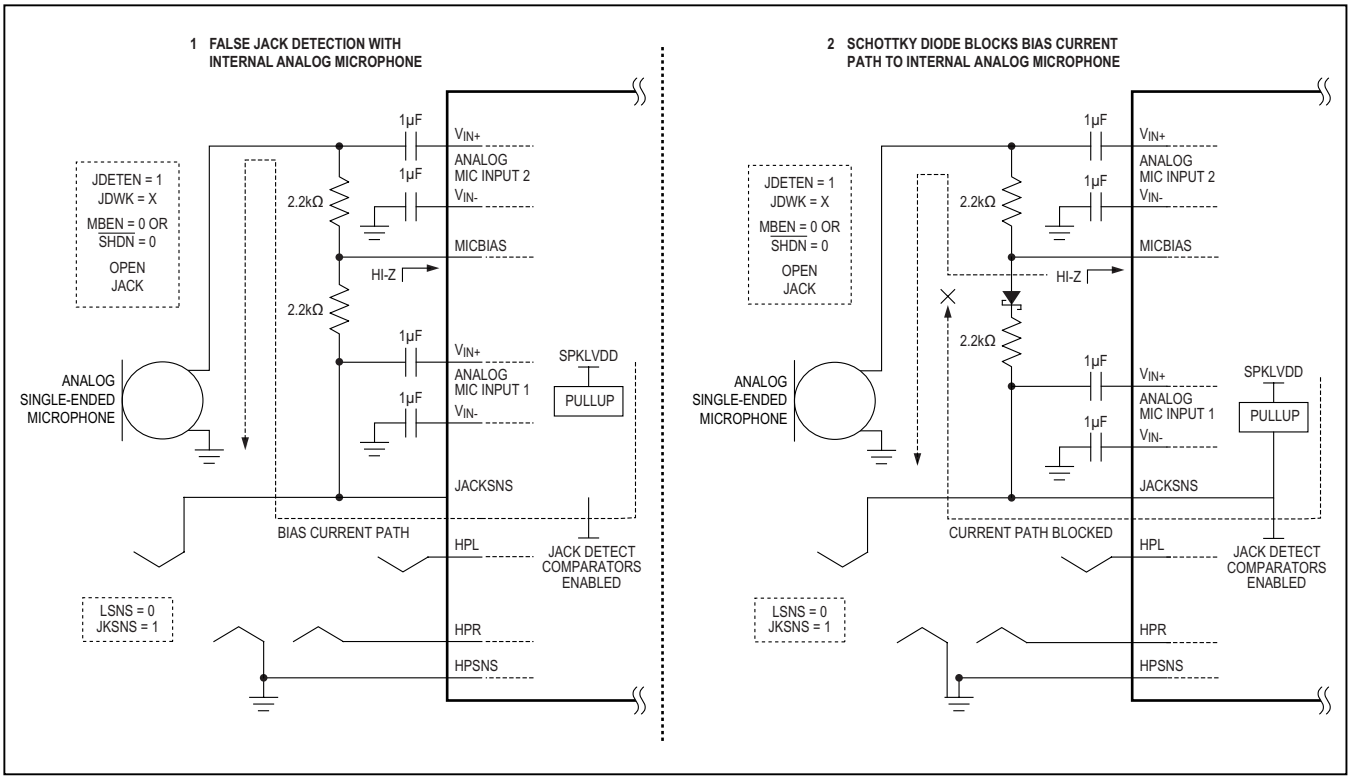



*图46. 利用内部模拟麦克风进行插孔检测*

## 附件按钮检测

插入插孔后，器件可检测附件上的按键是否按下，包括麦克风和将麦克风信号对地短路的开关。使能MICBIAS时，或者将其禁止并使用内部强上拉(JDWK = 0)时，均可检测按钮是否按下。按下按钮时将JKSNS的状态从1改变为0，直到释放按钮，并且这种状态变化在插孔检测变化标识(JDET)上产生事件。该事件用于触发与按下按钮相关的动作。

## 利用内部模拟麦克风进行插孔检测

如果应用要求固定的内部模拟麦克风，并且也必须检测、识别以及配合耳麦麦克风工作，通用的插孔检测应用电路(图43)将不能满足要求。使用内部模拟麦克风的应用详细信息请参见图46。

无插孔插入时(示例1)，内部上拉电阻试图将JACKSNS上拉至负载检测比较器门限以上；然而连接至MICBIAS的外部上拉电阻形成通过内部模拟麦克风上拉电阻的电流通路。所以，JACKSNS电压偏置在介于插孔检测和负载检测比较器门限之间的某个电平，造成错误的耳麦插孔检测。耳麦插孔插入时，JACKSNS插入耳麦插孔和内部模拟麦克风之间有一个并联负载，这可能会将耳麦当做耳机。

可插入一个正向压降极低的肖特基二极管，使其与外部上拉电阻串联(示例2)。关闭MICBIAS时，肖特基二极管反向偏置，阻塞电流通路；使能MICBIAS时，二极管正向偏置，连接至麦克偏置的外部上拉电阻正常工作，详细信息请参见图45。二极管会产生串联压降，需要调整MICBIAS电压和/或串联电阻值，以进行补偿，以及确保正确偏置耳麦MIC。也可以将一个开关串联在内部模拟麦克风上方或下方，在禁止MICBIAS时断开偏置电流通路。

## 表77. 插孔检测配置寄存器

| ADDRESS: 0x3D | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | JDETEN | R/W | 0 | **Jack Detect Enable**<br>0: Jack detect circuitry disabled<br>1: Jack detect circuitry enabled |
| 6 | JDWK | R/W | 0 | **JACKSNS Pullup Configuration**<br>0: 2.4kΩ resistor to SPKLVDD (allows microphone detection)<br>1: 5µA to SPKLVDD (minimizes supply current)<br>Valid when MICBIAS = 0 or $\overline{SHDN}$ = 0. |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | JDEB[1:0] | R/W | 0 | **Jack Detect Debounce**<br>Configures the jack detect debounce time:<br>00: 25ms 10: 100ms<br>01: 50ms 11: 200ms |
| 0 | | | 0 | |

## 表78. 插孔状态寄存器

| ADDRESS: 0x02 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | LSNS | R | 0 | **Microphone Load Sense (Valid Only if JDETEN = 1)**<br>0: $V_{JACKSNS} \le 0.95V \times V_{SUPPLY}$<br>1: $V_{JACKSNS} > 0.95V \times V_{SUPPLY}$<br>$V_{SUPPLY}$ is determined by the state of MBEN and $\overline{SHDN}$ so that:<br>MBEN = 0 or $\overline{SHDN}$ = 0: $V_{SUPPLY} = V_{SPKLVDD}$ (internal pullup)<br>MBEN = 1 and $\overline{SHDN}$ = 1: $V_{SUPPLY} = V_{MICBIAS}$ (external pullup) |
| 1 | JKSNS | R | 0 | **Jack Connection Sense (Valid Only if JDETEN = 1)**<br>0: $V_{JACKSNS} < 0.1V \times V_{SUPPLY}$<br>1: $V_{JACKSNS} \ge 0.1V \times V_{SUPPLY}$<br>$V_{SUPPLY}$ is determined by the state of MBEN and $\overline{SHDN}$ so that:<br>MBEN = 0 or $\overline{SHDN}$ = 0: $V_{SUPPLY} = V_{SPKLVDD}$ (internal pullup)<br>MBEN = 1 and $\overline{SHDN}$ = 1: $V_{SUPPLY} = V_{MICBIAS}$ (external pullup) |
| 0 | — | — | — | — |

## 快速配置

快速配置寄存器为常用的信号通路和设置提供了一个简单的器件配置选项。每个快速配置寄存器包含只写、按键配置位。写入逻辑高时，快速配置位将在内部设置其它相应的全部寄存器位，将器件置为所选配置；向快速配置位写逻辑低没有影响，读取所有快速配置位时，始终返回逻辑低。

快速设置位仅更改与所选配置相对应的寄存器，不删除或复位非共用配置寄存器的当前配置，允许以一定的逻辑顺序使用多个不同快速配置寄存器的互补选项，以配置器件。不要将配置相同部分或共用数据通路的多个快速设置位组合在单个序列中，由于之后的快速设置位可能覆盖早期设置的寄存器，所以这种类型的序列可能不会产生预期结果。

数字音频接口(DAI)快速设置寄存器(表79)用于选择DAI数据格式，该寄存器中的配置设置主机模式时钟配置寄存器(表34)、DAI格式配置寄存器(表46)和DAI TDM控制寄存器(表47)。

回放通路快速设置寄存器(表80)用于配置数字回放通路以及选择和设置模拟输出，该寄存器中的配置位设置DAI I/O配置寄存器(表45)、输出使能寄存器(表8)，以及所选模拟输出混音器、音量和控制寄存器(耳机、接收器、扬声器或线出)。

### 表79. 数字音频接口(DAI)快速设置寄存器

| ADDRESS: 0x06 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | — | — | — | — |
| 6 | — | — | — | — |
| 5 | RJ_M | W | 0 | Sets up DAI for right-justified master mode operation. |
| 4 | RJ_S | W | 0 | Sets up DAI for right-justified slave mode operation. |
| 3 | LJ_M | W | 0 | Sets up DAI for left-justified master mode operation. |
| 2 | LJ_S | W | 0 | Sets up DAI for left-justified slave mode operation. |
| 1 | I2S_M | W | 0 | Sets up DAI for $I^2S$ master mode operation. |
| 0 | I2S_S | W | 0 | Sets up DAI for $I^2S$ slave mode operation. |

### 表80. 回放通路快速设置寄存器

| ADDRESS: 0x07 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | DIG2_HP | W | 0 | Sets up the DAC to headphone path. |
| 6 | DIG2_EAR | W | 0 | Sets up the DAC to receiver path. |
| 5 | DIG2_SPK | W | 0 | Sets up the DAC to speaker path |
| 4 | DIG2_LOUT | W | 0 | Sets up the DAC to line out path. |
| 3 | — | — | — | — |
| 2 | — | — | — | — |
| 1 | — | — | — | — |
| 0 | — | — | — | — |

模拟麦克风/直接输入至录音通路快速设置寄存器(表81)用于选择、设置模拟输入以及配置数字录音通路，该寄存器中的配置位设置DAI I/O配置寄存器(表45)、输入使能寄存器(表7)，以及相应的输入混音器、音量和控制寄存器(模拟麦克风或直接至ADC混音器)。

线入至录音通路快速设置寄存器(表82)用于设置模拟输入以及配置数字录音通路，该寄存器中的配置位设置DAI I/O配置寄存器(表45)、输入使能寄存器(表7)，以及相应的输入混音器、音量和控制寄存器(单端或差分线入)。

## 表81. 模拟麦克风/直接输入至录音通路快速设置寄存器

| ADDRESS: 0x08 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | IN12_MIC1 | W | 0 | Sets up the IN1/IN2 to microphone 1 to ADCL path |
| 6 | IN34_MIC2 | W | 0 | Sets up the IN3/IN4 to microphone 2 to ADCR path |
| 5 | — | — | — | — |
| 4 | — | — | — | — |
| 3 | IN12_DADC | W | 0 | Sets up the IN1/IN2 direct to ADCL path |
| 2 | IN34_DADC | W | 0 | Sets up the IN3/IN4 direct to ADCR path |
| 1 | IN56_DADC | W | 0 | Sets up the IN5/IN6 direct to ADCL path (WLP only) |
| 0 | — | — | — | — |

## 表82. 线入至录音通路快速设置寄存器

| ADDRESS: 0x09 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | IN12S_AB | W | 0 | Sets up stereo single-ended record: IN1/IN2 to line in A/B to ADCL/R |
| 6 | IN34S_AB | W | 0 | Sets up stereo single-ended record: IN3/IN4 to line in A/B to ADCL/R |
| 5 | IN56S_AB | W | 0 | Sets up stereo single-ended record: IN5/IN6 to line in A/B to ADCL/R (WLP only) |
| 4 | IN34D_A | W | 0 | Sets up mono differential record: IN3/IN4 to line in A to ADCL |
| 3 | IN65D_B | W | 0 | Sets up mono differential record: IN6/IN5 to line in B to ADCR (WLP only) |
| 2 | — | — | — | — |
| 1 | — | — | — | — |
| 0 | — | — | — | — |

模拟麦克风输入至模拟输出快速设置寄存器(表83)用于配置模拟输入以及选择、设置模拟输出，该寄存器的配置位设置输入使能寄存器(表7)、输出使能寄存器(表8)，以及相应输入和输出混音器、音量和控制寄存器(模拟麦克风以及耳机、扬声器、接收器或线路输出)。

线路输入至模拟输出快速设置寄存器(表84)用于配置模拟输入以及选择和设置模拟输出，该寄存器中的配置位设置输入使能寄存器(表7)、输出使能寄存器(表8)，以及相应输入和输出混音器、音量和控制寄存器(线路输入以及耳机、扬声器、接收器或线路输出)。

## 表83. 模拟麦克风输入至模拟输出快速设置寄存器

| ADDRESS: 0x0A | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | IN12_M1HPL | W | 0 | Sets up the IN1/IN2 differential to microphone 1 to headphone left path |
| 6 | IN12_M1SPKL | W | 0 | Sets up the IN1/IN2 differential to microphone 1 to speaker left path |
| 5 | IN12_M1EAR | W | 0 | Sets up the IN1/IN2 differential to microphone 1 to receiver path |
| 4 | IN12_M1LOUTL | W | 0 | Sets up the IN1/IN2 differential to microphone 1 to lineout left path |
| 3 | IN34_M2HPR | W | 0 | Sets up the IN3/IN4 differential to microphone 2 to headphone right path |
| 2 | IN34_M2SPKR | W | 0 | Sets up the IN3/IN4 differential to microphone 2 to speaker right path |
| 1 | IN34_M2EAR | W | 0 | Sets up the IN3/IN4 differential to microphone 2 to receiver path |
| 0 | IN34_M2LOUTR | W | 0 | Sets up the IN3/IN4 differential to microphone 2 to lineout right path |

## 表84. 线入至模拟输出快速设置寄存器

| ADDRESS: 0x0B | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | IN12S_ABHP | W | 0 | Sets up the IN1/IN2 single ended to line In A/B to headphone L/R path |
| 6 | IN34D_ASPKL | W | 0 | Sets up the IN3/IN4 differential to line in A to speaker left path |
| 5 | IN34D_AEAR | W | 0 | Sets up the IN3/IN4 differential to line in A to receiver path |
| 4 | IN12S_ABLOUT | W | 0 | Sets up the IN1/IN2 single ended to line in A/B to lineout L/R path |
| 3 | IN34S_ABHP | W | 0 | Sets up the IN3/IN4 single ended to line in A/B to headphone L/R path |
| 2 | IN65D_BSPKR | W | 0 | Sets up the IN6/IN5 differential to line in B to speaker right path (WLP only) |
| 1 | IN65D_BEAR | W | 0 | Sets up the IN6/IN5 differential to line in B to receiver path (WLP only) |
| 0 | IN34S_ABLOUT | W | 0 | Sets up the IN3/IN4 single ended to line in A/B to lineout L/R path |

## 器件状态标识

器件利用寄存器0x01 (表85)和$\overline{IRQ}$报告器件各种功能的状态，发生某个事件时，置位相应的状态寄存器位，读取寄存器后清零。可通过轮询寄存器0x01或将$\overline{IRQ}$配置成发生特定事件时拉低，以确定器件状态。$\overline{IRQ}$为开漏输出，需要上拉电阻(标称10kΩ)才能正常工作。首次退出关断状态(进入常规工作)时，其它状态标识可能变为有效，取决于器件设置、寄存器排序和时钟排序。

### 状态标识屏蔽

寄存器0x03为器件状态中断屏蔽寄存器(表86)，决定器件状态中断寄存器(表85)中的哪些位可触发$\overline{IRQ}$硬中断(有效

## 表85. 器件状态中断寄存器

| ADDRESS: 0x01 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | CLD | CoR | 0 | **Clipping Detect Flag**<br>0: No clipping has occurred.<br>1: Digital record / playback clipping has occurred.<br>CLD asserts when the digital record or playback path is clipping due to signal amplitude exceeding full-scale. This condition is detected at the record path gain control output (AVLG/AVRG), the playback path gain control output (DVG), and the parametric equalizer output. To resolve, adjust the gain settings near these detection points. |
| 6 | SLD | CoR | 0 | **Slew Level Detect Flag**<br>0: No volume slewing sequences have completed.<br>1: All volume / level slewing complete.<br>SLD asserts when any one (or more) of the programmable-gain analog output volume controllers or digital level control arrays has completed slewing from a previous setting to a new programmed setting. If multiple settings are changed at the same time, in either the analog or digital domain, the SLD flag will assert only after the last slew is completed. SLD also asserts when the serial interface soft-start or soft-stop process has completed. |
| 5 | ULK | CoR | 0 | **Digital Audio Interface (DAI) Phase Locked Loop (PLL) Unlock Flag**<br>0: PLL is locked (if enabled and operating properly).<br>1: PLL is not locked (if enabled and operating properly).<br>ULK reports that the digital audio phase-locked loop for DAI is not locked. This condition only occurs in slave mode when the deviation on LRCLK relative to PCLK exceeds the lock on range (approximately 4 PCLK periods). This condition can also occur if PCLK is running and LRCLK has been stopped outside of shutdown. Deviation in BCLK (or shutting it down) will never trigger a ULK assertion. DAI input and output data may not be processed / clocked correctly if a ULK event occurs. |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | JDET | CoR | 0 | **Jack Configuration Change Flag**<br>0: No change in jack configuration.<br>1: Jack configuration has changed.<br>JDET asserts anytime jack detection is enabled, and either LSNS or JKSNS changes state (Table 78). If jack detection is enabled, JDET will assert correctly even while the device is in the shutdown state. This allows JDET to generate wake on insert interrupts. |
| 1 | DRCACT | CoR | 0 | **DRC Compression Flag**<br>0: The DRC is either disabled or not in the compression region.<br>1: The DRC is operating in the compression region. |
| 0 | DRCCLP | CoR | 0 | **DRC Clipping Flag**<br>0: The DRC is either disabled or no clipping has occurred.<br>1: DRC clipping has occurred. |

低电平)。默认设置下，器件的全部状态中断(JDET除外)仅置位相应的状态位，不产生硬中断。将屏蔽寄存器中的对应位置高时，使能硬中断。

## 器件版本标识

器件提供版本ID号寄存器，允许软件识别器件的当前版本。器件的当前版本ID值为0x43。

### 表86. 器件状态中断屏蔽寄存器

| ADDRESS: 0x03 | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | ICLD | R/W | 0 | **Clipping Detect Interrupt Enable**<br>0: Clipping detection only sets CLD (0x01[7]).<br>1: Clipping detection triggers $\overline{IRQ}$ and sets CLD (0x02[7]). |
| 6 | ISLD | R/W | 0 | **Slew Level Detect Interrupt Enable**<br>0: Slew level detection only sets SLD (0x01[6]).<br>1: Slew level detection triggers $\overline{IRQ}$ and sets SLD (0x02[6]). |
| 5 | IULK | R/W | 0 | **Digital PLL Unlock Interrupt Enable**<br>0: PLL Unlock Condition only sets ULK (0x01[5]).<br>1: PLL Unlock Condition triggers $\overline{IRQ}$ and sets ULK (0x02[5]). |
| 4 | — | — | — | — |
| 3 | — | — | — | — |
| 2 | IJDET | R/W | 1 | **Jack Configuration Change Interrupt Enable**<br>0: Changes in headset configuration only sets JDET (0x01[2]).<br>1: Changes in headset configuration triggers $\overline{IRQ}$ and sets JDET (0x01[2]). |
| 1 | IDRCACT | R/W | 0 | **DRC Compression Interrupt Enable**<br>0: DRC compression only sets DRCACT (0x01[1]).<br>1: DRC compression triggers $\overline{IRQ}$ and sets DRCACT (0x01[1]). |
| 0 | IDRCCLP | R/W | 0 | **DRC Clipping Interrupt Enable**<br>0: DRC clipping only sets DRCCLP (0x01[0]).<br>1: DRC clipping triggers $\overline{IRQ}$ and sets DRCCLP (0x01[0]). |

### 表87. 版本ID号寄存器

| ADDRESS: 0xFF | | | | DESCRIPTION |
|---|---|---|---|---|
| BIT | NAME | TYPE | POR | |
| 7 | REV_ID[7:0] | R | 0 | **Read Back the Revision ID of the Device**<br>The current revision ID is 0x43. |
| 6 | | | 1 | |
| 5 | | | 0 | |
| 4 | | | 0 | |
| 3 | | | 0 | |
| 2 | | | 0 | |
| 1 | | | 1 | |
| 0 | | | 1 | |

## I²C串行接口

MAX98090采用I²C /SMBus兼容的2线串行接口，包括一根串行数据线(SDA)和一根串行时钟线(SCL)。SDA和SCL的时钟速率高达400kHz，方便了MAX98090和主机之间的通信。图3所示为2线接口的时序图。主机在总线上产生SCL并发起数据传输。主机发送相应的从地址和寄存器地址，随后是发送的数据字，由此向MAX98090写入数据。

每次传输都以START (S)或REPEATED START (Sr)条件和STOP (P)条件打包成帧。发送给MAX98090的每个字长为8位，其后是应答时钟脉冲。主机从MAX98090读取数据时发送相应的从地址，随后是9个SCL脉冲。MAX98090通过SDA发送数据，与主机产生的SCL脉冲同步。主机在接收到每字节数据后对其进行应答。每次读操作由START (S)或REPEATED START (Sr)条件、非应答和STOP (P)条件打包成帧。SDA既是输入又是开漏输出，SDA需要一个上拉电阻，通常大于500Ω。SCL仅作为输入，如果总线上有多个主机，或者单主机具有开漏SCL输出，SCL也将需要一个上拉电阻，通常大于500Ω。SDA和SCL总线串联电阻可选。串联电阻保护MAX98090的数字输入免受总线上高压毛刺的冲击，并最大程度地降低总线信号的串扰和下冲。

## 表88. 器件I²C从地址

| PART NUMBER | READ ADDRESS | WRITE ADDRESS |
|---|---|---|
| MAX98090A | 0x21 | 0x20 |
| MAX98090B | 0x23 | 0x22 |

### 位传输

每个SCL周期传输一位数据。在SCL脉冲的高电平期间内，SDA上的数据必须保持稳定。SCL为高电平时，SDA上的变化将产生控制信号，请参见*START和STOP条件*部分。

### START和STOP条件

总线空闲时，SDA和SCL的空闲状态为高电平。主机通过发送START条件启动通信，START条件是SCL为高电平时，SDA由高到低的跳变。STOP条件是SCL为高电平时，SDA由低到高跳变。来自主机的START条件通知MAX98090开始传输。主机通过发送STOP条件终止传输并释放总线。如果产生的是REPEATED START条件(而不是STOP条件)，则总线保持有效。

### 提前STOP条件

MAX98090在数据传输期间可随时识别STOP条件，除非STOP条件与START条件出现在同一高电平脉冲。为确保正常工作，请勿在START条件的同一SCL高电平脉冲期间发送STOP条件。

### 从地址

从地址定义为7个最高位(MSB)，后边跟读/写控制位。对于MAX98090，7个最高位为0010000。将读/写控制位设置为1 (从地址 = 0x21)，使MAX98090配置为读模式；将读/写控制位设置为0 (从地址 = 0x20)，使MAX98090配置为写模式。该地址是在START条件后发送到MAX98090的第一个字节。类似地，对于该MAX98090，7个最高位为0010001。将读/写控制位设置为1 (从地址 = 0x23)，使MAX98090配置为读模式；将读/写控制位设置为0 (从地址 = 0x22)，使MAX98090配置为写模式。从地址汇总于表88。

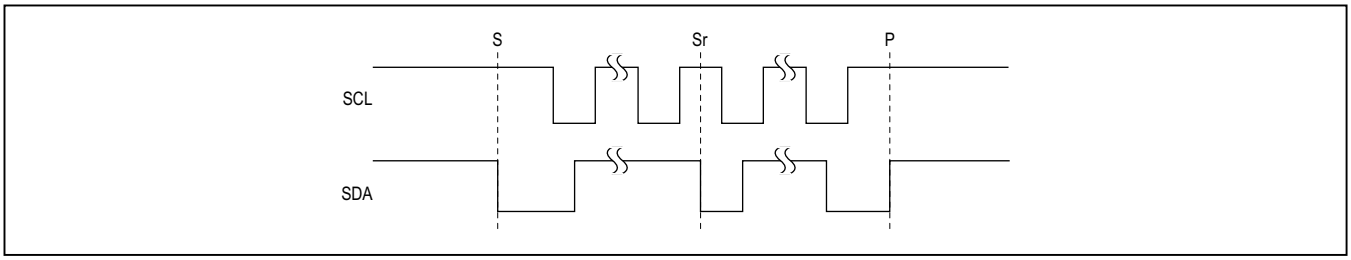



*图47. START、STOP和REPEATED START条件*

### 应答

写操作中，应答位(ACK)是第9个时钟位，是MAX98090对其接收的每个数据字节的握手信号。如果成功接收了之前的字节，那么MAX98090在主控制器产生的第9个时钟脉冲期间拉低SDA。监测ACK可以检测失败的数据传输。如果接收器件忙，或者系统发生故障，则会导致数据传输失败。数据传输失败时，总线主机会重新开始通信。当MAX98090处于读操作时，在第9个时钟脉冲期间，主控制器拉低SDA，以应答数据接收。每次读取字节后，主机均发送应答信号，以便继续传输数据。当主机从MAX98090读取数据的最后一个字节时，发送非应答，随后是STOP条件。

### 写数据格式

对MAX98090的写操作包括：START条件、从机地址(R/$\overline{W}$位置0)、配置内部寄存器地址指针的一个数据字节、1个或多个数据字节和STOP条件。图49所示为向MAX98090写入1个字节数据时的正确帧格式，图50所示为向MAX98090写入n个字节数据时的帧格式。

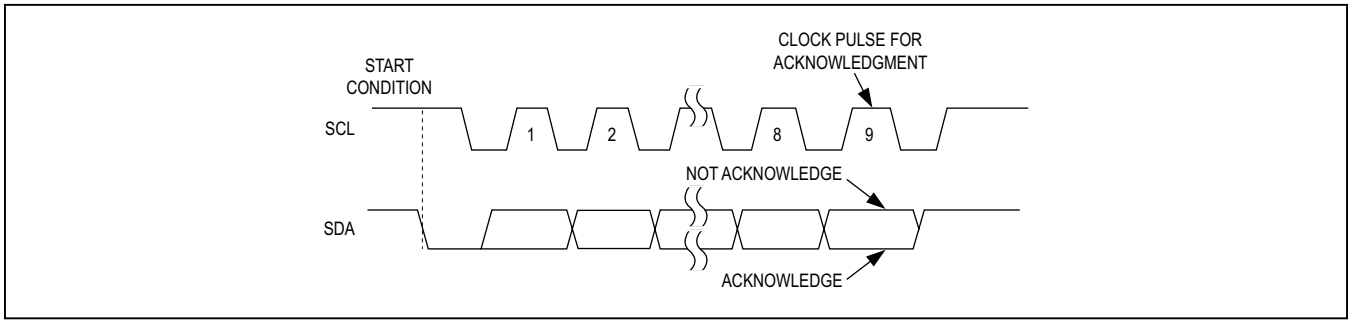



*图48. 应答时序*

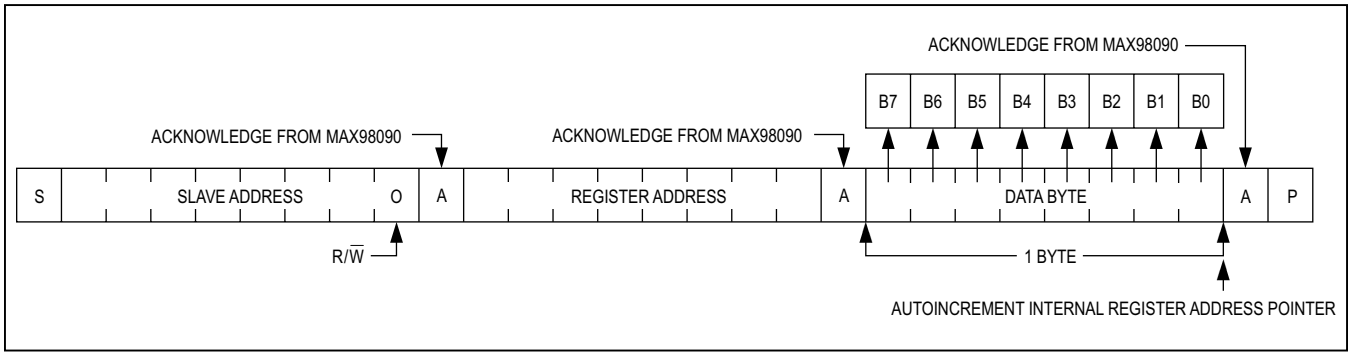



*图49. 向MAX98090写入1个数据字节*

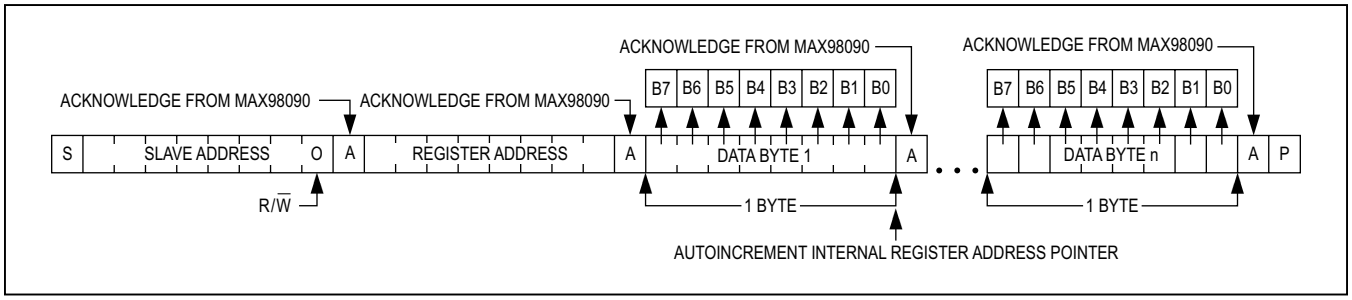



*图50. 向MAX98090写入n个数据字节*

R/$\overline{W}$位置0的从地址表示主控制器要向MAX98090写入数据。MAX98090在主控制器产生的第9个SCL脉冲期间应答接收到的地址。

从主控制器发送的第二字节配置MAX98090的内部寄存器地址指针，指针告诉MAX98090要写入的下一个字节的位置。接收到地址指针数据后，MAX98090发送一个应答脉冲。

发送到MAX98090的第三字节为写入指定寄存器的数据。MAX98090发送应答脉冲表示接收到数据字节，每次接收数据之后，地址指针自动递增至下一个寄存器地址。自动递增功能使主机能够在一个连续帧内连续进行寄存器写操作。主机通过发送STOP条件终止传输。0xE7以上的寄存器地址被保留，不要对这些地址进行写操作。

## 读数据格式

通过发送从地址，并将R/$\overline{W}$位置1，启动读操作。MAX98090在第9个SCL时钟脉冲期间拉低SDA，应答接收到的从地址。START条件之后为读命令，将地址指针复位到寄存器0x00。

从MAX98090发送的第一个字节是寄存器0x00的内容。发送数据在SCL的上升沿有效，地址指针在每次读取数据字节后都自动递增。这种自动递增功能使得在一个连续帧内可以连续读取全部寄存器的内容。读数据字节任何时刻都可发送STOP条件。如果发送了一个STOP条件，随后是另一个读操作，则读取的第一个字节为寄存器0x00的数据。

发送读命令之前，可将地址指针预设为某个特定的寄存器。主机预设地址指针时，首先发送MAX98090的从地址，并将R/$\overline{W}$位置0，随后跟寄存器地址。然后发送一个REPEATEDSTART条件和从地址，并将R/$\overline{W}$位置1。随后，MAX98090将传输指定寄存器的内容，地址指针在传输完第一个字节后自动递增。

主机在接收到每个读字节之后的应答时钟脉冲期间进行应答。主机必须应答除最后一个字节以外所有正确接收的字节。最后一个字节之后必须是来自主机的非应答，然后是STOP条件。图51所示为从MAX98090读取1个字节时的帧格式，图52所示为从MAX98090读取多个字节时的帧格式。

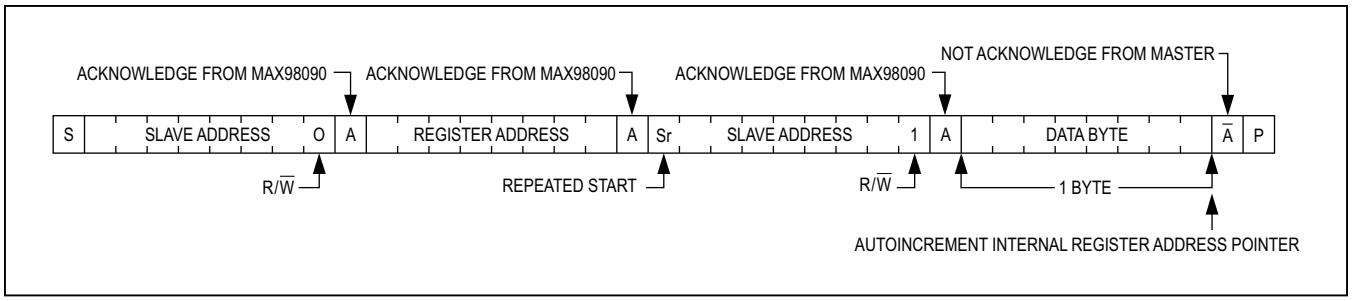



*图51. 从MAX98090读取1个字节的数据*

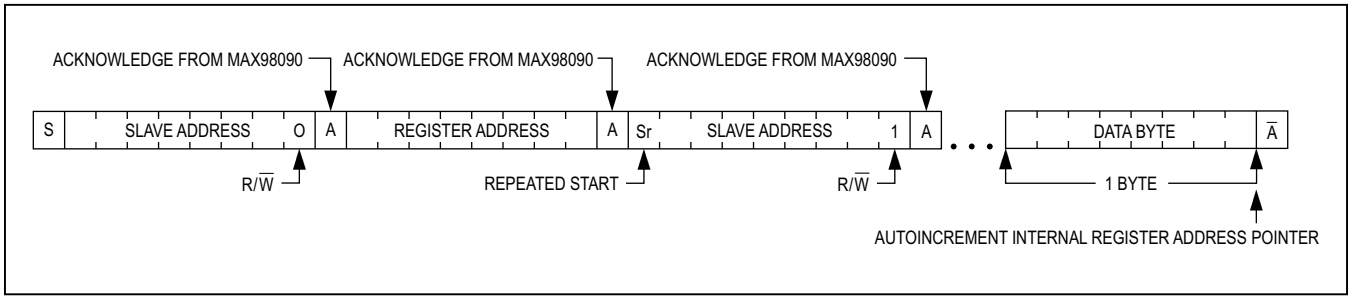



*图52. 从MAX98090读取n个字节的数据*

## 应用信息

### 典型应用电路

图53和图54为两个应用电路示例。图中外部元件为器件工作的最低要求。根据应用的不同，可能需要其它元件。

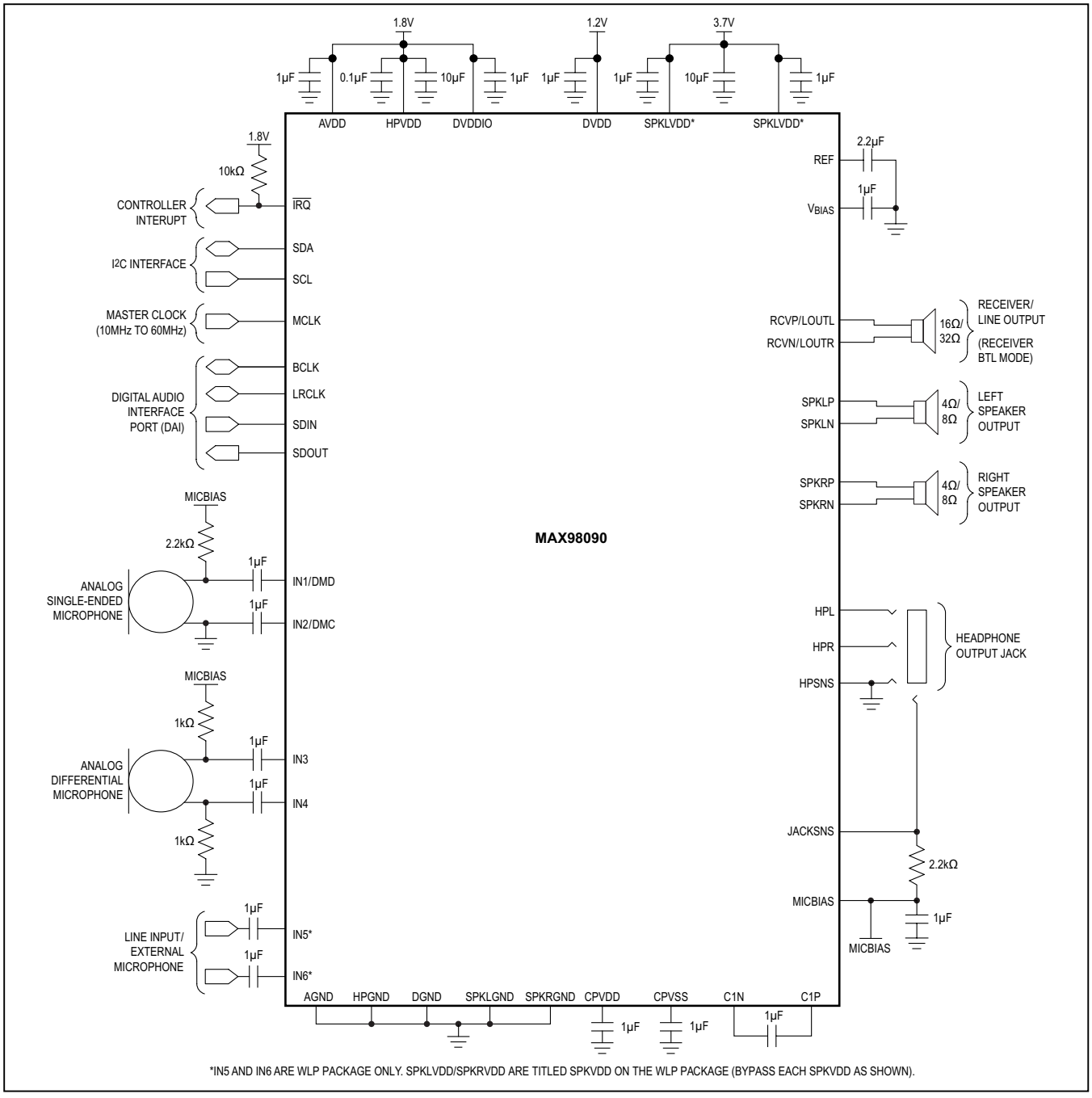
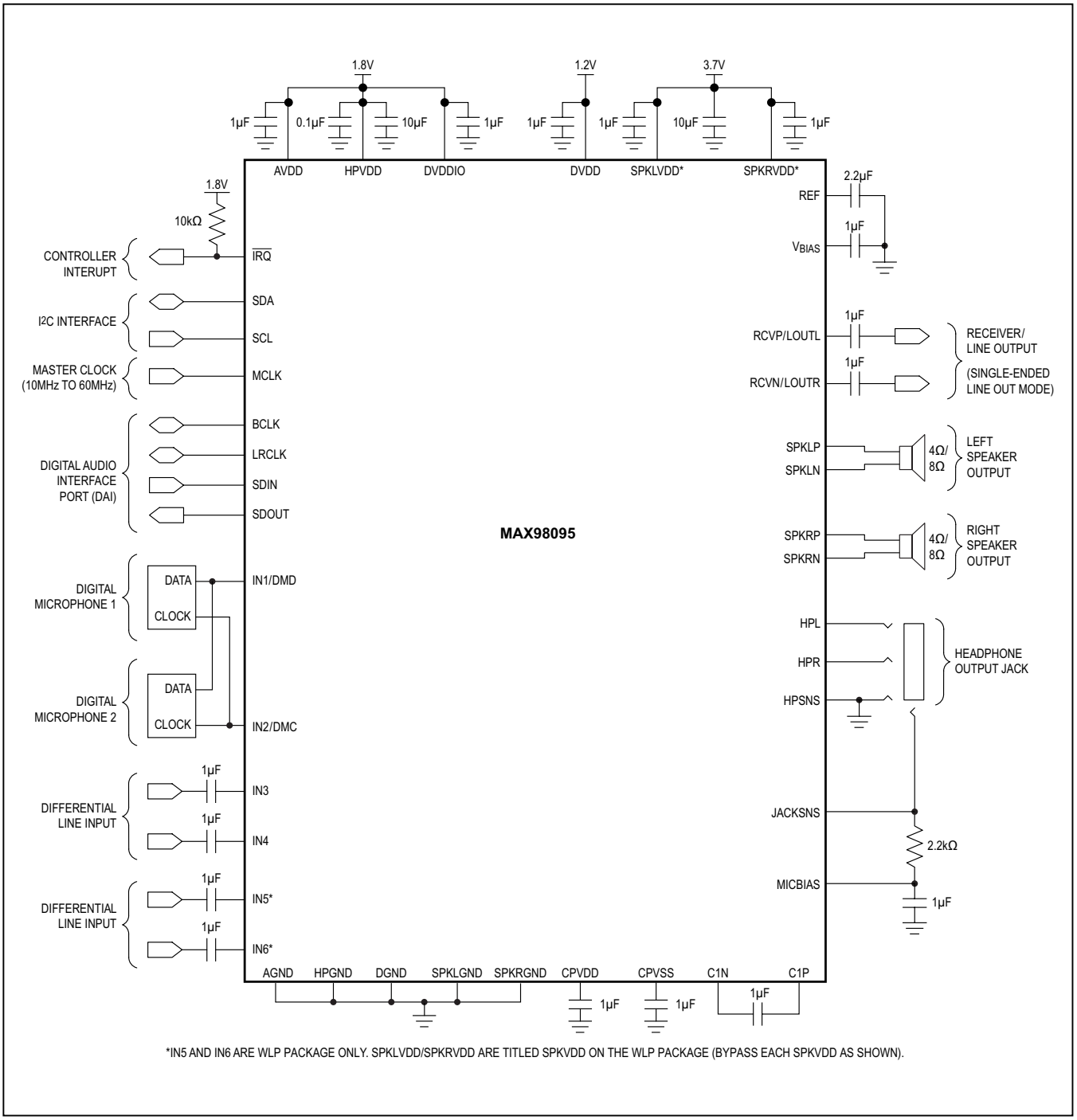



*图53. 使用模拟麦克风和接收器输出的典型应用电路*




*IN5 AND IN6 ARE WLP PACKAGE ONLY. SPKLVDD/SPKRVDD ARE TITLED SPKVDD ON THE WLP PACKAGE (BYPASS EACH SPKVDD AS SHOWN).

*图54. 使用数字麦克风输入和立体声线出的典型应用电路*

### 启动/关断寄存器排序

为了确保器件初始化及咔嗒/噼噗声最小化，以正确顺序配置器件的控制寄存器。为了关断器件，只需设置SHDN = 0。表89所示为器件的启动顺序示例。为将模拟输出驱动器(耳机、扬声器、接收器和线出)的咔嗒/噼噗声降至最小，应按照以下顺序为输出驱动器上电：

1) 器件上电($\overline{SHDN}$ = 0)之前及使能输出之前，应使能输出驱动器静音，应将PGA增益设置为其最低设置。
2) 完成配置设置之后，器件上电($\overline{SHDN}$ = 1)。
3) 使能相应配置下的任意模拟输出。
4) 禁止每路的模拟输出静音控制。
5) 如果禁止音量平滑(表75)，使音量缓升，每次一个寄存器台阶，从最小音量升至所要求的音量(增益)(该过程是表89示例的一部分)；如果使能音量平滑，则自动执行该过程，可单步设置音量(增益)。

尽管许多配置选项和设置可在器件工作($\overline{SHDN}$ = 1)时进行更改，但有些设置只能在器件处于关断($\overline{SHDN}$ = 0)时进行调节。表90列出了不应在工作期间进行更改的寄存器和位。如果在常规工作($\overline{SHDN}$ = 1)期间更改这些设置，会影响器件稳定性和性能指标。器件退出关断状态之前，全部外部时钟(主机模式下的MCLK，从机模式下的MCLK、LRCLK和BCLK)必须稳定运行。如果在器件常规工作(非关断状态)时使能或更改时钟，可能会产生相位误差和音频尖峰脉冲。

## 表89. 详细的器件启动顺序

| SEQUENCE | DESCRIPTION | REGISTERS |
|---|---|---|
| 1 | Set $\overline{SHDN}$ = 0 | 0x45 (Default POR State) |
| 2 | Configure Clocks (also enable all external clocks) | 0x1B to 0x21 |
| 3 | Configure Digital Audio Interface (DAI) | 0x22 to 0x25 |
| 4 | Configure Digital Signal processing (DSP) | 0x17 to 0x1A, 0x26 to 0x28, 0x33 to 0x36, 0x41 |
| 5 | Load Coefficients | 0x46 to 0xBD |
| 6 | Configure Power and Bias Mode | 0x42 to 0x44 |
| 7 | Configure Analog Mixers | 0x0D, 0x15, 0x16, 0x29, 0x2A, 0x2B, 0x2E, 0x2F, 0x37, 0x3A |
| 8 | Configure Analog Gain and Volume Controls. To Minimize Click and Pop for Analog Outputs, Enable Mute and Set the Output PGAs to the minimum gain setting. | 0x0E to 0x11, 0x2B to 0x2D, 0x30 to 0x32, 0x38, 0x39, 0x3B, 0x3C |
| 9 | Configure Miscellaneous Functions | 0x03, 0x12, 0x13, 0x14, 0x40 |
| 11 | Set $\overline{SHDN}$ = 1 (Power Up) | 0x45 |
| 10 | Enable Desired Functions | 0x3D to 0x3F |
| 11 | Disable Mute on Analog Output Drivers | 0x2C, 0x2D, 0x31, 0x32, 0x39, 0x3C |
| 12 | For all Analog Output Drivers, if Gain Smoothing is Disabled Ramp the Gain up One Volume Step per Write until the Desired Gain is Reached. If it is Enabled, Program the Desired Gain in a Single Step. | 0x30 to 0x32, 0x38, 0x39, 0x3B, 0x3C |

## 表90. 要求$\overline{SHDN}$ = 0时进行更改的寄存器

| DESCRIPTION | REGISTER |
|---|---|
| Clock Control and Quick Configuration Registers | 0x04 to 0x0B, 0x1B to 0x26 |
| DAC/ADC Enables (only these bits) | 0x3E, 0x3F |
| Bias/DAC/ADC Control | 0x42 to 0x44 |
| Digital Signal Processing Enables and Coefficients | 0x33 to 0x35, 0x41, 0x46 to 0xBD |
| Digital Microphone Configuration | 0x13, 0x14 |

## 元件选择

### 交流耦合电容

输入电容$C_{IN}$结合器件线路输入的阻抗，形成高通滤波器，消除模拟输入信号中的直流偏压。交流耦合电容允许放大器自动偏置至最优直流水平。如果源阻抗极低(相对)，高通滤波器的-3dB点由下式给出：

$$f_{-3dB} = \frac{1}{2\pi \times R_{IN} \times C_{IN}}$$

所选CIN的$f_{-3dB}$恰好低于有用信号的最低频率。为了获得最佳音质，使用具有低电压系数电介质的电容，例如钽电容或铝电解电容。具有高电压系数的电容，例如陶瓷电容，低频时可能会增大失真。如果需要，可采用类似的方式根据线路输出驱动器所连接的输出级的输入电阻计算线路输出交流耦合电容值。

### 电荷泵电容选择

选择ESR小于100mΩ的电容，以获得最佳性能。低ESR陶瓷电容最小化电荷泵的输出电阻。大多数表贴陶瓷电容满足ESR要求。为在扩展级温度范围内获得最佳性能，选择采用X7R电介质的电容。

飞电容(连接在C1N和C1P之间)的值影响电荷泵的输出电阻。太小的值影响器件提供足够电流驱动的能力，造成输出电压降低。增大飞电容的值则在一定程度上降低电荷泵的输出电阻。1µF以上，内部开关的导通电阻和外部电荷泵电容的ESR起主要作用。

保持电容(旁路HPVSS)值和ESR直接影响HPVSS处的纹波。增大电容值减小输出纹波。同样，降低ESR将减小纹波和输出电阻。在最大输出功率较低的系统中，可使用较小的电容值。更多信息请参见*典型工作特性*部分的输出功率和负载电阻关系图。

## 无滤波D类扬声器工作

传统的D类放大器需要外部滤波器从放大器输出中恢复音频信号。滤波器增加了系统成本并增大了方案尺寸，同时也会降低效率和THD+N性能。传统的PWM架构提供较大的差分输出摆幅(峰–峰值为2 x SPK_VDD)，并产生了较大的纹波电流。滤波元件中的任何寄生电阻都会造成功率损耗，降低效率。

如果应用(例如耳麦、衰减器等)中从驱动器到扬声器的走线较短且为低阻，器件无需输出滤波器。器件依靠扬声器线圈的固有电感以及扬声器和人耳的天然滤波特性从方波输出中恢复音频信号。由于省去了D类输出滤波器，使得方案尺寸更小、成本更低、效率更高。如果走线较长，且/或串联电阻/电感较高，可能就需要输出LC滤波器。这种情况下，如果负载的标称阻抗在整个音频波段内不为常数，可能需要佐贝尔(阻抗匹配)电路。

由于IC的输出频率恰好超出绝大多数扬声器的带宽，方波频率造成的音圈偏移非常小。尽管偏移很小，如果扬声器设计不能处理额外的功率，也有可能导致设备损坏。为优化性能，可选用串联电感大于10µH的扬声器。典型的8Ω扬声器，其串联电感通常在20µH至100µH范围内。

### EMI及可选磁珠滤波器

降低走线长度最小化辐射EMI。在PCB上，将SPKLP/SPKLN和SPKRP/SPKRN连接为差分线对，走线尽量短，这将减小走线环路面积，从而降低电路电感。如果在扬声器输出上使用滤波元件，将任何接地无源元件与SPK_GND的连接走线长度最小化，进一步减小EMI。

如果扬声器引线较长(超过约12in)，采用磁珠及接地电容的滤波器结构，可实现进一步EMI抑制(图55)。磁珠应具有低直流电阻、高频(> 600MHz)阻抗(100Ω至600Ω)，额定值至少为1A。电容值根据所选的磁珠及实际扬声器引线长度变化。根据EMI性能，选择小于1nF的电容。

## RF敏感度

GSM无线电利用时分多址(TDMA)以217Hz间隔发射，所产生的射频信号以217Hz进行强调幅，其谐波很容易被音频放大器解调。器件特别针对抑制射频信号进行了设计；然而，PCB布局对最终产品的敏感度影响很大。

射频应用中，布局及元件选择的改善可减小对射频噪声的敏感度，防止射频信号被解调为音频噪声。走线长度应保持短于相应射频波长的1/4。尽可能缩短走线长度，防止电路板走线形成天线并将射频信号耦合到器件内部。以米为单位的波长(λ)由下式给出：λ = c/f，其中c = 3 x $10^8$ m/s，f = 射频频率。

将音频信号布在PCB的中间层，使其上、下的接地区域将其屏蔽，防止射频干扰。理想情况下，PCB的顶层和底层应主要为接地区域，产生有效屏蔽。

由于电容的频率响应与陷波滤波器相似，所以利用电容的自谐频率可获得更大的射频抗扰性。根据制造商的不同，

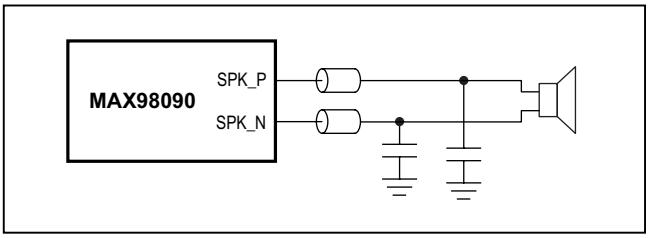



*图55. 可选D类磁珠EMI滤波器*

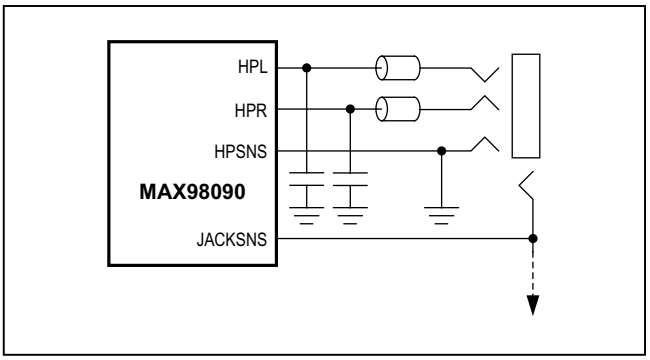



*图56. 可选H类输出RFI滤波器*

10pF至20pF电容通常在射频频率处呈现自谐。将这些电容安装在输入引脚时，可有效地将器件输入处的射频噪声短路至地。为了使这些电容有效工作，它们必须具有低阻、低感通路连接至接地区域。尽量避免使用微过孔连接至接地区域，因为这些过孔在射频频率下传导不良。在麦克风输出，通过使用带有接地电容的磁珠滤波器，可进一步提高RFI (图56)。

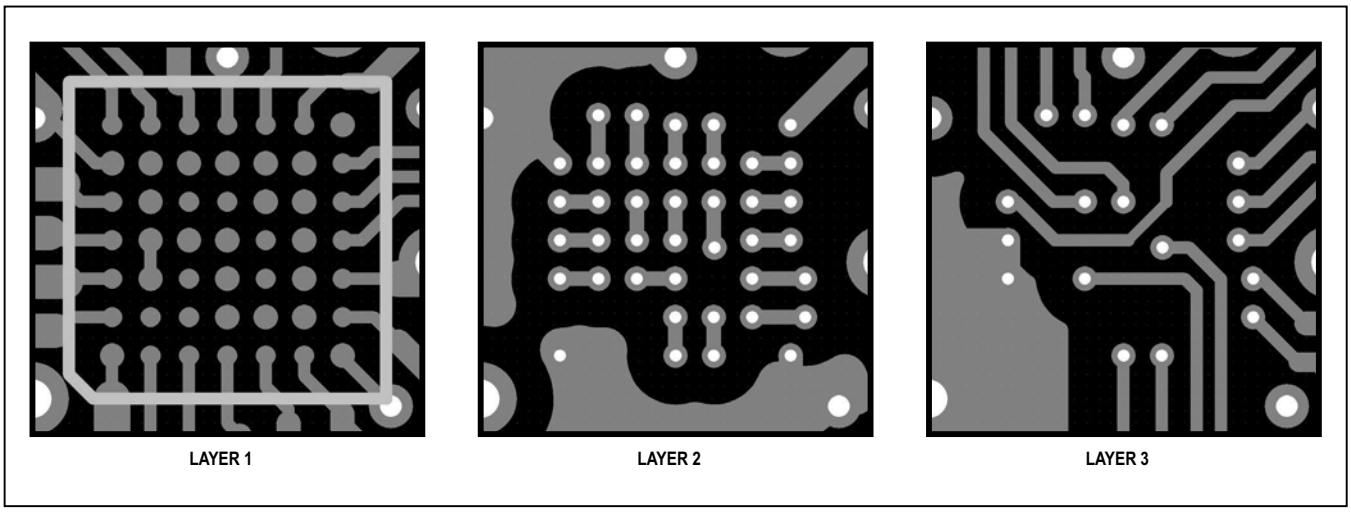



*图57. WLP封装的PCB连接示例*

## 电源旁路、布局和接地

适当的布局和接地对获得最佳性能至关重要。设计PCB布局时，适当的电路隔离可以将器件的模拟部分与数字部分分开。这样保证了模拟音频走线不会出现在数字走线附近。

在PCB的专用层上使用大面积连续接地层可以最小化环路面积。采用尽可能短的走线将AGND、DGND和HPGND直接连接至接地区域。适当的接地可改善音频性能、最大程度降低通道之间的串扰，并可防止数字噪声耦合至模拟音频信号。

以最短的走线长度将MICBIAS、BIAS和REF上的旁路电容直接连接至接地区域。还要确保连接至AGND的通路最短，将AVDD直接旁路至AGND。以最短的布线长度，将所有数字I/O端连接至DGND，DVDD和DVDDIO直接旁路至DGND。

使C1P和C1N之间的电容尽量靠近器件，以将C1P至C1N的走线长度降至最短。C1P和C1N之间增加的电感和电容降低耳机放大器的输出功率。利用电容旁路HPVDD、CPVDD和CPVSS，电容靠近引脚，采用短走线连接至HPGND。关闭CPVDD和CPVSS的去耦将电源纹波最小化、耳机放大器输出功率最大化。

HPSNS检测耳机插孔上的地噪声，并将相同噪声加至输出音频信号，从而使输出(耳机输出、地)无噪声。将HPSNS连接至耳机插孔屏蔽，确保精确检测耳机地噪声。

将SPK_VDD旁路至SPK_GND，走线尽量短；将SPKLP、SPKLN、SPKRP和SPKRN连接至立体声扬声器，走线尽量短。如果在扬声器输出上使用滤波元件，确保使其尽量靠近器件，以充分发挥这些器件的作用。

把麦克风至器件的麦克风信号以差分对方式布线，确保正和负信号尽可能靠近、并且具有相同的走线长度。当使用单端麦克风或其它单端音频源时，在尽量靠近音频源的位置将麦克风负输入接地，然后将正、负端走线作为差分对。

现备有一个评估板(EV kit)，可作为布局实例。利用该评估板可快速设置器件，并提供了易于使用的软件，用于控制其内部寄存器。

## 推荐的PCB布线

IC采用49焊球WLP封装。图57所示为如何利用3层PCB连接焊球的例子。为确保不断开地回路，利用第2层作为第1层和第3层之间的连接层或dog–bone层，并将其余区域作为覆铜接地区域。

### 不使用的引脚

表91列出了没有使用某些电路模块时，相应引脚的连接。如果系统噪声过大，或担心使能没有使用的模拟输入，可以将不使用的模拟音频输入交流耦合到AGND(如果元件成本和电路板面积允许)。

### WLP应用信息

关于WLP结构、尺寸、载带信息、PCB工艺、焊球布局以及推荐的回流温度特性的最新应用信息，以及可靠性测试结果的最新信息，请参见*应用笔记1891：晶片级封装(WLP)及其应用*。图58所示为器件使用的WLP焊球尺寸。

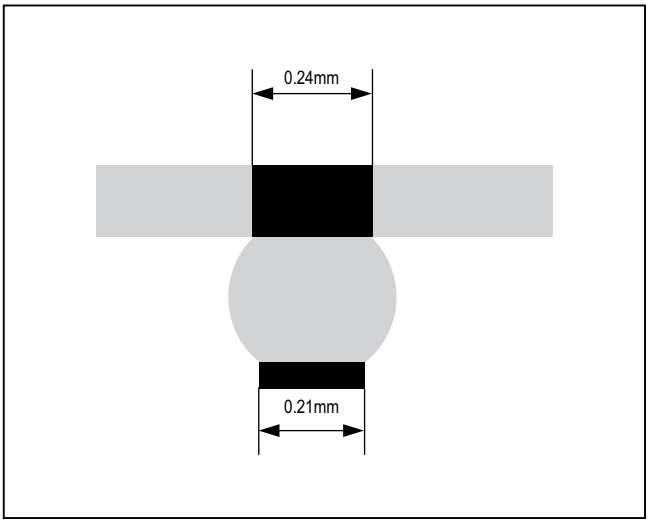



*图58. WLP封装焊球尺寸*

## 表91. 不使用的引脚连接

| PIN NAME | CONNECTION | PIN NAME | CONNECTION |
|---|---|---|---|
| **SUPPLY PLANES** | | **ANALOG AUDIO OUTPUTS** | |
| AVDD | Always connect | HPL | Unconnected |
| AGND | Always connect | HPR | Unconnected |
| HPVDD | Always connect | HPSNS | AGND |
| HPGND | Always connect | SPKLP | Unconnected |
| DVDD | Always connect | SPKLN | Unconnected |
| DVDDIO | Always connect | SPKRP | Unconnected |
| DGND | Always connect | SPKRN | Unconnected |
| SPKVDD | Always connect | RCVP / LOUTL | Unconnected |
| SPKLVDD | Always connect | RCVN / LOUTR | Unconnected |
| SPKRVDD | Always connect | **DIGITAL AUDIO INTERFACE** | |
| SPKLGND | Always connect | SDIN | DGND |
| SPKRGND | Always connect | SDOUT | Unconnected |
| **CHARGE PUMP** | | MCLK | Always connect |
| CPVDD | Unconnected | LRCLK | DGND |
| CPVSS | Unconnected | BCLK | DGND |
| C1P | Unconnected | **I²C INTERFACE** | |
| C1N | Unconnected | SCL | Always connect |
| **ANALOG AUDIO INPUTS** | | SDA | Always connect |
| IN1/DMD | Unconnected | $\overline{IRQ}$ | Unconnected |
| IN2/DMC | Unconnected | **OTHER** | |
| IN3 | Unconnected | MICBIAS | Unconnected |
| IN4 | Unconnected | JACKSNS | Unconnected |
| IN5 | Unconnected | BIAS | Always connect |
| IN6 | Unconnected | REF | Always connect |

# 超低功耗立体声音频编解码器

## 定购信息

| 器件 | 地址 | 温度范围 | 引脚–封装 |
|---|---|---|---|
| MAX98090AEWJ+T | 0x20 | -40°C至+85°C | 49 WLP |
| MAX98090AETL+T | 0x20 | -40°C至+85°C | 40 TQFN |
| MAX98090BEWJ+T | 0x22 | -40°C至+85°C | 49 WLP |
| MAX98090BETL+T | 0x22 | -40°C至+85°C | 40 TQFN |

*+表示无铅(Pb)/符合RoHS标准的封装。*

*T = 卷带包装*

## 芯片信息

PROCESS: CMOS

## 封装信息

如需最近的封装外形信息和焊盘布局(占位面积)，请查询**china.maximintegrated.com/packages**。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

| 封装类型 | 封装编码 | 外形编号 | 焊盘布局编号 |
|---|---|---|---|
| 49 WLP | W493B3+2 | **21-0443** | 参考 **应用笔记1891** |
| 40 TQFN | T4055+1 | **21-0140** | **90-0121** |

## 修订历史

| 修订号 | 修订日期 | 说明 | 修改页 |
|---|---|---|---|
| 0 | 1/13 | 最初版本。 | — |
| 1 | 8/13 | 更正部分错误。 | 1, 9, 11, 15 -17, 20 -26, 30, 37 -48, 50 -54, 56 -63, 66 -68, 72, 78, 79, 82, 84 -88, 91, 92, 94 -96, 98, 103 -105, 110, 113, 120, 121, 129, 141, 142, 146, 149, 150, 151, 158 -162, 164 |

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