

四通道PCI Express均衡器/转接驱动器

概述

MAX4950 PCI Express (PCIe®)四通道均衡器/转接驱动器工作在+3.3V单电源。该器件通过可编程输入均衡和可编程转接驱动电路提高了接收信号的完整性。输出电路能够恢复板上去加重损耗，用于补偿电路板损耗。该器件允许优化PCIe关键元件的布局，支持更长的带状线、微带线或电缆传输。

MAX4950包含四路相同的缓冲器，能够均衡速率高达5GT/s的差分信号，每个通道提供信号空闲和接收检测功能。MAX4950理想用于PCIe Gen I (2.5GT/s)和Gen II (5.0GT/s)数据速率，并具有省电模式。

MAX4950采用小尺寸、无铅、42引脚(3.5mm x 9.0mm) TQFN封装，便于优化布局并可满足最小空间要求，顺畅的电路板连线方便布线。MAX4950工作在0°C至+70°C温度范围。

应用

服务器
工业PC
测试设备
台式计算机
笔记本电脑(外置视频卡)
通信交换机
存储局域网

特性

- ◆ +3.3V单电源供电
- ◆ 支持I代(2.5GT/s)和II代(5.0GT/s)传输速率
- ◆ 回波损耗：
 - ≥ 10dB ($f \leq 1.25\text{GHz}$)
 - ≥ 8dB ($f \leq 2.5\text{GHz}$)
- ◆ 非常低的延时
 - 280ps传输延时
- ◆ 独立的通道检测
- ◆ 极低的通道间偏差：±50ps
- ◆ BER = 10^{-12} 时，总抖动 ≤ 35ps_{p-p}
- ◆ 三电平可编程输入均衡
- ◆ 三电平可编程输出去加重
- ◆ 片上50Ω输入/输出端接
- ◆ 所有引脚提供±2kV人体模式(HBM)静电保护
- ◆ 节省空间的3.5mm x 9.0mm、TQFN封装

订购信息

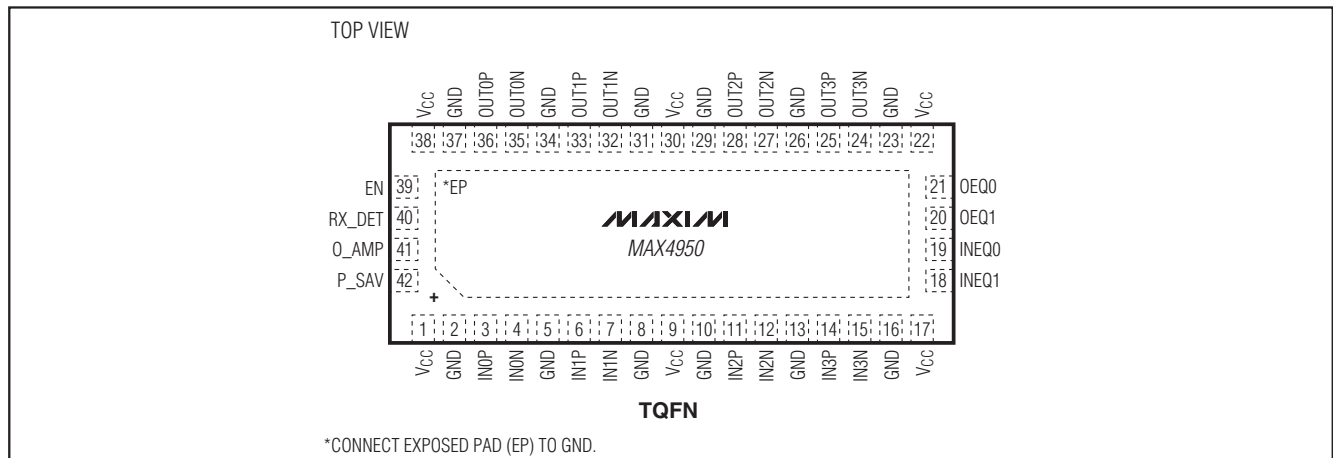
PART	TEMP RANGE	PIN-PACKAGE
MAX4950CTO+	0°C to +70°C	42 TQFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。

*EP = 裸焊盘。

PCIe是PCI-SIG组织的注册商标。

引脚配置



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ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V _{CC}	-0.3V to +4.0V
All Other Pins (Note 1).....	-0.3V to (V _{CC} + 0.3V)
Continuous Current IN _P and IN _N	±30mA
Peak Current IN _P and IN _N (pulsed for 1μs, 1% duty cycle).....	±100mA
Continuous Power Dissipation (T _A = +70°C) 42-Pin TQFN (derate 34.5mW/°C above +70°C)	2759mW

Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2)

42-Pin TQFN.....	2.0°C/W
Junction-to-Ambient Thermal Resistance (θ _{JA}) (Note 2) 42-Pin TQFN.....	29.0°C/W
Operating Temperature Range.....	0°C to +70°C
Storage Temperature Range.....	-65°C to +150°C
Junction Temperature.....	+150°C
Lead Temperature (soldering, 10s).....	+300°C

Note 1: All I/O pins are clamped by internal diodes.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com.cn/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE						
Power-Supply Range	V _{CC}		3.0		3.6	V
Supply Current	I _{CC}	O_AMP = GND, P_SAV = GND (Note 4)		262	328	mA
		EN = V _{CC} EN = GND		100	125	
Differential Input Impedance	Z _{RX-DIFF-DC}	DC	80	100	120	Ω
Differential Output Impedance	Z _{TX-DIFF-DC}	DC	80	100	120	Ω
Common-Mode Resistance to GND	Z _{RX-HIGH-IMP-DC-POS}	V _{IN_P} = V _{IN_N} = 0 to +200mV, input terminations not powered	50			kΩ
Common-Mode Resistance to GND	Z _{RX-HIGH-IMP-DC-NEG}	V _{IN_P} = V _{IN_N} = -150mV to 0, input terminations not powered	1			kΩ
Common-Mode Resistance to GND, Input Terminations Powered	Z _{RX-DC}	DC	40	50	60	Ω
Output Short-Circuit Current	I _{TX-SHORT}	Single-ended			90	mA
Common-Mode Delta Between Active and Idle States	V _{TX-CM-DC-ACTIVE-IDLE-DELTA}	O_AMP = GND			100	mV
DC Output Offset During Active State	V _{TX-CM-DC-LINE-DELTA}	I(V _{OUT_P} + V _{OUT_N})			25	mV
DC Output Offset During Electrical Idle	V _{TX-IDLE-DIFF-DC}	I(V _{OUT_P} + V _{OUT_N})			10	mV
AC PERFORMANCE (Note 5)						
Differential Input Return Loss	RL _{RX-DIFF}	f = 0.05GHz to 1.25GHz	10			dB
		f = 1.25GHz to 2.5GHz	8			
Common-Mode Input Return Loss	RL _{RX-CM}	f = 0.05GHz to 2.5GHz	6			dB

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Return Loss	RL-TX-DIFF	f = 0.05GHz to 1.25GHz	10			dB
		f = 1.25GHz to 2.5GHz	8			
Common-Mode Output Return Loss	RL-TX-CM	f = 0.05GHz to 2.5GHz	6			dB
Redriver Operation Differential Input Signal Range	V _{RX-DIFF-PP}	f = 0.05GHz to 2.5GHz	120		1200	mV _{P-P}
Full-Swing Differential Output Voltage (No Deemphasis)	V _{TX-DIFF-PP}	2 × I(V _{OUT_P} + V _{OUT_N}), O_AMP = GND; f = 500MHz	800	1000	1200	mV _{P-P}
Differential Output Voltage (Low Swing, No Deemphasis)	V _{TX-DIFF-PP-LOW}	2 × I(V _{OUT_P} + V _{OUT_N}), O_AMP = V _{CC} ; f = 500MHz	600	750	900	mV _{P-P}
Output Deemphasis Ratio, 0dB	V _{TX-DE-RATIO-0dB}	f = 2.5GHz, OEQ1 = GND, OEQ0 = GND; see Table 3		0		dB
Output Deemphasis Ratio, 3.5dB	V _{TX-DE-RATIO-3.5dB}	f = 2.5GHz, OEQ1 = GND, OEQ0 = V _{CC} ; see Table 3		3.5		dB
Output Deemphasis Ratio, 6dB	V _{TX-DE-RATIO-6dB}	f = 2.5GHz, OEQ1 = V _{CC} , OEQ0 = V _{CC} or GND; see Table 3		6		dB
Input Equalization, 0dB	V _{RX-EQ-0dB}	f = 2.5GHz, INEQ1 = GND, INEQ0 = GND; see Table 2 (Note 6)		0		dB
Input Equalization, 3.5dB	V _{RX-EQ-3.5dB}	f = 2.5GHz, INEQ1 = GND, INEQ0 = V _{CC} ; see Table 2 (Note 6)		3.5		dB
Input Equalization, 6dB	V _{RX-EQ-6dB}	f = 2.5GHz, INEQ1 = V _{CC} , INEQ0 = V _{CC} or GND; see Table 2 (Note 6)		6		dB
Output Common-Mode Voltage Swing Peak-to-Peak	V _{TX-CM-AC-PP}	Max(V _{OUT_P} + V _{OUT_N})/2 – Min(V _{OUT_P} + V _{OUT_N})/2			100	mV _{P-P}
Propagation Delay	T _{PD}	f = 2.5GHz, K28.7 pattern	160	280	400	ps
Rise/Fall Time	T _{TX-RISE-FALL}	(Note 7)	30			ps
Rise/Fall Time Mismatch	T _{TX-RF-MISMATCH}	(Note 7)			20	ps
Output Skew Same Pair	T _{SK}	f = 2.5GHz		10	15	ps
Output Skew Lane to Lane	T _{SKL}	f = 2.5GHz	-50		50	ps
Deterministic Jitter	T _{TX-DJ-DD}	K28.5 pattern, 5.0GT/s, AC-coupled, R _L = 50Ω, effects of deemphasis deembedded			15	ps _{P-P}
Random Jitter	T _{TX-RJ-DD}	K28.7 pattern, f > 1.5MHz, BER = 10 ⁻¹²			1.4	ps _{RMS}
Electrical Idle Entry Delay	T _{TX-IDLE-SET-TO-IDLE}	From input to output		15		ns
Electrical Idle Exit Delay	T _{TX-IDLE-TO-DIFF-DATA}	From input to output		8		ns

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Electrical Idle Detect Threshold	V _{TX-IDLE-THRESH}	Squarewave input at 500MHz	65	85	120	mV _{P-P}
Output Voltage During Electrical Idle (AC)	V _{TX-IDLE-DIFF-AC-P}	I(V _{OUT_P} - V _{OUT_N}), f = 2.5GHz			20	mV _{P-P}
Receiver Detect Pulse Amplitude	V _{TX-RCV-DETECT}	Voltage change in positive direction			600	mV
Receiver Detect Pulse Width				100		ns
Receiver Detect Retry Period				200		ns
CONTROL LOGIC (INEQ1, INEQ0, OEQ1, OEQ0, EN, RX_DET, O_AMP, P_SAV)						
Input Logic-Level Low	V _{IL}				0.6	V
Input Logic-Level High	V _{IH}		1.4			V
Input Logic Hysteresis	V _{HYST}			130		mV
Input Leakage Current	I _{IN}	V _{CONTROL_LOGIC} = +0.5V or +1.5V	-50		+50	μA
ESD PROTECTION						
All Pins		Human Body Model (HBM)		±2		kV

Note 3: All devices are 100% production tested at T_A = +70°C. Specifications for all temperature limits are guaranteed by design.

Note 4: Currents are applicable for both PCIe Generation I and Generation II speeds. Power-saving mode (P_SAV), where electrical idle and receiver detection are only performed on channel 0 and reduced output swing (O_AMP) reduces this current. Table 5 summarizes the predicted power consumption.

Note 5: Guaranteed by design, unless otherwise noted.

Note 6: Equivalent to same amount of deemphasis driving the input.

Note 7: Rise and fall times are measured using 20% and 80% levels.

时序图

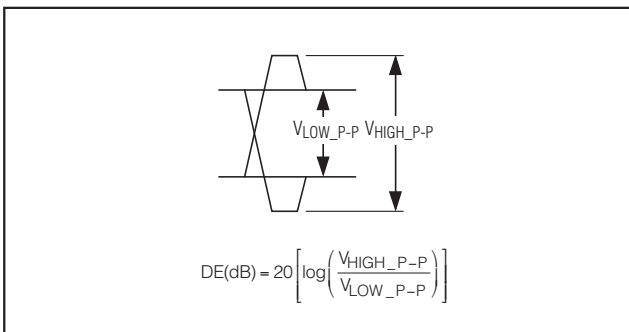


图1. 输出去加重示意图

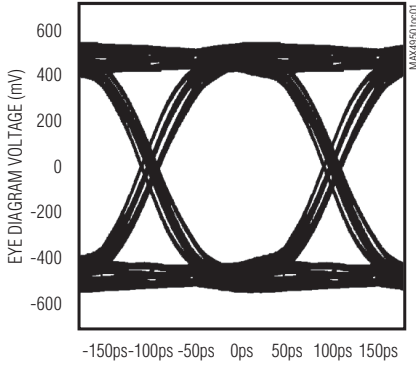
四通道PCI Express均衡器/转接驱动器

典型工作特性

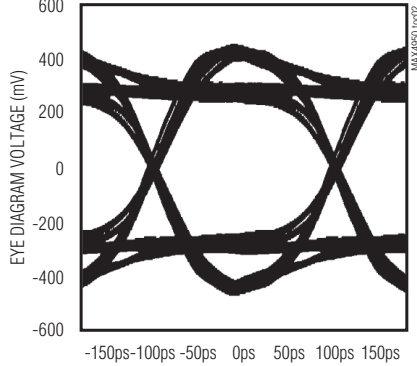
($V_{CC} = +3.3V$ and $T_A = +25^\circ C$, unless otherwise noted. All eye diagrams measured using K28.5 pattern.)

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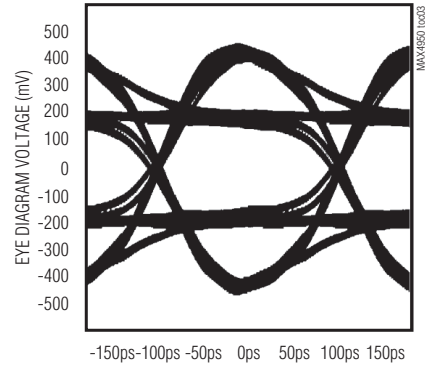
**INEQ0 = INEQ1 = 0, O_AMP = 0,
VIN = 200mVp-p, OEQ0 = 0, OEQ1 = 0**



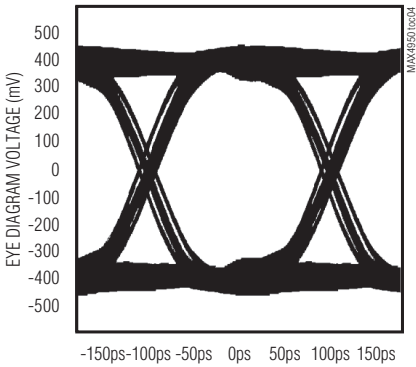
**INEQ0 = INEQ1 = 0, O_AMP = 0,
VIN = 200mVp-p, OEQ0 = 1, OEQ1 = 0**



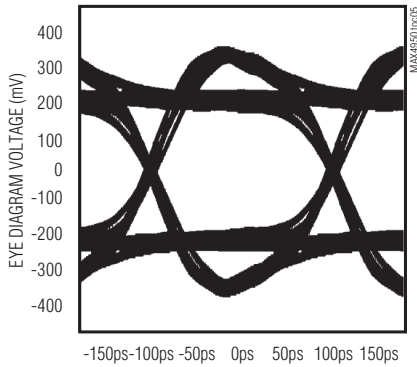
**INEQ0 = INEQ1 = 0, O_AMP = 0,
VIN = 200mVp-p, OEQ0 = 0, OEQ1 = 1**



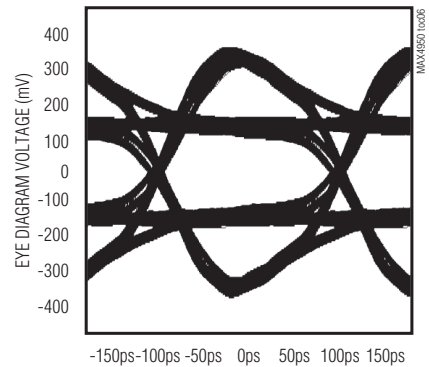
**INEQ0 = INEQ1 = 0, O_AMP = 1,
VIN = 200mVp-p, OEQ0 = 0, OEQ1 = 0**



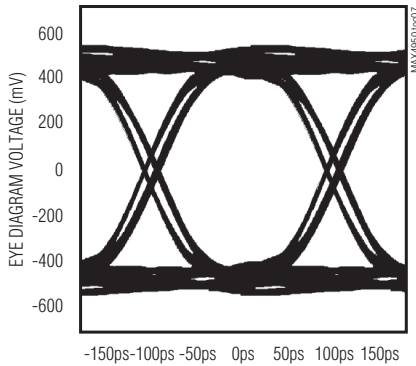
**INEQ0 = INEQ1 = 0, O_AMP = 1,
VIN = 200mVp-p, OEQ0 = 1, OEQ1 = 0**



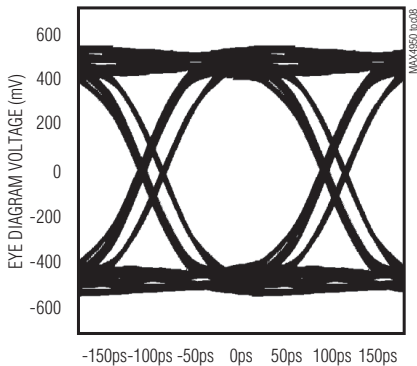
**INEQ0 = INEQ1 = 0, O_AMP = 1,
VIN = 200mVp-p, OEQ0 = 0, OEQ1 = 1**



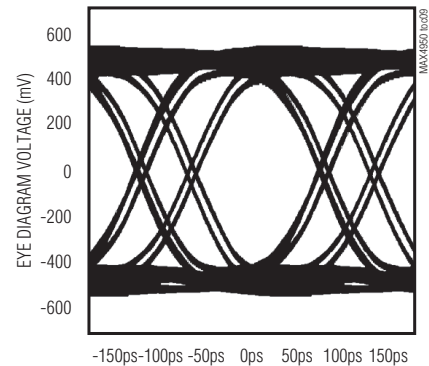
**INEQ0 = 1, INEQ1 = 0, O_AMP = 0, VIN = 500mVp-p,
WITH 6in. STRIPLINE OEQ0 = OEQ1 = 0**



**INEQ0 = 0, INEQ1 = 1, O_AMP = 0, VIN = 500mVp-p,
WITH 19in. STRIPLINE OEQ0 = OEQ1 = 0**



**INEQ0 = 0, INEQ1 = 0, O_AMP = 0, VIN = 500mVp-p,
WITH 19in. STRIPLINE OEQ0 = OEQ1 = 0**



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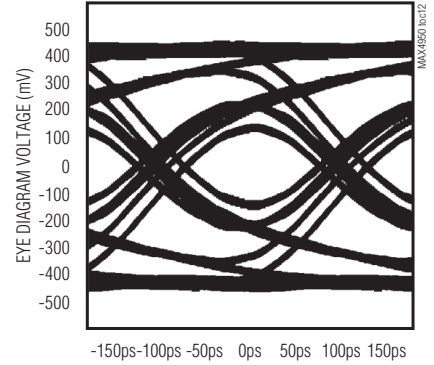
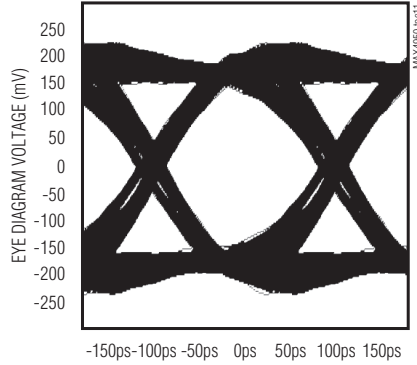
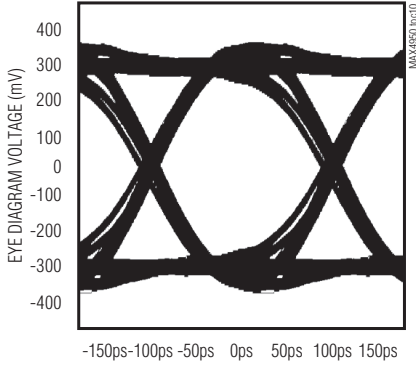
典型工作特性(续)

($V_{CC} = +3.3V$ and $T_A = +25^{\circ}C$, unless otherwise noted. All eye diagrams measured using K28.5 pattern.)

INEQ0 = INEQ1 = 0, O_AMP = 1, $V_{IN} = 200mV_{P-P}$,
OEQ0 = 1, OEQ1 = 0, OUTPUT AFTER 6IN. STRIPLINE

INEQ0 = INEQ1 = 0, O_AMP = 0, $V_{IN} = 200mV_{P-P}$,
OEQ0 = 0, OEQ1 = 1, OUTPUT AFTER 19IN. STRIPLINE

INEQ0 = INEQ1 = 0, O_AMP = 0, $V_{IN} = 200mV_{P-P}$,
OEQ0 = 0, OEQ1 = 0, OUTPUT AFTER 19IN. STRIPLINE



引脚说明

引脚	名称	功能
1, 9, 17, 22, 30, 38	VCC	电源输入端。采用1 μ F和0.01 μ F并联电容将VCC旁路至GND, 电容尽可能靠近器件放置。
2, 5, 8, 10, 13, 16, 23, 26, 29, 31, 34, 37	GND	地。
3	IN0P	同相输入0。
4	IN0N	反相输入0。
6	IN1P	同相输入1。
7	IN1N	反相输入1。
11	IN2P	同相输入2。
12	IN2N	反相输入2。
14	IN3P	同相输入3。
15	IN3N	反相输入3。
18	INEQ1	输入均衡控制MSB。INEQ1在内部通过60k Ω (典型值)电阻下拉, 参见表2。
19	INEQ0	输入均衡控制LSB。INEQ0在内部通过60k Ω (典型值)电阻下拉, 参见表2。
20	OEQ1	输出加重控制MSB。OEQ1在内部通过60k Ω (典型值)电阻下拉, 参见表3。
21	OEQ0	输出加重控制LSB。OEQ0在内部通过60k Ω (典型值)电阻下拉, 参见表3。
24	OUT3N	反相输出3。
25	OUT3P	同相输出3。
27	OUT2N	反相输出2。
28	OUT2P	同相输出2。

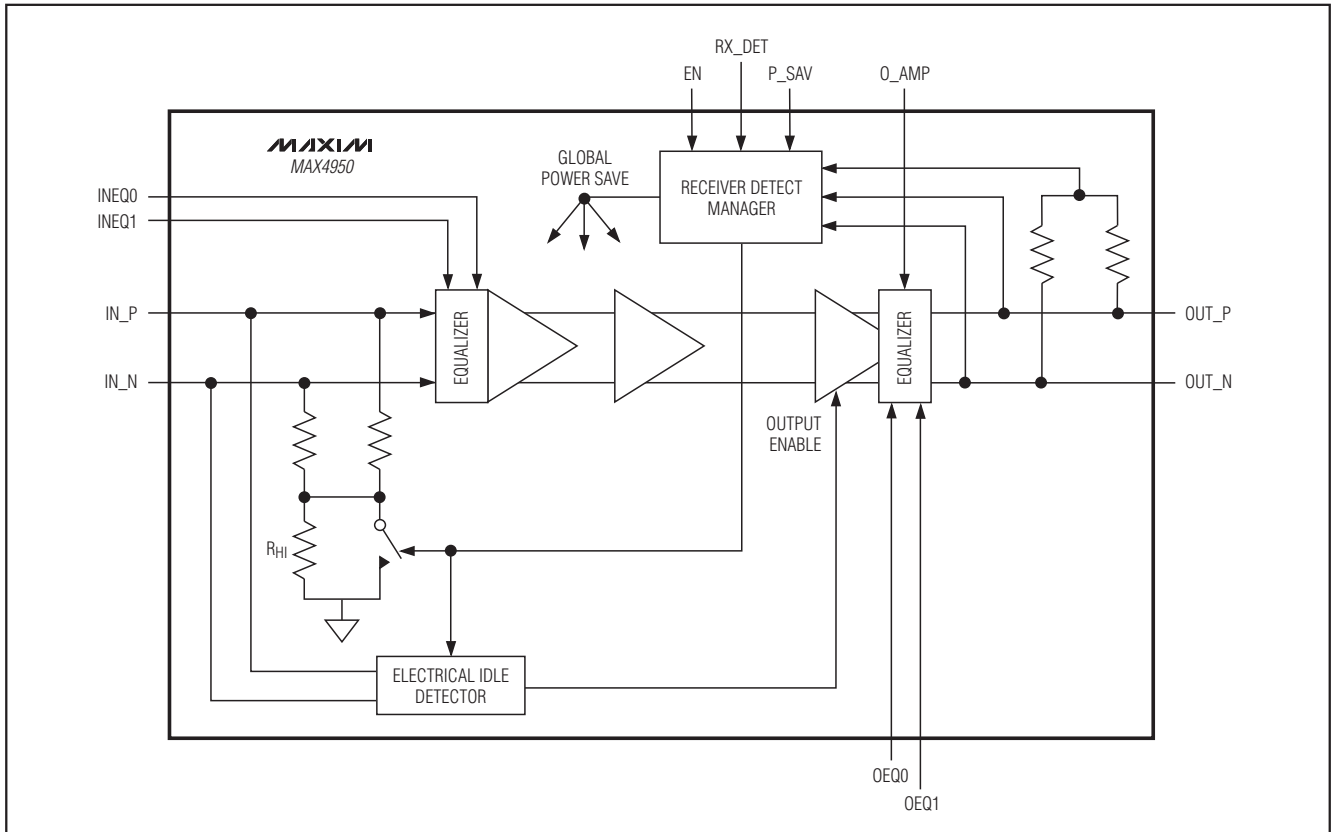
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引脚说明(续)

引脚	名称	功能
32	OUT1N	反相输出1。
33	OUT1P	同相输出1。
35	OUT0N	反相输出0。
36	OUT0P	同相输出0。
39	EN	使能输入。将EN驱动至低电平，进入待机模式；将EN驱动至高电平，进入正常工作模式。EN在内部通过60kΩ (典型值)电阻下拉。
40	RX_DET	接收器检测控制。将RX_DET驱动至高电平，启动接收检测；正常工作模式下，将RX_DET驱动至低电平。RX_DET在内部通过60kΩ (典型值)电阻下拉。
41	O_AMP	输出转接驱动选择输入。O_AMP在内部通过60kΩ (典型值)电阻下拉。
42	P_SAV	省电模式输入。P_SAV在内部通过60kΩ (典型值)电阻下拉，参见表6。
—	EP	裸焊盘。内部连接至GND，将EP连接至大面积地层以改善散热，EP不能用作电气接点。

功能框图



四通道PCI Express均衡器/转接驱动器

详细说明

MAX4950四通道均衡器/转接驱动器设计用于支持PCIe Gen I (2.5GT/s)和Gen II (5.0GT/s)数据速率。器件包含四路相同的驱动器，每个通道均提供信号空闲/接收检测功能，且具有均衡功能，用于补偿电路板损耗。通过可编程输入均衡电路提高接收信号的完整性。MAX4950输出级具有转接驱动输出摆幅选择输入O_AMP (表1)以及可编程输出去加重功能，用于优化PCIe关键元件的布局，支持更长的带状线、微带线或电缆传输。

可编程输入均衡

MAX4950具有可编程输入均衡功能，通过设置两个控制端INEQ1和INEQ0可提供0dB、3.5dB或6dB的高频提升(见表2)。

可编程输出去加重

MAX4950具有可编程输出去加重功能，通过设置两个控制端OEQ1和OEQ0可提供0dB、3.5dB或6dB的去加重比(见表3)。

接收检测

MAX4950每个通道均具有接收检测功能。初始上电时，如果EN为高电平，则启动接收检测功能。当EN为高电平时，还可通过RX_DET输入的上升沿启动接收检测功能。检测过程中，无论EN处于何种逻辑状态，器件均保持在低功耗待机模式并禁止输出。在某个通道检测到有效接收信号之前会重复接收检测。如果一个通道上检测到了有效接收信号，则其它通道的重复检测次数将限制为3次。根据接收检测的结果，使能通道输出和空闲检测。

注：对于缓慢上升的电源，推荐采用EN触发方式，以避免接收检测超时。

空闲检测

MAX4950具有空闲检测功能，以防止将噪声驱动到输出端。如果MAX4950检测到差分输入跌落至 $V_{TX-IDLE-THRESH}$ 以下，MAX4950将禁止输出；当差分输入信号高于 $V_{TX-IDLE-THRESH}$ 时，MAX4950将开启输出并对信号进行驱动。空闲和驱动模式下的输出共模电压有一点差异。

省电功能

MAX4950具有省电模式，可降低静态电源电流。省电模式下，关闭通道1、通道2和通道3的空闲检测和接收检测电路，所有通道操作受控于通道0。当所有通道保持同步工

表1. 输出转接驱动摆幅

O_AMP	DIFFERENTIAL OUTPUT VOLTAGE (mVp-p)
0	1000 (typ)
1	750 (typ)

表2. 输入均衡

INEQ1	INEQ0	INPUT EQUALIZATION (dB)
0	0	0 at 5.0GT/s
0	1	3.5 (typ) at 5.0GT/s
1	X	6 (typ) at 5.0GT/s

X = 无关。

表3. 输出去加重

OEQ1	OEQ0	OUTPUT DEEMPHASIS RATIO (dB)
0	0	0 at 5.0GT/s
0	1	3.5 (typ) at 5.0GT/s
1	X	6 (typ) at 5.0GT/s

X = 无关。

表4. 接收检测输入功能

RX_DET	EN	DESCRIPTION
X	0	Receiver Detection Inactive
0	1	Receiver Detection Inactive
Rising Edge	1	Initiate Receiver Detection
1	1	Following a Rising Edge, Indefinite Retry Until Receiver Detected

X = 无关。

作时，这一功能可有效降低功耗。常规工作模式下，所有通道具有独立的空闲和接收检测功能。将P_SAV驱动至高电平则进入省电模式；将P_SAV驱动至低电平，器件处于常规工作模式。不需要器件工作时，可以使用MAX4950的待机控制输入(EN)，进一步降低功耗。将EN驱动至低电平，器件将进入待机模式；将EN驱动至高电平则使能器件。表5所示为常规模式、省电模式和待机模式下采用不同驱动强度的典型功耗差异。

四通道PCI Express均衡器/转接驱动器

表5. 省电模式静态功耗

EN	P_SAV	O_AMP	QUIESCENT POWER SUPPLY CURRENT (typ) (mA)	QUIESCENT POWER SUPPLY CURRENT (max) (mA)	QUIESCENT POWER DISSIPATION (3.3V, typ) (mW)	QUIESCENT POWER DISSIPATION (3.6V, max) (mW)
0	0	0	100	125	330	450
0	0	1	80	100	264	360
0	1	0	100	125	330	450
0	1	1	80	100	264	360
1	0	0	262	328	865	1181
1	0	1	242	303	799	1091
1	1	0	214	268	706	965
1	1	1	194	243	640	875

应用信息

裸焊盘封装

图2所示为两片MAX4950的典型应用，两个器件均安装在主板上，可独立设置输入和输出均衡，以实现最佳性能。设置接收均衡器，通过两组连接器和微带传输线接收来自远端板卡的衰减信号。Rx输出仅具有小幅均衡或没有均衡。Tx部分提供高质量传输信号，并具有输出电压提升功能(去加重)。

带裸焊盘的42引脚、TQFN封装提供了一条低热阻通道，为IC散热。MAX4950的裸焊盘必须焊接到电路板的地层，以获得最佳散热。有关裸焊盘的更多信息，请参考Maxim应用笔记HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*。

布局

电源上电顺序

电路板布局和设计会显著影响MAX4950的性能。采用良好的高频设计技术，包括降低地回路的电感、数据信号采用阻抗受控的传输线。电源去耦器件应该尽可能靠近V_{CC}放置，V_{CC}始终连接至功率层。推荐将接收和发送引线放置在不同电路板层，以降低串扰。

警告：请勿超出最大额定参数，超出规定的额定值可能导致器件永久性损坏。

推荐所有器件采用适当的电源上电顺序。加载信号之前，应先接GND，然后接V_{CC}，特别是在信号不具有限流功能的情况下。

芯片信息

PROCESS: BiCMOS

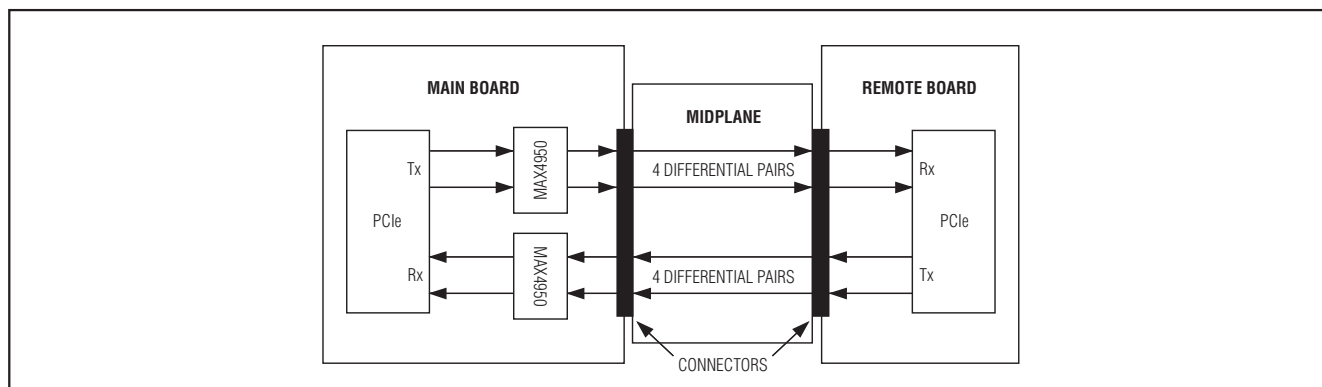


图2. 典型应用框图

四通道PCI Express均衡器/转接驱动器

封装信息

如需最近的封装外形信息和焊盘布局，请查询 www.maxim-ic.com.cn/packages。

封装类型	封装编码	文档编号
42 TQFN-EP	T423590+1	21-0181

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