19-4583; Rev 0; 4/09

双通道PCI Express均衡器/转接驱动器

概述

MAX4950A双通道PCI Express® (PCIe)均衡器/转接驱动器采用+3.3V单电源供电。该器件通过可编程输入均衡和具有输出去加重以补偿高频损耗的转接驱动电路，有效提高接收信号的完整性。该器件能够优化PCIe关键元件的布局，支持更长的带状线、微带线或电缆传输。

MAX4950A包含两个相同通道，用于均衡PCIe Gen I (2.5GT/s)和Gen II (5.0GT/s)信号。MAX4950A在每个通道都提供信号空闲和接收检测功能，并具有省电模式。

MAX4950A采用小尺寸36引脚(6.0mm x 6.0mm) TQFN封装，提供顺畅的电路板连线，进一步减小占用空间。MAX4950A工作在0°C至+70°C商业级温度范围。

应用

服务器

工业PC

测试设备

计算机

外置图形卡

通信交换机

存储局域网

PCI Express是PCI-SIG组织的注册商标。

特性

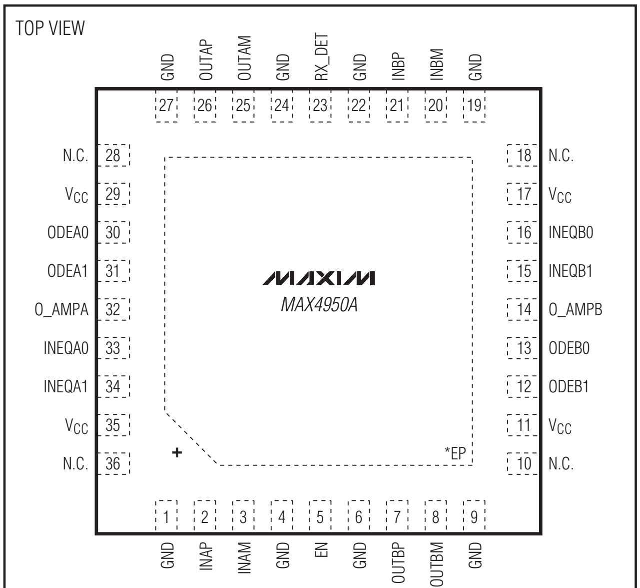
- +3.3V单电源供电
- 支持PCIe Gen I (2.5GT/s)和Gen II (5.0GT/s)电缆传输
  优异的差分回波损耗指标：
  ≥ 8dB (f = 1.25GHz至2.5GHz)
- 传输延时低至280ps (典型值)
- 独立的通道检测
- 三电平可编程输入均衡
- 三电平可编程输出去加重
- 标准的-2.5dB可编程输出电平
- 片上50Ω输入/输出端接
- 节省空间的6.0mm x 6.0mm、TQFN封装

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX4950ACTX+T	0°C to +70°C	36 TQFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。
**EP = 裸焊盘。*
T = 卷带包装。

引脚配置



TQFN

*CONNECT EXPOSED PAD (EP) TO GND.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC} ....-0.3V to +4.0V
All Other Pins (Note 1)................-0.3V to (V_{CC} + 0.3V)
Continuous Current IN_P, IN_M, OUT_P, OUT_M ....±30mA
Peak Current IN_P, IN_M, OUT_P, OUT_M
(pulsed for 1µs, 1% duty cycle)...........................±100mA
Continuous Power Dissipation (T_A = +70°C)
36-Pin TQFN (derate 35.7mW/°C above +70°C) 2857mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2)
36-Pin TQFN...1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 2)
36-Pin TQFN...28°C/W
Operating Temperature Range..........................0°C to +70°C
Junction Temperature Range ....-40°C to +150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: All I/O pins are clamped by internal diodes.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com.cn/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE						
Power-Supply Range	V_{CC}		3.0		3.6	V
Supply Current	I_{CC}	EN = V_{CC}, V_{O_AMPA} = V_{GND}, V_{O_AMPB} = V_{GND} (Note 4)		130	165	mA
Differential Input Impedance	$Z_{RX-DIFF-DC}$	DC	80	100	120	Ω
Differential Output Impedance	$Z_{TX-DIFF-DC}$	DC	80	100	120	Ω
Common-Mode Resistance to GND	$Z_{RX-HIGH-IMP-DC-POS}$	V_{IN_P} = V_{IN_M} = 0 to +200mV, input terminations not powered	50			kΩ
Common-Mode Resistance to GND	$Z_{RX-HIGH-IMP-DC-NEG}$	V_{IN_P} = V_{IN_M} = -150mV to 0, input terminations not powered	1			kΩ
Common-Mode Resistance to GND, Input Terminations Powered	Z_{RX-DC}		40	50	60	Ω
Output Short-Circuit Current	$I_{TX-SHORT}$	Single-ended			90	mA
Common-Mode Delta Between Active and Idle States	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	$V_{O\_AMP\_}$ = V_{GND}			100	mV
DC Output Offset During Active State	$V_{TX-CM-DC-LINE-DELTA}$	$\lvert V_{OUT\_P} - V_{OUT\_M} \rvert$			25	mV
DC Output Offset During Electrical Idle	$V_{TX-IDLE-DIFF-DC}$	$\lvert V_{OUT\_P} - V_{OUT\_M} \rvert$			10	mV
AC PERFORMANCE						
Differential Input Return Loss (Note 5)	$RL_{RX-DIFF}$	f = 0.05GHz to 1.25GHz	10			dB
		f = 1.25GHz to 2.5GHz	8			
Common-Mode Input Return Loss (Note 5)	RL_{RX-CM}	f = 0.05GHz to 2.5GHz	6			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Return Loss (Note 5)	$RL_{TX-DIFF}$	f = 0.05GHz to 1.25GHz	10			dB
		f = 1.25GHz to 2.5GHz	8			
Common-Mode Output Return Loss (Note 5)	RL_{TX-CM}	f = 0.05GHz to 2.5GHz	6			dB
Redriver-Operation Differential Input Signal Range	$V_{RX-DIFF-PP}$	f = 0.05GHz to 2.5GHz	120		1200	mV_{P-P}
Full-Swing No-Deemphasis Differential Output Voltage	$V_{TX-DIFF-PP}$	ABS|V_{OUT_P} - V_{OUT_M}|; O_AMP_ = GND	800	1000	1200	mV_{P-P}
Low-Swing No-Deemphasis Differential Output Voltage	$V_{TX-DIFF-PP-LOW}$	ABS|V_{OUT_P} - V_{OUT_M}|; O_AMP_ = V_{CC}	600	750	900	mV_{P-P}
Output Deemphasis Ratio, 0dB	$V_{TX-DE-RATIO-0dB}$	f = 2.5GHz, ODE_1 = GND, ODE_0 = GND, Figure 1 (see Table 3)		0		dB
Output Deemphasis Ratio, 3.5dB	$V_{TX-DE-RATIO-3.5dB}$	f = 2.5GHz, ODE_1 = GND, ODE_0 = V_{CC}, Figure 1 (see Table 3)		3.5		dB
Output Deemphasis Ratio, 6dB	$V_{TX-DE-RATIO-6dB}$	f = 2.5GHz, ODE_1 = V_{CC}, ODE_0 = V_{CC} or GND, Figure 1 (see Table 3)		6		dB
Input Equalization, 0dB (Note 6)	$V_{RX-EQ-0dB}$	f = 2.5GHz, INEQ_1 = GND, INEQ_0 = GND (see Table 2)		0		dB
Input Equalization, 3.5dB (Note 6)	$V_{RX-EQ-3.5dB}$	f = 2.5GHz, INEQ_1 = GND, INEQ_0 = V_{CC} (see Table 2)		3.5		dB
Input Equalization, 6dB (Note 6)	$V_{RX-EQ-6dB}$	f = 2.5GHz, INEQ_1 = V_{CC}, INEQ_0 = V_{CC} or GND (see Table 2)		6		dB
Output Common-Mode Voltage	$V_{TX-CM-AC-PP}$	MAX(V_{OUT_P} + V_{OUT_M})/2 - MIN(V_{OUT_P} + V_{OUT_M})/2			100	mV_{P-P}
Propagation Delay (Note 5)	T_{PD}	f = 2.5GHz	160	280	400	ps
Rise/Fall Time	$T_{TX-RISE-FALL}$	(Note 7)	30			ps
Rise/Fall Time Mismatch	$T_{TX-RF-MIISMATCH}$	(Note 7)			20	ps
Same-Pair Output Skew (Note 5)	T_{SK}	f = 2.5GHz		10	15	ps
Lane-to-Lane Output Skew (Note 5)	T_{SKL}	f = 2.5GHz	-50		+50	ps
Deterministic Jitter (Note 5)	$T_{TX-DJ-DD}$	K28.5± pattern, 5.0GT/s, AC coupled, R_L = 50Ω, effects of deemphasis deembedded			15	ps_{P-P}
Random Jitter	$T_{TX-RJ-DD}$	DIO.2 pattern			1.4	ps_{RMS}
Electrical Idle Entry Delay	$T_{TX-IDLE-SET-TO-IDLE}$	From input to output		15		ns
Electrical Idle Exit Delay	$T_{TX-IDLE-TO-DIFF-DATA}$	From input to output		12		ns

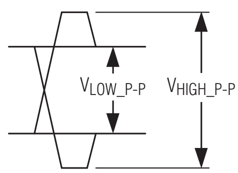
ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 75nF coupling capacitor on each output, R_L = 50Ω resistor on each output, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Electrical Idle Detect Threshold	$V_{TX-IDLE-THRESH}$		65	95	120	mV_{P-P}
Output Voltage During Electrical Idle (AC)	$V_{TX-IDLE-DIFF-AC-P}$	ABS|V_{OUT_P} - V_{OUT_M}|, f = 500MHz			25	mV_{P-P}
Receiver Detect Pulse Amplitude (Note 5)	$V_{TX-RCV-DETECT}$	Voltage change in positive direction			600	mV
Receiver Detect Pulse Width				100		ns
Receiver Detect Retry Period				200		ns
CONTROL LOGIC (INEQ_1, INEQ_0, ODE_1, ODE_0, EN, RX_DET, O_AMP_)						
Input Logic-Level Low	V_{IL}				0.6	V
Input Logic-Level High	V_{IH}		1.4			V
Input Logic Hysteresis	V_{HYST}			130		mV
Input Leakage Current	I_{IN}	$V_{CONTROL\_LOGIC}$ = +0.5V or +1.5V	-50		+50	µA

Note 3: All devices are 100% production tested at T_A = +70°C. Specifications for all temperature limits are guaranteed by design.
Note 4: Currents are applicable for both PCIe Generation I and Generation II speeds. Table 5 summarizes the predicted power consumption.
Note 5: Guaranteed by design, unless otherwise noted.
Note 6: Equivalent to the same amount of deemphasis driving the output.
Note 7: Rise and fall times are measured using 20% and 80% levels.

时序图



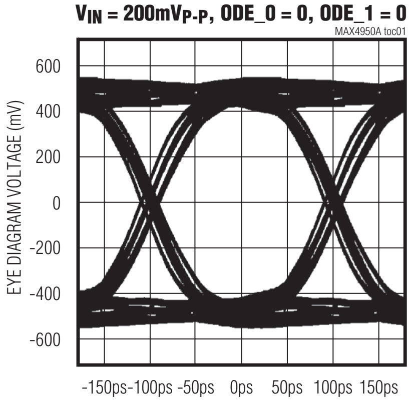
$$PE(dB) = 20\left[\log\left(\frac{V_{HIGH\_P-P}}{V_{LOW\_P-P}}\right)\right]$$

图1. 输出去加重示例

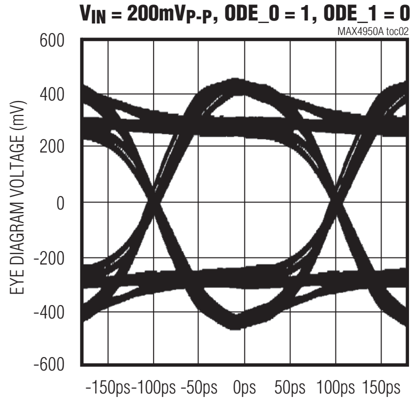
典型工作特性

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

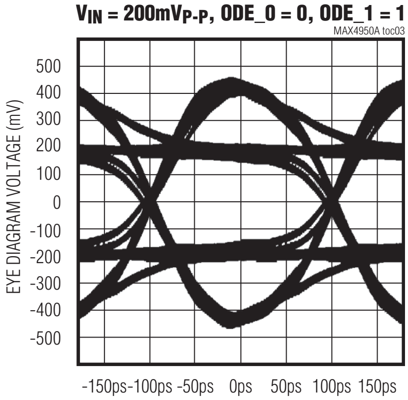
INEQ_0 = INEQ_1 = 0, O_AMP_ = 0,
V_{IN} = 200mV$_{P-P}$, ODE_0 = 0, ODE_1 = 0



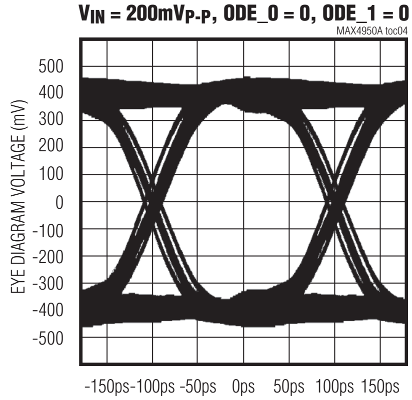
INEQ_0 = INEQ_1 = 0, O_AMP_ = 0,
V_{IN} = 200mV$_{P-P}$, ODE_0 = 1, ODE_1 = 0



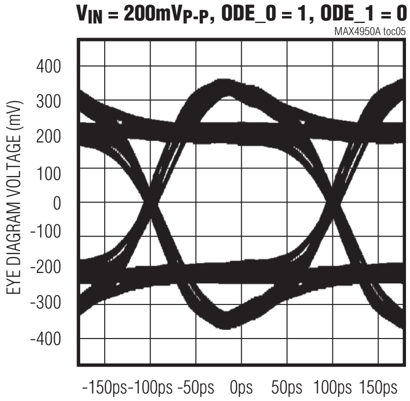
INEQ_0 = INEQ_1 = 0, O_AMP_ = 0,
V_{IN} = 200mV$_{P-P}$, ODE_0 = 0, ODE_1 = 1



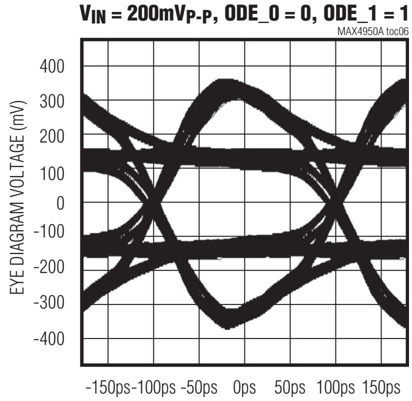
INEQ_0 = INEQ_1 = 0, O_AMP_ = 1,
V_{IN} = 200mV$_{P-P}$, ODE_0 = 0, ODE_1 = 0



INEQ_0 = INEQ_1 = 0, O_AMP_ = 1,
V_{IN} = 200mV$_{P-P}$, ODE_0 = 1, ODE_1 = 0



INEQ_0 = INEQ_1 = 0, O_AMP_ = 1,
V_{IN} = 200mV$_{P-P}$, ODE_0 = 0, ODE_1 = 1

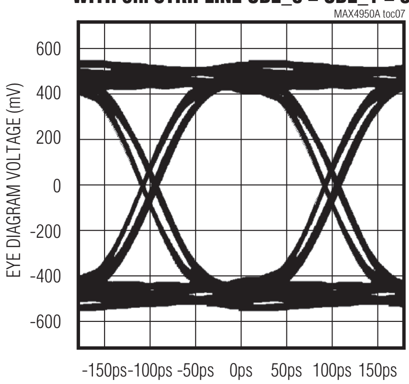


双通道PCI Express均衡器/转接驱动器

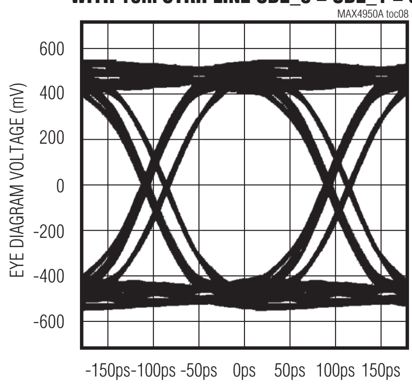
典型工作特性(续)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

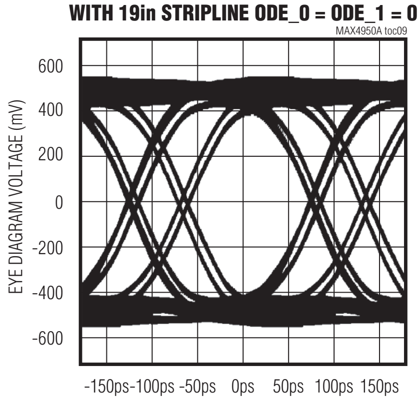
INEQ_0 = 1, INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 500mV$_{P-P}$, WITH 6in STRIPLINE ODE_0 = ODE_1 = 0



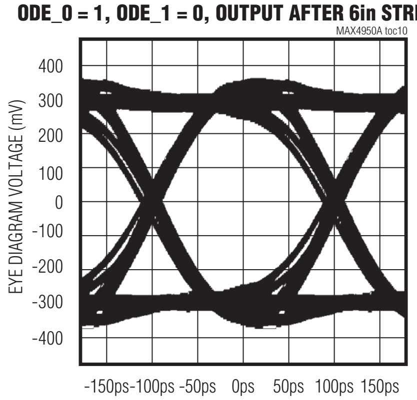
INEQ_0 = 0, INEQ_1 = 1, O_AMP_ = 0, V_{IN} = 500mV$_{P-P}$, WITH 19in STRIPLINE ODE_0 = ODE_1 = 0



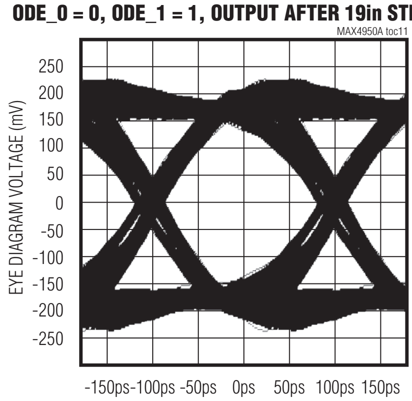
INEQ_0 = INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 500mV$_{P-P}$, WITH 19in STRIPLINE ODE_0 = ODE_1 = 0



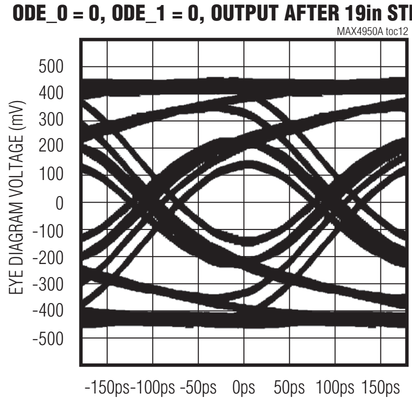
INEQ_0 = INEQ_1 = 0, O_AMP_ = 1, V_{IN} = 200mV$_{P-P}$, ODE_0 = 1, ODE_1 = 0, OUTPUT AFTER 6in STRIPLINE



INEQ_0 = INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 200mV$_{P-P}$, ODE_0 = 0, ODE_1 = 1, OUTPUT AFTER 19in STRIPLINE



INEQ_0 = INEQ_1 = 0, O_AMP_ = 0, V_{IN} = 200mV$_{P-P}$, ODE_0 = 0, ODE_1 = 0, OUTPUT AFTER 19in STRIPLINE



引脚说明

引脚	名称	功能
1, 4, 6, 9, 19, 22, 24, 27	GND	地。
2	INAP	同相输入A。
3	INAM	反相输入A。
5	EN	使能输入。将EN驱动至低电平，进入待机模式；将EN驱动至高电平，进入正常工作模式。EN在内部通过50kΩ (典型值)电阻下拉。
7	OUTBP	同相输出B。
8	OUTBM	反相输出B。
10, 18, 28, 36	N.C.	浮空，内部没有连接。
11, 17, 29, 35	V_{CC}	电源输入，采用1μF和0.01μF并联电容将V_{CC}旁路至GND，并尽可能靠近器件放置。
12	ODEB1	输出B去加重控制MSB，ODEB1在内部通过50kΩ (典型值)电阻下拉，参见表3。
13	ODEB0	输出B去加重控制LSB，ODEB0在内部通过50kΩ (典型值)电阻下拉，参见表3。
14	O_AMPB	输出B幅度选择输入，O_AMPB在内部通过50kΩ (典型值)电阻下拉。
15	INEQB1	输入B均衡控制MSB，INEQB1在内部通过50kΩ (典型值)电阻下拉，参见表2。
16	INEQB0	输入B均衡控制LSB，INEQB0在内部通过50kΩ (典型值)电阻下拉，参见表2。
20	INBM	反相输入B。
21	INBP	同相输入B。
23	RX_DET	接收检测控制。触发RX_DET将启动接收检测。RX_DET在内部通过50kΩ (典型值)电阻下拉。
25	OUTAM	反相输出A。
26	OUTAP	同相输出A。
30	ODEA0	输出A去加重控制LSB，ODEA0在内部通过50kΩ (典型值)电阻下拉，参见表3。
31	ODEA1	输出A去加重控制MSB，ODEA1在内部通过50kΩ (典型值)电阻下拉，参见表3。
32	O_AMPA	输出A幅度选择输入，O_AMPA在内部通过50kΩ (典型值)电阻下拉。
33	INEQA0	输入A均衡控制LSB，INEQA0在内部通过50kΩ (典型值)电阻下拉，参见表2。
34	INEQA1	输入A均衡控制MSB，INEQA1在内部通过50kΩ (典型值)电阻下拉，参见表2。
—	EP	裸焊盘。内部连接至GND，将EP连接至大面积地层以改善散热，EP不能用作电气接点。

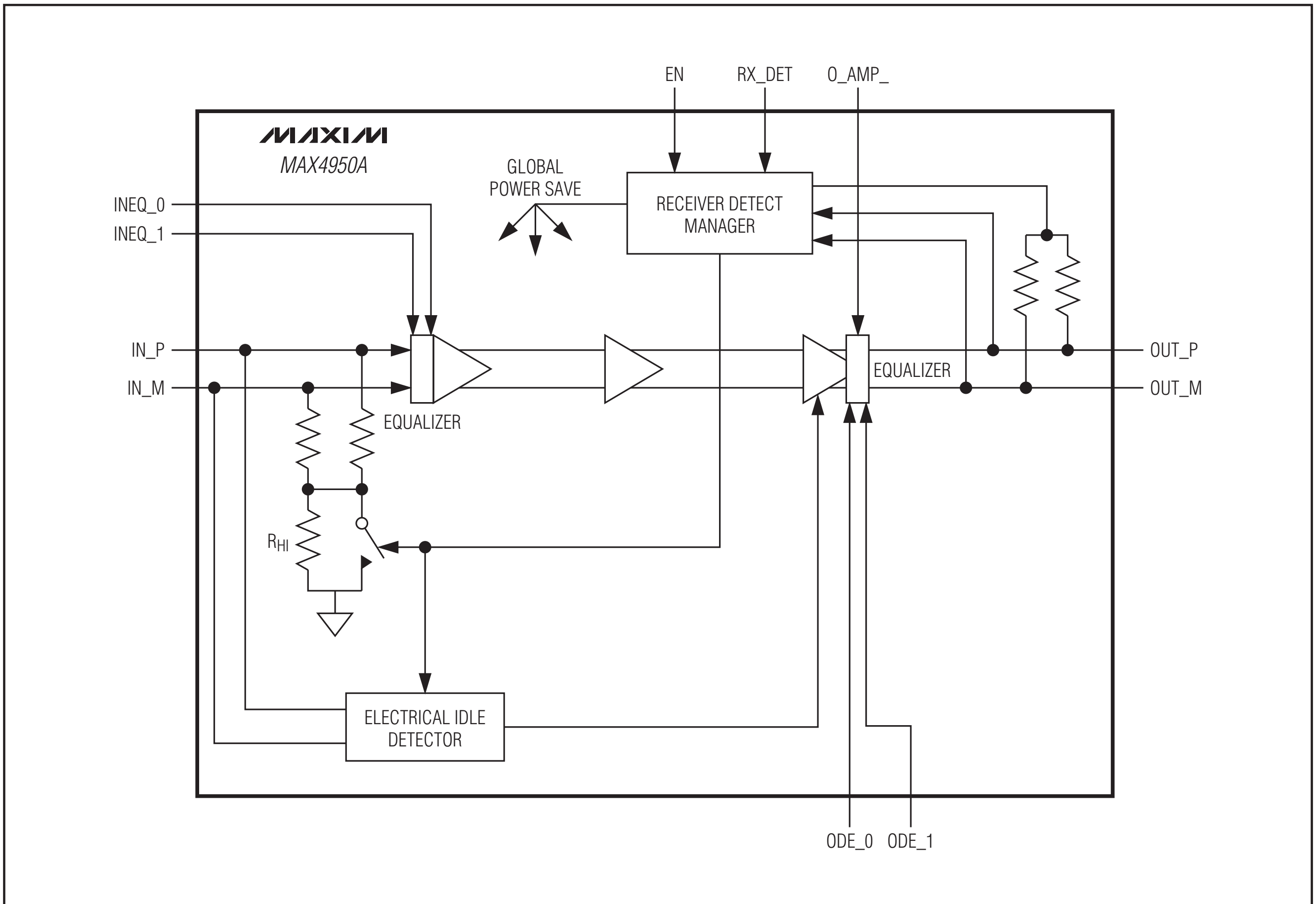

EN
RX_DET
O_AMP_
MAX4950A
GLOBAL POWER SAVE
RECEIVER DETECT MANAGER
INEQ_0
INEQ_1
IN_P
IN_M
EQUALIZER
EQUALIZER
OUT_P
OUT_M
R_{HI}
ELECTRICAL IDLE DETECTOR
ODE_0
ODE_1

图2. 每个通道的方框图

详细说明

MAX4950A双通道均衡器/转接驱动器设计用于支持Gen I (2.5GT/s)和Gen II (5.0GT/s) PCIe数据速率。器件包含两路相同的驱动器，每个通道均提供信号空闲/接收检测功能，并具有均衡功能，用于补偿电路板损耗。通过可编程输入均衡电路提高接收信号的完整性。MAX4950A的每个通道都具有输出幅度选择输入O_AMPA和O_AMPB (表1)以及可编程输出去加重功能，能够优化PCIe关键元件的布局，支持更长的带状线、微带线或电缆传输。

表1. 输出幅度选择

O_AMPA/ O_AMPB	DIFFERENTIAL OUTPUT VOLTAGE (mV_{P-P})
0	1000 (typ)
1	750 (typ)

可编程输入均衡

MAX4950A具有可编程输入均衡功能，能够为每个通道提供0dB、3.5dB或6dB的高频提升(见表2)。

表2. 输入均衡

INEQ_1	INEQ_0	INPUT EQUALIZATION (dB)
0	0	0
0	1	3.5 (typ)
1	X	6 (typ)

X = 无关。

可编程输出去加重

MAX4950A在每个通道均具有可编程输出去加重功能，通过设置两个控制端ODE_1和ODE_0提供0dB、3.5dB或6dB的去加重比(见表3)。

表3. 输出去加重

ODE_1	ODE_0	OUTPUT DEEMPHASIS RATIO (dB)
0	0	0
0	1	3.5 (typ)
1	X	6 (typ)

X = 无关。

接收检测

MAX4950A的每个通道均具有接收检测功能。初始上电时，如果EN为高电平，则启动接收检测功能。当EN为高电平时，还可通过RX_DET输入的上升沿或下降沿启动接收检测功能。检测过程中，无论EN是否处于逻辑高电平，器件均保持在低功耗待机模式并禁止输出。开启接收检测后，将在每个通道重复进行。一旦某个通道检测到了有效接收信号，则在另一通道进行最多三次检测。根据接收检测的结果，使能通道输出和空闲检测(见表4)。

表4. 接收检测输入功能

RX_DET	EN	DESCRIPTION
X	0	Receiver detection inactive
0	1	Following a rising or falling edge, indefinite retry until receiver detected
Rising or Falling Edge	1	Initiate receiver detection
1	1	Following a rising or falling edge, indefinite retry until receiver detected

X = 无关。

空闲检测

MAX4950A具有空闲检测功能，以防止将噪声驱动到输出端。如果MAX4950A检测到差分输入跌落至$V_{TX-IDLE-THRESH}$以下，MAX4950A将禁止输出；当差分输入信号高于$V_{TX-IDLE-THRESH}$时，MAX4950A将开启输出并对信号进行驱动。

省电功能

MAX4950A具有使能输入(EN)，用于关断器件、降低电源电流。将EN驱动至低电平时，器件进入关断模式；将EN置于高电平时则使能器件。正常工作时，通过降低通道输出幅度也可以降低电源电流。表5所示为关断模式、正常工作模式下不同输出驱动强度的典型功耗差异。

双通道PCI Express均衡器/转接驱动器

表5. 均衡和去加重电路的静态功耗

EN	O_AMPB	O_AMPA	QUIESCENT POWER SUPPLY CURRENT (typ) (mA)	QUIESCENT POWER SUPPLY CURRENT (max) (mA)	QUIESCENT POWER DISSIPATION (3.3V, typ) (mW)	QUIESCENT POWER DISSIPATION (3.6V, max) (mW)
0	0	0	60	75	198	270
0	0	1	55	68	182	243
0	1	0	55	68	182	243
0	1	1	50	60	165	216
1	0	0	130	165	429	594
1	0	1	125	157	413	565
1	1	0	125	157	413	565
1	1	1	120	150	396	540

应用信息

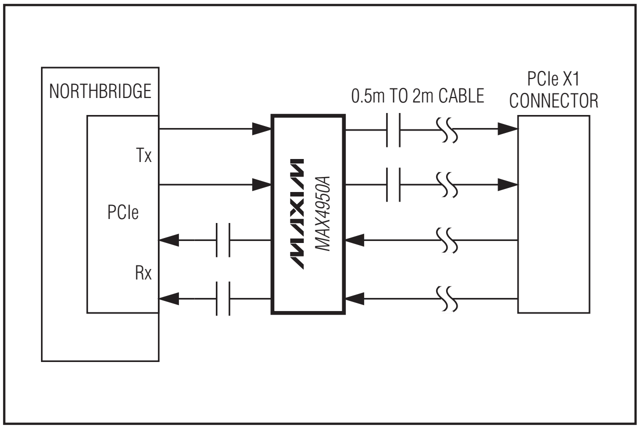


图3. 典型应用电路——MAX4950A用作X1通道电缆驱动器

布局

电路板布局和设计会显著影响MAX4950A的性能。采用良好的高频设计技术，包括降低地回路的电感、数据信号采用阻抗受控的传输线。推荐将接收和发送引线放置在不同电路板层以降低串扰，电源去耦电容应该尽可能靠近V_{CC}放置，V_{CC}连接至电源层。

裸焊盘封装

带裸焊盘的36引脚、TQFN封装提供了一条低热阻通道，为IC散热。MAX4950A的裸焊盘必须焊接到电路板的地层，以获得最佳散热。有关裸焊盘封装的更多信息，请参考Maxim应用笔记HFAN-08.1：*Thermal Considerations of QFN and Other Exposed-Paddle Packages*。

电源上电顺序

警告：请勿超出最大额定参数，因为超出规定的额定值可能导致器件永久性损坏。

推荐所有器件采用适当的电源上电顺序。加载信号之前，应先接GND然后接V_{CC}，特别是在信号不具有限流功能的情况下。

芯片信息

PROCESS: BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局，请查询**www.maxim-ic.com.cn/packages**。

封装类型	封装编码	文档编号
36 TQFN	T3666+2	21-0141

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