19-0222; Rev 0; 5/05

可提供评估板

完备的450MHz正交发送器

MAX2370

概述

MAX2370是用于450MHz系统、高度集成的正交发射芯片。该器件收到差分I/Q基带输入信号后，经由正交调制器和IF可变增益放大器 (VGA)，将其上变频至中频 (IF)。然后，信号被送入外部IF滤波器，经由镜频抑制混频器和RF VGA上变频至RF。片上功率放大器 (PA) 驱动电路对信号进行放大。IF合成器、RF合成器、本振缓冲器和SPI™/QSPI™/MICROWIRE™兼容的3线可编程总线组成了该IC的完备功能模块。

MAX2370采用48引脚TQFN封装，带有裸焊盘，工作在扩展工业级温度范围 (-40°C至+85°C)。

应用

450MHz CDMA/WCDMA电话

OFDM、cdma2000®、WCDMA、NMT

无线数据链路

SPI和QSPI是Motorola, Inc.的商标。
MICROWIRE是National Semiconductor Corp.的商标。
cdma2000是无线电通信协会的注册商标。

特性

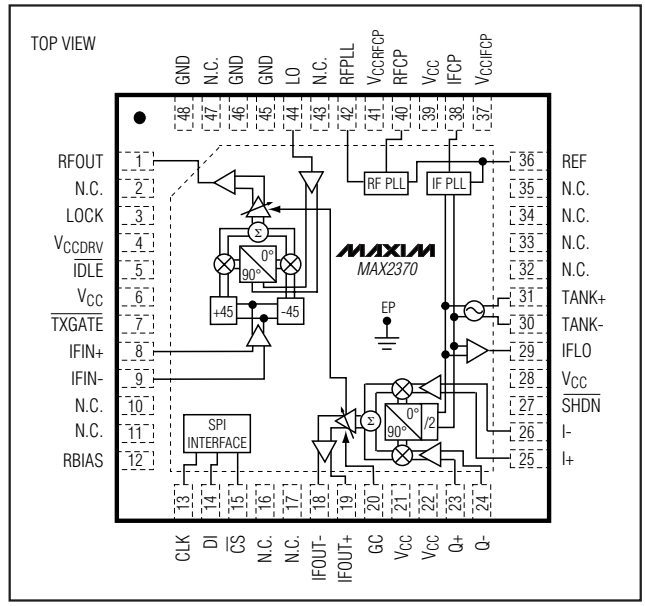
- ◆ 450MHz工作频率
- ◆ +8dBm输出功率
  - ±885kHz频偏时，ACPR典型值为-64dBc
  - ±1.125MHz频偏时，ACPR典型值为-66dBc
- ◆ 100dB功率控制范围
- ◆ 为RF和IF本振提供双路合成器
- ◆ SPI/QSPI/MICROWIRE兼容的3线接口总线
- ◆ 单边带上变频器
- ◆ 直接驱动外部功率放大器

定购信息

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX2370ETM	-40°C to +85°C	48 Thin QFN-EP* (7mm x 7mm)	T4877-3
MAX2370ETM+	-40°C to +85°C	48 Thin QFN-EP* (7mm x 7mm)	T4877+3

**EP = 裸焊盘。*
+ 表示无铅封装。

引脚配置/功能框图



ABSOLUTE MAXIMUM RATINGS

V_{CC}, RFOUT, V_{CCIFCP}, V_{CCRFCP}, V_{CCDRV} to GND .....-0.3V to +3.6V
DI, SCLK, $\overline{CS}$, GC, $\overline{SHDN}$, $\overline{TXGATE}$, $\overline{IDLE}$, LOCK to GND .....-0.3V to (V_{CC} + 0.3V)
AC Input Pins (IFIN_, Q_, I_, TANK_, REF, RFPLL, LO) to GND .....1V Peak
Digital Input Current ($\overline{SHDN}$, $\overline{TXGATE}$, $\overline{IDLE}$, SCLK, DI, $\overline{CS}$) .....±10mA

Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN (derate 38.5mW/°C above +70°C).....3077mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.3V, $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = high, V_{GC} = 2.5V, R_{BIAS} = 10kΩ, registers set according to Table 1, f_{REF} = 19.2MHz, no AC signals applied, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	2.7		3.3	V
Operating Supply Current	V_{GC} = 0.6V		53	79	mA
	V_{GC} = 1.95V		57	87	
	P_{RFOUT} = +5.5dBm, IFG[2:0] = 011		118		
	P_{RFOUT} = +8dBm, IFG[2:0] = 011		134		
	Addition for IFLO buffer		3.4	7.7	
	$\overline{IDLE}$ = low		6	10	
	$\overline{TXGATE}$ = low		5	7	
Sleep-Mode Supply Current	$\overline{SHDN}$ = 0V		0.5	20	µA
Logic-High Voltage		0.7 x V_{CC}			V
Logic-Low Voltage				0.3 x V_{CC}	V
Logic Input Current		-5		+5	µA
GC Input Current	V_{GC} = 0.5V to 2.5V		3.3	5	µA
GC Input Current During Shutdown	$\overline{SHDN}$ = low, V_{GC} = 2.5V		7	11	µA
Lock Indicator High Voltage (Locked)	47kΩ pullup load	V_{CC} - 0.4V			V
Lock Indicator Low Voltage (Unlocked)	47kΩ pullup load			0.5	V

AC ELECTRICAL CHARACTERISTICS

(MAX2370 EV kit, V_{CC} = +2.7V to +3.3V, $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = high, V_{GC} = 2.5V, R_{BIAS} = 10kΩ, 50Ω system, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = $\overline{CS}$ = 3.0V, f_{REF} = 19.2MHz, LO input power = -15dBm, f_{LO} = 575MHz, f_{RFOUT} = 455MHz, f_{IF} = 120MHz, registers set according to Table 1, input voltage at I and Q = 130mV_{RMS} differential, cascade specifications assume 400Ω IF filter with 5dB insertion loss, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
MODULATOR						
IF Frequency Range	Typically meets 30dB sideband suppression over this frequency range			95 to 195		MHz
I/Q Common-Mode Input Voltage	(Notes 2, 3)		1.35		V_{CC} - 1.25	V
I/Q Input Current	V_{CM} = 1.4V				6	µA
Gain-Control Range	V_{GC} = 0.5V to 2.5V	+25°C < T_A < +85°C	70	87		dB
		T_A = -40°C		85		
Gain Variation Over Temperature	Relative to +25°C, T_A = -40°C to +85°C			-2.4, +3.4		dB
Carrier Suppression	V_{GC} = 2.5V		30	40		dB
Sideband Suppression	V_{GC} = 2.5V		30	40		dB
IF Output Noise at Rx Band	V_{GC} set to give -12dBm IF output power, noise measured at 10MHz offset (Note 4)			-138	-135	dBm/Hz
IF Adjacent Channel Power Ratio IS-95 Reverse Modulation	V_{GC} set to give -12dBm IF output power, IFG[2:0] = 011	f_{OFFSET} = ±885kHz in 30kHz BW		-66		dBc
		f_{OFFSET} = ±1.125MHz in 30kHz BW		-69		
		f_{OFFSET} = ±1.98MHz in 30kHz BW		-84		
		f_{OFFSET} = ±4MHz in 30kHz BW		-89		
UPCONVERTER AND PREDRIVER						
RFOUT Frequency Range	See the *Typical Operating Characteristics* for typical gain vs. frequency			410 to 500		MHz
LO Frequency Range	Typically meets 30dB image suppression over this range			530 to 695		MHz
LO and RFPLL Input Power			-15	-7	0	dBm
Conversion Gain				23		dB
MPL Gain Change	MPL = 0, gain relative to MPL = 1			-3.4		dB
RF Gain-Control Range	V_{GC} = 0.5V to 2.5V	+25°C < T_A < +85°C	30	44		dB
		T_A = -40°C		46		
RF Image Suppression	At maximum output power			-20		dBc
Rx Band Noise Power	P_{RFOUT} = +8dBm, noise measured at +10MHz offset (Note 4)			-130	-128.5	dBm/Hz
CASCADED MODULATOR, UPCONVERTER, AND PREDRIVER						
RFOUT Output Power	Meets ACPR specifications (Note 4)		5.5	10		dBm
Adjacent Channel Power Ratio IS-95 Reverse Modulation (Note 4)	P_{OUT} = +8dBm, IFG[2:0] = 011	f_{OFFSET} = ±885kHz in 30kHz BW		-64	-57	dBc
		f_{OFFSET} = ±1.125MHz in 30kHz BW		-66	-61	
		f_{OFFSET} = ±1.98MHz in 30kHz BW		-82	-78	
		f_{OFFSET} = ±4MHz in 30kHz BW		-86	-78	
	P_{OUT} = +5.5dBm, IFG[2:0] = 011	f_{OFFSET} = ±885kHz in 30kHz BW		-64	-58	
		f_{OFFSET} = ±1.125MHz in 30kHz BW		-67	-62	
		f_{OFFSET} = ±1.98MHz in 30kHz BW		-81	-78	
		f_{OFFSET} = ±4MHz in 30kHz BW		-86	-85	

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2370 EV kit, V_{CC} = +2.7V to +3.3V, $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = high, V_{GC} = 2.5V, R_{BIAS} = 10kΩ, 50Ω system, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = $\overline{CS}$ = 3.0V, f_{REF} = 19.2MHz, LO input power = -15dBm, f_{LO} = 575MHz, f_{RFOUT} = 455MHz, f_{IF} = 120MHz, registers set according to Table 1, input voltage at I and Q = 130mV_{RMS} differential, cascade specifications assume 400Ω IF filter with 5dB insertion loss, T_A = +25°C, unless otherwise noted.) (Note 1)

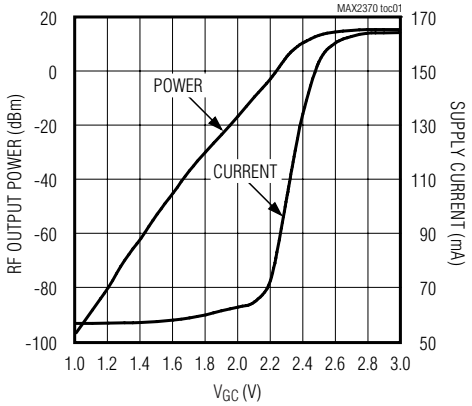
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Power Variation Over Temperature	Relative to +25°C, T_A = -40°C to +85°C		0, -2		dB
IF PLL					
Reference Frequency		5		30	MHz
Reference Frequency Signal Level		0.1		0.6	V_{P-P}
IF Main-Divide Ratio		256		16,383	
IF Reference-Divide Ratio		2		2047	
VCO Operating Range			190 to 390		MHz
Charge-Pump Source/Sink Current	ICP = 00	96	139	174	µA
	ICP = 01	135	192	240	
	ICP = 10	190	278	348	
	ICP = 11	267	390	488	
Turbolock Boost Current	ICP = 11, ICP_MAX = 1	533	774	968	µA
Charge-Pump Source/Sink Current Matching	All values of ICP, over compliance range			6	%
IF Charge-Pump Compliance		0.5		V_{CCIFCP} - 0.5V	V
RF PLL					
RF PLL Frequency Range	RF PLL operated at 2x LO frequency			1300	MHz
Reference Frequency		5		30	MHz
RF Main-Divide Ratio		4096		262,143	
RF Reference-Divide Ratio		2		8191	
Charge-Pump Source/Sink Current	RCP = 00	220	325	406	µA
	RCP = 01	441	650	813	
	RCP = 10	499	738	923	
	RCP = 11	717	1063	1329	
Turbolock Boost Current	(Note 5)	1152	1694	2118	µA
Charge-Pump Source/Sink Current Matching	All values of RCP, over compliance range			6	%
RF Charge-Pump Compliance		0.5		V_{CCRFCP} - 0.5V	V
Phase-Detector Noise Floor	RCP = 11, RCP_TURBO1 = RCP_TURBO2 = 0, 50kHz comparison frequency		-162		dBc/Hz

Note 1: Guaranteed by production test at T_A = +25°C to +85°C, design and characterization at T_A = -40°C.
Note 2: ACPR is met over the specified V_{CM} range.
Note 3: V_{CM} must be supplied by the I/Q baseband source with ±8µA current capability.
Note 4: Guaranteed by design and characterization to 6σ.
Note 5: When enabled with RCP_TURBO1 and RCP_TURBO2 (see Tables 3 and 4), the total charge-pump current is specified. For all values of RCP, the total turbolock current is 1.63 times the corresponding nonturbo current value.

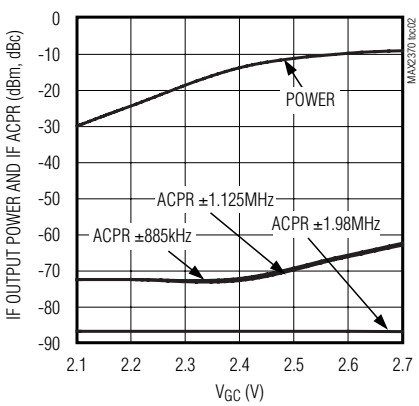
典型工作特性

(MAX2370 EV kit, $V_{CC\_}$ = $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = $\overline{CS}$ = 3.0V, f_{REF} = 19.2MHz, LO input power = -15dBm, f_{LO} = 575MHz, f_{RFOUT} = 455MHz, f_{IF} = 120MHz, R_{BIAS} = 10kΩ, V_{GC} = 2.5V, registers set according to Table 1, input voltage at I and Q = 130mV_{RMS} differential, T_A = +25°C, unless otherwise noted.)

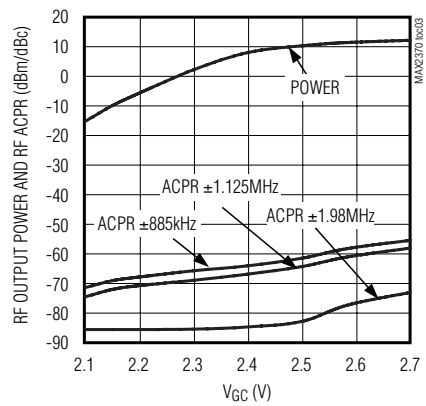
RF OUTPUT POWER AND SUPPLY CURRENT vs. GAIN-CONTROL VOLTAGE



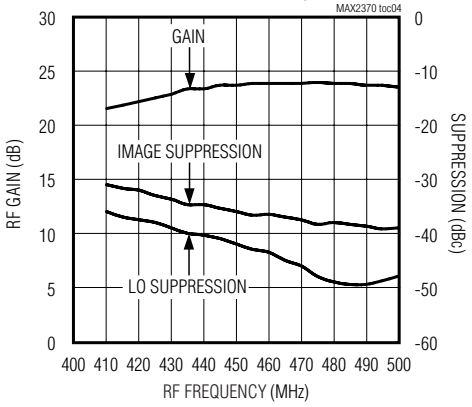
IF OUTPUT POWER AND IF ACPR vs. GAIN-CONTROL VOLTAGE



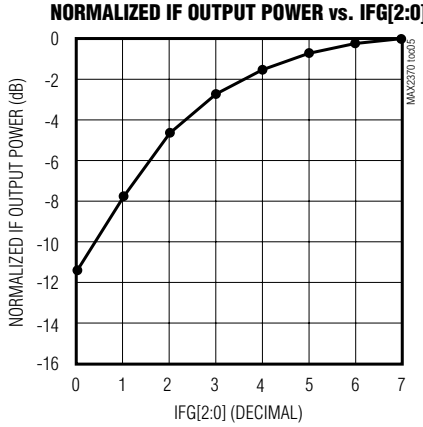
RF OUTPUT POWER AND RF ACPR vs. GAIN-CONTROL VOLTAGE



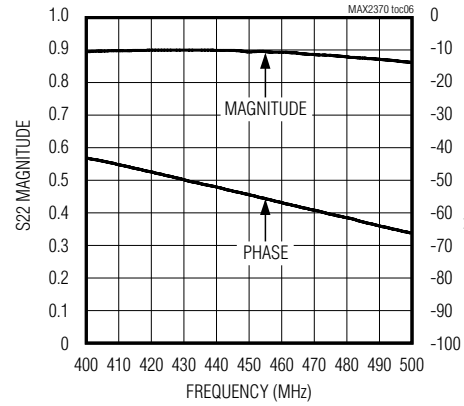
RF GAIN, IMAGE SUPPRESSION, AND LO SUPPRESSION vs. FREQUENCY



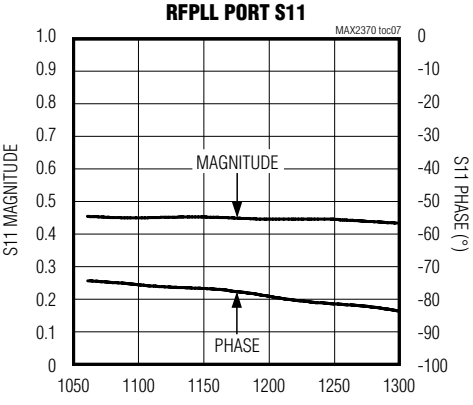
NORMALIZED IF OUTPUT POWER vs. IFG[2:0]



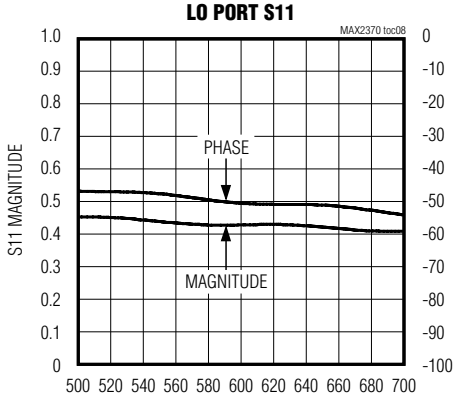
RFOUT PORT S22



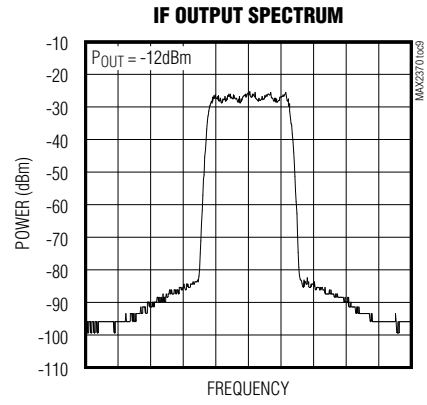
RFPLL PORT S11



LO PORT S11



IF OUTPUT SPECTRUM

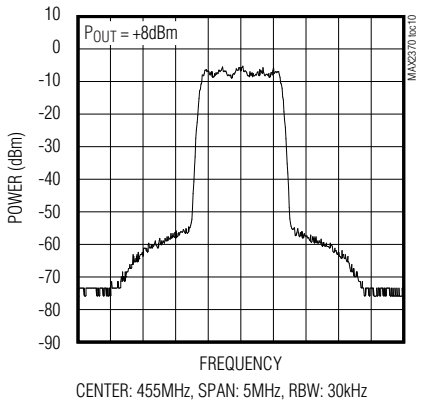


完备的450MHz正交发送器

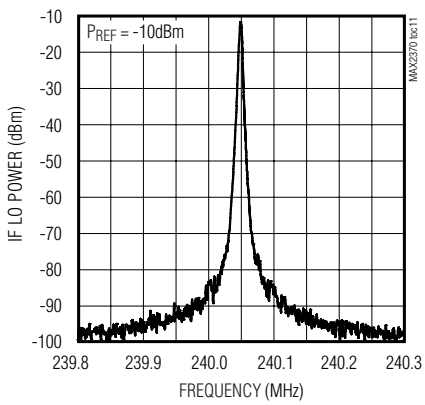
典型工作特性 (续)

(MAX2370 EV kit, $V_{CC\_}$ = $\overline{SHDN}$ = $\overline{IDLE}$ = $\overline{TXGATE}$ = $\overline{CS}$ = 3.0V, f_{REF} = 19.2MHz, LO input power = -15dBm, f_{LO} = 575MHz, f_{RFOUT} = 455MHz, f_{IF} = 120MHz, R_{BIAS} = 10kΩ, V_{GC} = 2.5V, registers set according to Table 1, input voltage at I and Q = 130mV_{RMS} differential, T_A = +25°C, unless otherwise noted.)

RF OUTPUT SPECTRUM



IF LOCAL OSCILLATOR SPECTRUM



引脚说明

引脚	名称	功能
1	RFOUT	RF输出，集电极开路输出，要求上拉一个电感至电源电压，此电感可作为匹配网络的一部分。
2, 10, 11, 16, 17, 32–35, 43, 47	N.C.	没有连接，该引脚开路，有些引脚在芯片内部已连接。
3	LOCK	IF和/或RF PLL状态指示，漏极开路输出。需要外加上拉电阻，通过配置寄存器的LD_MODE[1:0]位控制。
4	V_{CCDRV}	RF驱动级电源，用尽可能靠近引脚的电容旁路到地。旁路电容的接地过孔不能与其它接地支路共用。
5	$\overline{IDLE}$	数字输入，驱动到逻辑高电平时为正常工作状态；$\overline{IDLE}$为低电平时，除了RF PLL，其余电路处于关断状态。可以用一个很小的RC滤波器滤除数字信号噪声。
6	V_{CC}	上变频器电源输入，用尽可能靠近引脚的电容旁路到地。旁路电容的接地过孔不能与其它接地支路共用。
7	$\overline{TXGATE}$	数字输入，驱动到逻辑高电平时为正常工作状态；$\overline{TXGATE}$为低电平时，除了RF PLL、IF PLL、IF VCO外，其余电路处于关断状态。可以用一个很小的RC滤波器滤除数字信号噪声。
8, 9	IFIN+, IFIN-	差分IF输入至RF上变频器，IFIN+和IFIN-内部偏置在典型的V_{CC} - 1.5V。此端口输入阻抗为400Ω，差分IF滤波器输出交流耦合到该端口。须保持最短的差分传输线，尽可能降低寄生效应的影响。
12	RBIAS	偏置电阻连接，内部偏置在1.18V典型值。外部电阻必须连接在RBIAS与地之间，以合理设置上变频器和PA驱动级的偏置电流，标称电阻值为10kΩ，这个电阻值会影响驱动电路的线性特性。

引脚说明 (续)

引脚	名称	功能
13, 14, 15	CLK, DI, $\overline{CS}$	3线 (SPI/QSPI/MICROWIRE兼容) 串口CMOS输入，每个引脚可以用一个很小的RC滤波器滤除数字信号噪声。
18, 19	IFOUT-, IFOUT+	差分IF输出，IF_SEL为低电平时该端口有效，支持FM和CDMA模式。 IFOUT+和IFOUT-必须通过电感上拉到V_{CC}，典型差分负载为560Ω。此端口与IFIN+/-之间用400Ω差分IF带通滤波器连接，上拉电感为滤波器的一部分。此端口的差分输出阻抗通常为400Ω,包括560Ω的外部差分电阻。这些引脚之间要求用最短的传输线，以防止引入杂散信号和噪声。
20	GC	RF和IF增益控制模拟输入，输入电压范围从0.5V (最小增益) 到2.5V (最大增益)。没有驱动时，GC内部偏置在1.5V。该引脚需要一个RC低通滤波器，以消除DAC噪声和PDM时钟干扰。
21	V_{CC}	IF VGA电源输入，用尽可能靠近引脚的0.1µF电容旁路到地。旁路电容的接地过孔不能与其它接地支路共用。
22	V_{CC}	I/Q调制器电源输入，用尽可能靠近引脚的0.1µF电容旁路到地。旁路电容的接地过孔不能与其它接地支路共用。
23, 24	Q+, Q-	基带Q通道差分输入。Q+和Q-直接连到一对儿差分输入端，要求外部提供1.35V至 (V_{CC} - 1.5V) 的共模偏置电压。
25, 26	I+, I-	基带I通道差分输入。I+和I-直接连到一对儿差分输入端，要求外部提供1.35V至 (V_{CC} - 1.5V) 的共模偏置电压。
27	$\overline{SHDN}$	数字输入，驱动到低电平时关断IC；高电平时器件正常工作。可以用一个很小的RC低通滤波器消除数字噪声。
28	V_{CC}	VCO电源输入，用尽可能靠近引脚的0.1µF电容旁路到地。旁路电容的接地过孔不能与其它接地支路共用。
29	IFLO	IF LO输出，提供IF VCO输出连接，用于驱动外部锁相环。将BUF_EN控制位置低可禁止其工作。IFLO内部偏置在1.5V。
30, 31	TANK-, TANK+	IF VCO的差分谐振槽路连接。TANK+和TANK-内部偏置在1.6V，必须交流耦合到外部谐振电路。
36	REF	参考频率输入，REF的内部偏置在大约1.0V，必须交流耦合至参考源。这是一个高阻端口，需要外部端接到所要求的匹配阻抗。
37	V_{CCIFCP}	IF电荷泵电源输入，这个电源可不同于系统V_{CC}，用尽可能靠近引脚的0.1µF电容旁路到地。旁路电容的接地过孔不能与其它接地支路共用。
38	IFCP	高阻抗IF电荷泵输出，通过IF PLL环路滤波器连接到IF VCO的调谐输入端。从IFCP到调谐输入用尽可能短的连线，以减少杂散信号的引入。
39	V_{CC}	数字电路电源输入，用尽可能靠近引脚的0.1µF电容旁路到地。旁路电容的接地过孔不能与其它接地支路共用。

引脚说明 (续)

引脚	名称	功能
40	RFCP	高阻RF电荷泵输出。通过RF PLL环路滤波器连接到RF VCO的调谐输入。从RFCP到调谐输入需要采用尽可能短的连线，以减少杂散信号的引入。
41	V_{CCRFCP}	RF电荷泵电源输入，这个电源可不同于系统V_{CC}，用尽可能靠近引脚的0.1µF电容旁路到地。旁路电容的接地过孔不能与其它接地支路共用。
42	RFPLL	RF PLL输入，此端口驱动RF PLL。RFPLL内部偏置在V_{CC} - 0.8V。
44	LO	RF LO 输入，LO内部偏置在V_{CC} - 0.8V。
45, 46, 48, EP	GND	地。为保证正常的工作和散热，裸露焊盘要均匀地焊接到电路板的地平面。

详细说明

MAX2370正交发送器通过外部的共模偏置能够接受差分基带I/Q输入，上变频器把基带信号变为95MHz至195MHz的中频信号。由增益控制引脚 (GC) 的电压同时控制IF和RF VGA，具有很好的线性指标和低功耗特性。IF信号通过外部滤波器后经过上变频，进入VGA，然后送入PA驱动器，到达输出端。RF上变频需要外部VCO。IF PLL、RF PLL和工作模式由软件通过SPI/QSPI/MICROWIRE 3线接口编程控制。

以下对*功能框图*中的每部分电路进行说明。

I/Q调制器

差分同相 (I) 和正交 (Q) 信号采用直流耦合，并由基带DAC输出偏置。I、Q输入需要V_{CC} / 2直流偏置电压和8µA的驱动电流。但是，1.35V至V_{CC} - 1.25V 的共模电压都能满足要求。I/Q每个输入引脚对地容性负载为0.6pF。输出IF VCO送入2分频正交器后获得正交LO分量，驱动I/Q调制器。调制器输出被送入IF VGA。

IF VCO

IF VCO振荡频率为IF频率的2倍。振荡频率取决于外部谐振槽路（*参考IF谐振槽路设计*部分），IF VCO的典型杂散特性请*参考典型工作特性*。

IFLO输出缓冲器

IFLO提供了一个LO缓冲器，当BUF_EN为1时，IFLO输出频率与IF VCO的频率相同，典型输出功率为-12dBm。该输出适用于接收频率与发射IF频率相同的场合。

IF/RF PLL

IF/RF PLL用一个电荷泵输出驱动外部环路滤波器。该环路滤波器通常是一个二阶、无源、相位超前-置后补偿网络。滤波器的带宽、相位噪声取决于调谐器件。对相位噪声影响最大的是电感和变容二极管，使用高Q值电感和变容二极管可以获得最大的等效并联阻抗。IF_TURBO_CHARGE、RCP_TURBO1和RCP_TURBO2可以置位，使能增强模式，频率采集时增强模式能提供更大的电荷泵电流；频率采集完成后，增强模式将被禁止，此时，电荷泵电流返回到配置寄存器 ICP和RCP位所设置的数值 (表3)。

IF VGA

IF VGA通过改变GC引脚的电压控制IF输出电平，0.5V到2.5V的电压可实现大于70dB的增益控制范围，2.5V电压对应于最大增益。差分IF输出端口优化在95MHz到195MHz频率范围。为防止低温振荡，V_{GC}电压不能超过V_{CC} - 0.2V。

单边带混频器和RF VGA

RF发送混频器采用单边带技术，可省去外部RF滤波器。RF VGA使用与IF VGA相同的GC电压控制单边带混频器，能够达到最佳的电流损耗和线性指标。RF VGA可提供44dB的功率控制范围。

PA驱动器

MAX2370集成了一个能工作在410MHz到500MHz频率范围的功率放大器驱动电路。PA驱动器为集电极开路输出，需要上拉一个电感到V_{CC}。采用并-串匹配网络时，此电感可作为并联元件。

可编程寄存器

MAX2370集成了八个可编程寄存器，其中包括四个分频寄存器、一个配置寄存器、一个控制寄存器、一个电流控制寄存器和一个测试寄存器。每个寄存器有24位。每个寄存器的低4位有效位 (LSB) 是寄存器地址，20位高有效位 (MSB) 用于放置寄存器数据。大多数寄存器包含“无关”位，这些位可以是1或0，不会影响操作 (图1)。数据以MSB在前格式移入，然后是4位地址。$\overline{CS}$为低电平时，如果时钟有效，数据在时钟的上升沿串行移入器件。当$\overline{CS}$为高电平时，移位寄存器的数值锁存到由地址位选择的寄存器中。八个寄存器的典型设置见表1。分频和控制寄存器可通过SPI/QSPI/MICROWIRE串口编程。

RFM 寄存器设置RF PLL的主分频比，RFR寄存器设置参考频率的分频比，RF VCO频率由下式决定：

$$\text{RF VCO频率} = f_{REF} \times (RFM / RFR)$$

IFM和IFR寄存器相同：

$$\text{IF VCO频率} = f_{REF} \times (IFM / IFR)$$

f_{REF}是外部参考频率。

控制寄存器 (OPCTRL) 控制MAX2370的状态，表2说明了每一位的功能。

配置寄存器 (CONFIG) 对RF、IF PLL和基带I/Q的输入电平进行配置，表3给出了每位的功能。

电流控制寄存器 (I_{CC}CTRL) 修正偏置电流，以满足不同的工作模式。在大功率模式下，MPL = 1设置偏置电流和转换增益，使PA驱动器提供至少+5.5dBm的输出功率。低噪声模式下，MPL = 0 可以在任何给定输出功率下使输出噪声减小2.5dB，代价是输出功率比能够获得的最大功率减小3.4dB。

电源管理

偏置电压控制分布在不同的功能电路，可以实现不同的电源关断模式，如表 8所示。

关断期间，串口保持有效。设置控制位 SHDN_BIT = 0 或控制引脚$\overline{SHDN}$ = GND，器件关断。任何情况下都会保留PLL设置和寄存器信息。

应用信息

3线串口

图3所示为3线串口时序图，3线总线兼容于SPI/QSPI/MICROWIRE。

电磁兼容性考虑

为了获得一个低杂散，符合EMC标准的发送器，减小电流回路的面积可降低H场辐射。为减小电流回路面积，所有V_{CC}对地的旁路电容要尽可能靠近引脚安装。为减小电压波动，V_{CC}引线要短而粗。

只对寄存器必须设置的控制位进行编程设置，尽可能减少串口时钟。3线接口的RC滤波器有助于平滑时钟的边缘，降低高频频谱成份。RC滤波器还通过旁路高频信号提供瞬态保护。同样，逻辑输入 ($\overline{SHDN}$、$\overline{TXGATE}$、$\overline{IDLE}$) 等引脚也需RC滤波器。

靠近引脚安装高频旁路电容，每个电容要有专门的接地过孔。48引脚、薄型QFN-EP封装利用器件下方的裸露焊盘提供最小接地电感。至少采用5个低电感过孔将裸露焊盘接地。尽可能使用大面积接地，截断地平面会影响散热和屏蔽效果。

RF LO引线要尽可能短，以降低LO辐射和电磁干扰。

IF谐振槽路设计

IF谐振槽路为全差分结构。设计120MHz中频谐振器时，外部调谐器件的*典型应用电路*见应用笔记 *MAX2360中频槽路设计*。在 www.maxim-ic.com.cn网站可以获得更多的中频谐振槽路设计信息。

完备的450MHz正交发送器

IC内部，电荷泵漏电流小于10nA，相当于一个300MΩ的泄漏电阻。电荷泵输出具有很高的、超过300MΩ的直流电阻，这有助于减少相关频率上电荷泵的杂散效应。要保证变容二极管和环路滤波器的下面没有焊锡，并且使用低泄露电容。

PCB布局的考虑

MAX2370评估板为PCB布局提供了一个参考方案，为达到良好性能，要特别注意电源、RF、LO和IF的PCB设计。

电源设计

为减小IC不同部分的耦合，理想的电源布局为星型连接，在中心V_{CC}节点处放置大的去耦电容。V_{CC}引线从该节点引出，连接到MAX2370的各个V_{CC}引脚。每条电源线的末端采用旁路电容，并保证在敏感的频点与地之间的阻抗低于1Ω。这种布局需要在每个V_{CC}引脚提供一个去耦电容，为减小接地感抗，每个旁路电容至少有一个接地过孔。同样，连接裸露焊盘到PCB地，尽可能用多个接地过孔来减小感抗。

匹配网络布局

匹配网络布局对电路中的寄生成份非常敏感。为减少寄生电感，应保证所有连线尽可能短，元件尽可能靠近芯片。为减小寄生电容，可将匹配网络元件下面的地平面挖空。

高阻抗端口 (例如IF输入和输出) 要用最短的连接线，以减小寄生电容。

谐振槽路布局

须保持最短的谐振槽路引线，以减小串联电感效应和旁路电容，电感和耦合电容的焊盘要尽可能小，以减小寄生电容。

芯片信息

PROCESS: BiCMOS

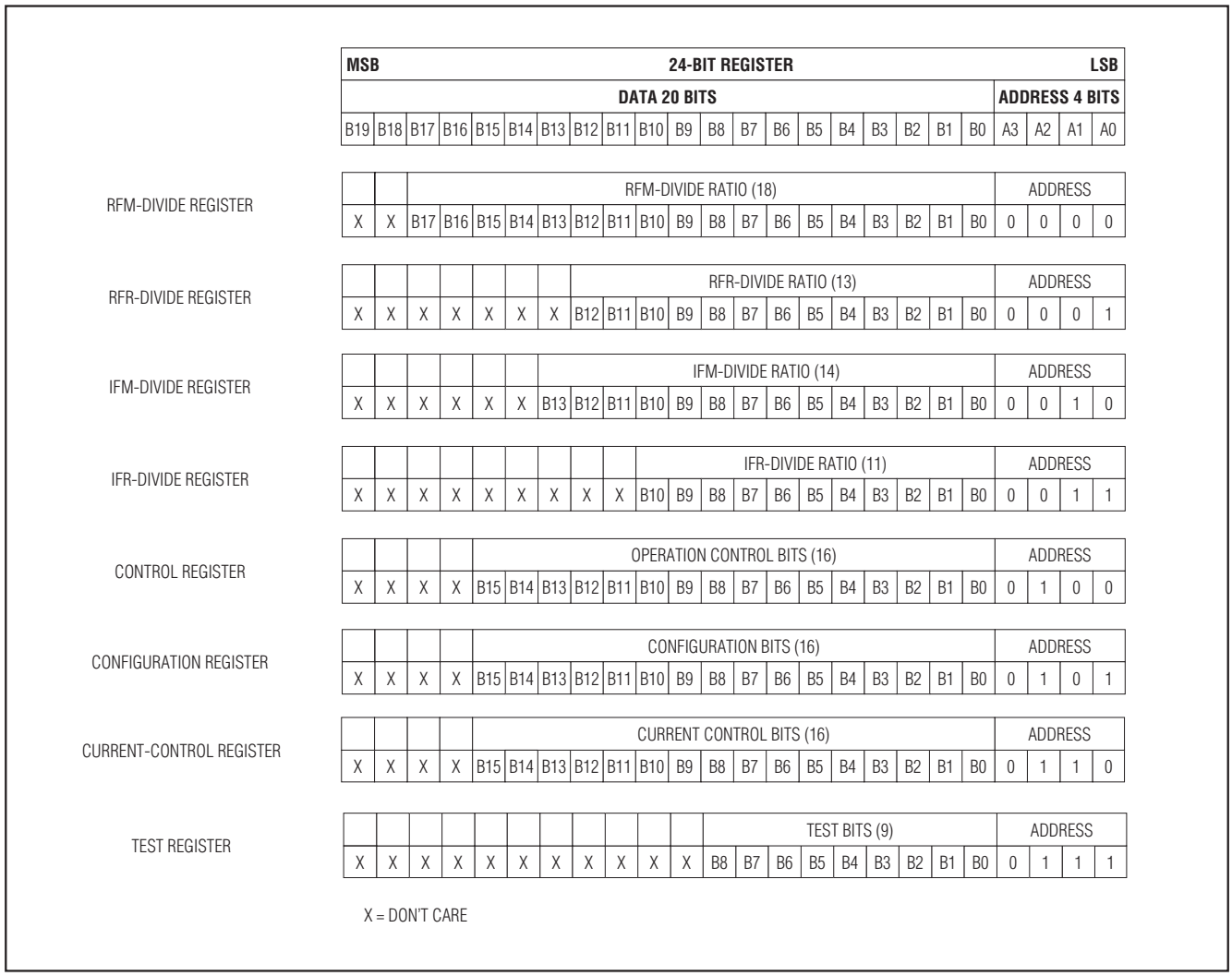

MSB
24-BIT REGISTER
LSB
DATA 20 BITS
ADDRESS 4 BITS
B19 B18 B17 B16 B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 A3 A2 A1 A0
RFM-DIVIDE REGISTER
RFM-DIVIDE RATIO (18)
ADDRESS
X X B17 B16 B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 0 0 0 0
RFR-DIVIDE REGISTER
RFR-DIVIDE RATIO (13)
ADDRESS
X X X X X X X B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 0 0 0 1
IFM-DIVIDE REGISTER
IFM-DIVIDE RATIO (14)
ADDRESS
X X X X X X B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 0 0 1 0
IFR-DIVIDE REGISTER
IFR-DIVIDE RATIO (11)
ADDRESS
X X X X X X X X X B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 0 0 1 1
CONTROL REGISTER
OPERATION CONTROL BITS (16)
ADDRESS
X X X X B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 0 1 0 0
CONFIGURATION REGISTER
CONFIGURATION BITS (16)
ADDRESS
X X X X B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 0 1 0 1
CURRENT-CONTROL REGISTER
CURRENT CONTROL BITS (16)
ADDRESS
X X X X B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 0 1 1 0
TEST REGISTER
TEST BITS (9)
ADDRESS
X X X X X X X X X X X B8 B7 B6 B5 B4 B3 B2 B1 B0 0 1 1 1
X = DON'T CARE

图1. 寄存器配置

表1. 典型工作模式下的寄存器设置

REGISTER NAME	TYPICAL SETTINGS	REGISTER ADDRESS	FUNCTION
RFM[17:0]	23000_{DEC}	0000_b	RF M-Divider Count
RFR[12:0]	384_{DEC}	0001_b	RF R-Divider Count
IFM[13:0]	4800_{DEC}	0010_b	IF M-Divider Count
IFR[10:0]	384_{DEC}	0011_b	IF R-Divider Count
OPCTRL[15:0]	$090F_{hex}$	0100_b	Operational Control Settings
CONFIG[15:0]	$D03F_{hex}$	0101_b	Configuration and Setup Control
I_{CC}CTRL[15:0]	$0C38_{hex}$	0110_b	Current Multiplication Factor, Throttle-Back Control, Modulator Bypass, Compensation for Gain Variation Over Temperature, Maximum Power-Level Setting
TEST[8:0]	100_{hex}	0111_b	Test Mode Control

表2. 控制寄存器 (OPCTRL，地址: 0100_b)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTINGS	FUNCTION
RESERVED	15	0	Reserved. Set to 0 for normal operation.
RCP_TURBO1	14	0	Works with RCP_TURBO2 (in the configuration register) to set the turbo charge-pump mode (see Table 7).
ICP_MAX	13	0	0 = Normal operation. 1 = Sets IF charge-pump current to turbo level and keeps it there even after lock is established. This mode provides the highest charge-pump current, but effectively no turbo mode since current is already at maximum.
RESERVED	12, 11	01	Reserved. Set to 01 for normal operation.
RESERVED	10, 9	00	Reserved. Set to 00 for normal operation.
IFG	8, 7, 6	100	3-bit gain balancing control. Increases IF gain by approximately 2dB per LSB. Provides a means for adjusting balance between RF and IF gain for optimized linearity.
RESERVED	5	0	Reserved. Set to 0 for normal operation.
BUF_EN	4	0	LO buffer enable. 0 = LO buffer off. 1 = LO buffer on.
MOD_TYPE	3	1	Selects type of modulation. 0 = Selects direct VCO modulation (IF VCO is directly modulated and the I/Q modulator is bypassed). 1 = Selects quadrature modulation.
$\overline{\text{STBY}}$	2	1	Standby control. 0 = Shuts down everything except the registers and serial interface. 1 = Normal operation.
$\overline{\text{TXSTBY}}$	1	1	Transmitter standby control. 0 = Shuts down the modulator and upconverter leaving PLLs locked and registers active. This bit's functionality is equivalent to that of the $\overline{\text{TX\_GATE}}$ pin. 1 = Normal operation.
SHDN_BIT	0	1	Shutdown control. 0 = Shuts down everything except the serial interface. 1 = Normal operation.

表3. 配置寄存器 (CONFIG, 地址: 0101_b)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTINGS	FUNCTION
IF_PLL_SHDN	15	1	IF PLL shutdown control. 0 = Shuts down IF PLL. This mode is used with an external IF PLL. 1 = Normal operation.
RF_PLL_SHDN	14	1	RF PLL shutdown control. 0 = Shuts down RF PLL. This mode is used with an external RF PLL. 1 = Normal operation.
RESERVED	13	0	Reserved. Set to 0 for normal operation.
IQ_LEVEL	12	1	Selects the nominal I/Q input levels. 0 = Selects 300mV$_{P-P}$ input mode. 1 = Selects 600mV$_{P-P}$ input mode.
RESERVED	11, 10	00	Reserved. Set to 00 for normal operation.
ICP	9, 8	00	Sets the IF charge-pump current. 00 = 139µA. 01 = 192µA. 10 = 278µA. 11 = 390µA.
RCP	7, 6	00	Sets the RF charge-pump current. 00 = 325µA. 01 = 650µA. 10 = 738µA. 11 = 1063µA.
RESERVED	5, 4	11	Reserved. Set to 11 for normal operation.
IF_TURBO_CHARGE	3	1	IF turbo-charge control. 0 = Disables extra charge-pump current during acquisition. 1 = Activates turbo-charge feature providing extra current during acquisition.
RCP_TURBO2	2	1	Works with RCP_TURBO1 (in the operation control register) to set the turbo charge-pump mode (see Table 7).
LD_MODE	1, 0	11	Determines output mode for LOCK pin as defined below: 00 = Test mode. 01 = IF PLL lock detector. 10 = RF PLL lock detector. 11 = Logical AND of IF PLL and RF PLL lock detectors.

表4. 电流控制寄存器 (I_{CC}CTRL, 地址: 0110_b)

BIT NAME	BIT LOCATION (0 = LSB)	TYPICAL SETTINGS	FUNCTION
RESERVED	15, 14, 13, 12	0000	Reserved. Set to 0000 for normal operation.
MPL	11	1	Sets the maximum RF output power level. 0 = Sets to low-noise mode. 1 = Sets to normal power mode.
RESERVED	10, 9, 8, 7	1000	Reserved. Set to 1000 for normal operation.
THROTTLE_BACK	6, 5, 4	011	Controls the throttleback rate (see Table 6).
I_MULT	3, 2, 1, 0	1000	Sets the current scale factor for the PA driver (see Table 5).

表5. 利用I_MULT位设置典型电流比例因数

BIT NAME	BITS	NOMINAL CURRENT SCALE FACTOR
I_MULT	0011	0.69
	0100	0.75
	0101	0.81
	0110	0.88
	0111	0.94
	1000 (default)	1.00
	1001	1.13
	1010	1.25
	1011	1.38
	1100	1.50

表6. 利用THROTTLE_BACK位设置降率

BIT NAME	BITS	NOMINAL RATE (dBmA/dB)
THROTTLE_BACK	000	1.3
	001	1.2
	010	1.1
	011	1.0
	100	0.9
	101	0.8
	110	0.7
	111	0.6

表7. RF增强电荷泵模式电流设置

RCP_TURBO1	RCP_TURBO2	FUNCTION
0	0	No turbo current. Charge-pump current is set by RCP bits.
0	1	Turbo current turns on every time RF PLL is reprogrammed. Turbo current is automatically turned off after RF PLL is locked.
1	0	Turbo current is always on.
1	1	Turbo current is turned on every time RF PLL is out of lock.

表8. 关断模式

POWER-DOWN MODE	COMMENTS	UPCONVERTER	MODULATOR	RF PLL	IF VCO	IF PLL
$\overline{\text{SHDN}}$ Pin	Ultra-low shutdown current	OFF	OFF	OFF	OFF	OFF
$\overline{\text{IDLE}}$ Pin	Rx only mode	OFF	OFF	—	OFF	OFF
$\overline{\text{TXGATE}}$ Pin	For punctured Tx mode	OFF	OFF	—	—	—
RF_PLL_SHDN Bit	For external RF PLL use	—	—	OFF	—	—
IF_PLL_SHDN Bit	For external IF PLL use	—	—	—	—	OFF
$\overline{\text{TXSTBY}}$ Bit	Tx is OFF, but IF and RF LOs stay locked	OFF	OFF	—	—	—

完备的450MHz正交发送器

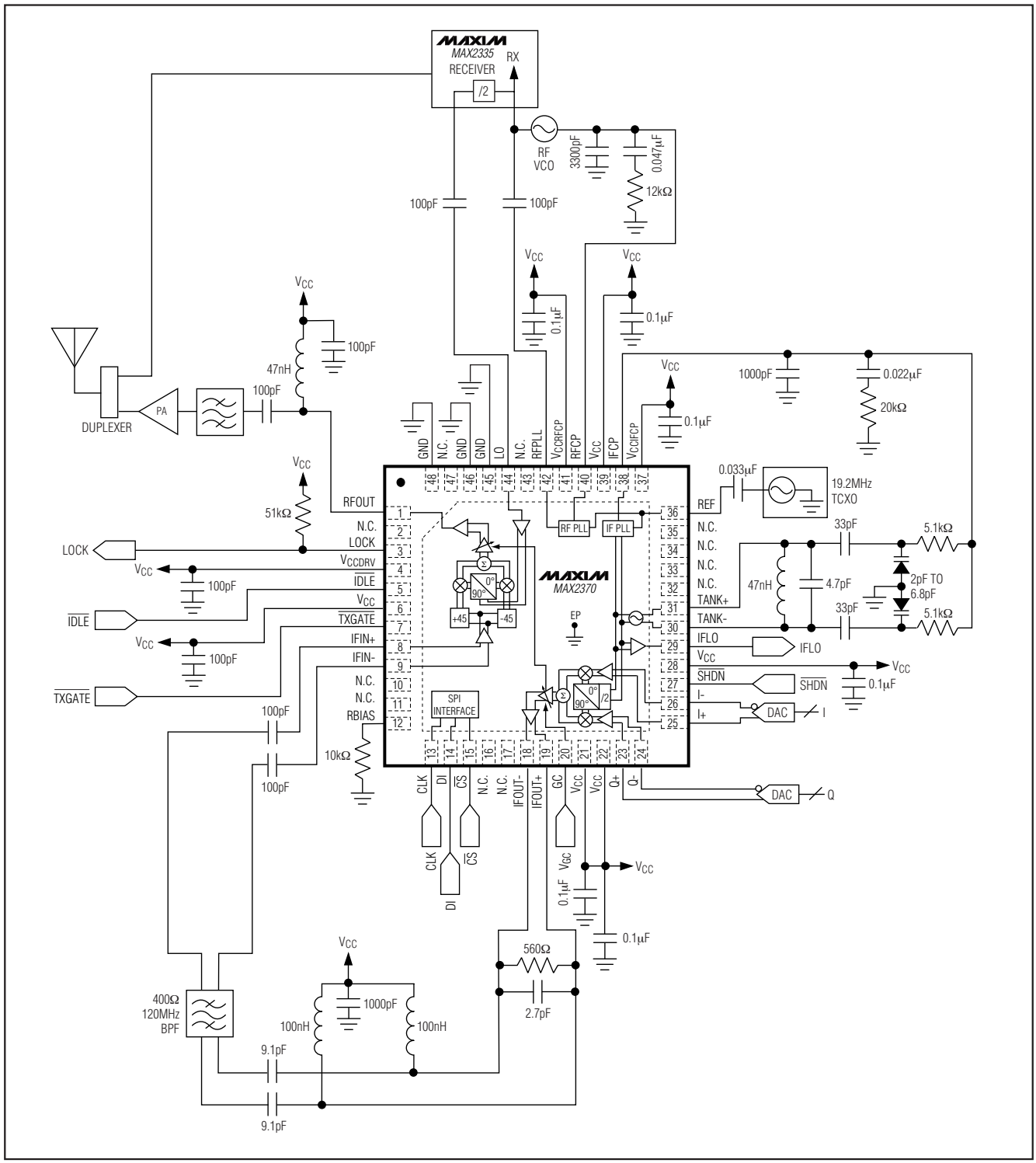


图2. MAX2370典型应用电路

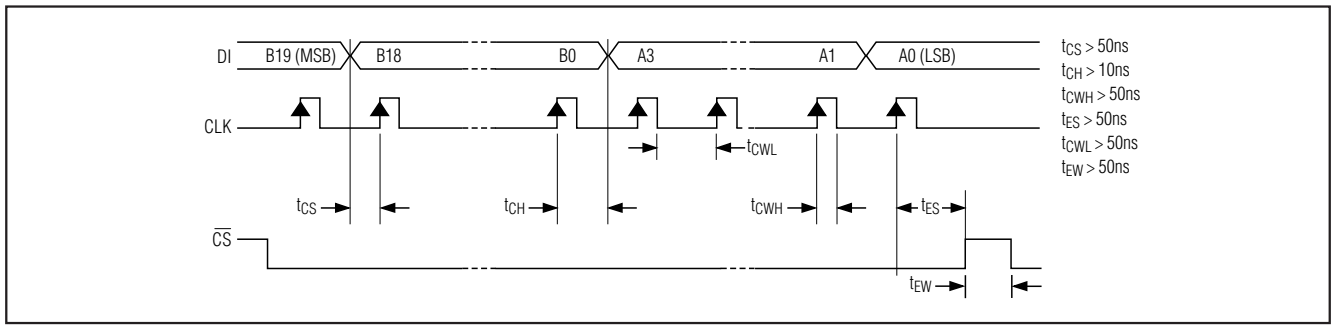

DI
B19 (MSB)
B18
B0
A3
A1
A0 (LSB)
CLK
$\overline{CS}$
t_{CS}
t_{CH}
t_{CWL}
t_{CWH}
t_{ES}
t_{EW}
t_{CS} > 50ns
t_{CH} > 10ns
t_{CWH} > 50ns
t_{ES} > 50ns
t_{CWL} > 50ns
t_{EW} > 50ns

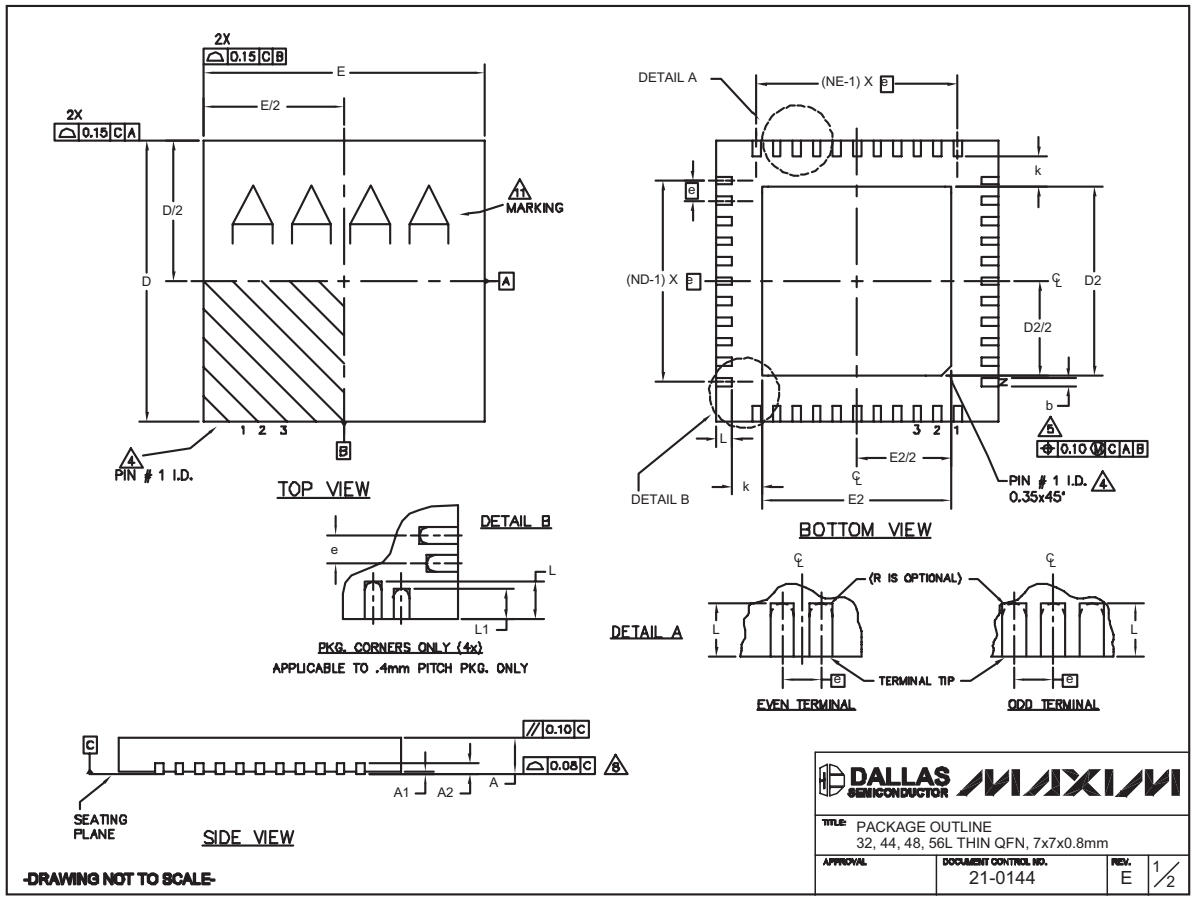
图3. 3线接口时序图

完备的450MHz正交发送器

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 www.maxim-ic.com.cn/packages。)

32, 44, 48L QFN.EPS



封装信息（续）

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 www.maxim-ic.com.cn/packages。)

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.40	0.50	0.60
L1	–	–	–	–	–	–	–	–	–	–	–	–	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C	DOWN BONDS ALLOWED
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–	YES
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–	NO
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1	YES
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–	NO
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T4877-4	–	5.45	5.60	5.63	5.45	5.60	5.63	–	YES
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–	NO
T4877-6	–	5.45	5.60	5.63	5.45	5.60	5.63	–	NO
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–	YES
T5677-1	–	5.20	5.30	5.40	5.20	5.30	5.40	–	YES

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-1/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
32, 44, 48, 56L THIN QFN, 7x7x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	E	2/2

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