19-6381; Rev 0; 6/12
备有评估板

MAX19794

10MHz至500MHz、双通道、模拟电压可变增益衰减器，内置10位、SPI控制DAC

概述

MAX19794为双路、通用的模拟电压可变增益衰减器(VVA)，设计工作在10MHz至500MHz频率范围的50Ω系统。器件包括一个拥有专利的控制电路，提供22.4dB衰减范围(每路衰减器)，典型线性控制斜率为8dB/V。

两路衰减器共用一路模拟控制信号，可以级联产生44.7dB的总衰减范围，获得16dB/V (5V工作)的典型线性控制斜率。

MAX19794单芯片方案采用了Maxim专有的SiGe BiCMOS工艺。器件采用+5V或+3.3V单电源供电，提供紧凑的36引脚、TQFN封装(6mm x 6mm x 0.8mm)，带有裸焊盘。在-40°C至+100°C扩展级温度范围内确保电气规格。

应用

宽带应用系统：无线基础架构中的数字及扩频通信系统

WCDMA/LTE、TD-SCDMA/TD-LTE、WiMAX®、cdma2000®、GSM/EDGE和MMDS基站

VSAT/卫星调制解调器

军用系统

微波点对点系统

增益调节

温补电路

自动电平控制(ALC)

发射器增益控制

接收器增益控制

通用测试设备

优势与特性

- 宽带覆盖
  - ✧ 整个衰减范围内保持IIP3大于+34.4dBm
- 高线性度
  - ✧ 整个衰减范围内保持IIP3大于+34.4dBm
  - ✧ +21.8dBm输入P1dB
- 单一芯片集成两路模拟衰减器
- 两种便利的控制选择
  - ✧ 单路模拟电压控制
  - ✧ 通过SPI控制的片上10位DAC
- 步增/步降脉冲控制输入
- 灵活的衰减控制范围
  - ✧ 22.4dB (每路衰减器)
  - ✧ 44.7dB (两路衰减器级联)
- 线性模拟控制响应(dB/V)简化自动电平控制和增益调整算法
- 在较宽的频率范围和衰减设置下保持优异的衰减平坦度
- 集成比较器(用于对衰减器控制电压进行逐次逼近测量)
- 源电流低至13mA
- 采用+5V或3.3V单电源供电
- 与MAX19791、MAX19792和MAX19793引脚相似
- 无铅封装

WiMAX是WiMAX Forum.注册的认证和服务商标。
cdma2000是Telecommunications Industry Association.的注册商标。

定购信息在数据资料的最后给出。

相关型号以及配合该器件使用的推荐产品，请参见：china.maximintegrated.com/MAX19794.related。

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +5.5V
REF_IN ..... -0.3V to Minimum (V_{CC} + 0.3V, 3.6V)
REF_SEL, DAC_LOGIC, MODE, DWN, UP,
DIN, CLK, $\overline{CS}$ ..... -0.3V to Minimum (V_{CC} + 0.3V, 3.6V)
COMP_OUT, DOUT ..... -0.3V to +3.6V
IN_A, OUT_A, IN_B, OUT_B ..... -0.3V to V_{CC} + 0.3V
CTRL (except for test mode) ..... -0.3V to V_{CC} + 0.3V
Maximum CTRL Pin Load Current
(CTRL configured as an output) 0.3mA
RF Input Power at IN_A, IN_B, OUT_A, OUT_B ..... +20dBm
Continuous Power Dissipation (Note 1) 2.8W
Operating Case Temperature Range (Note 2) ... -40°C to +100°C
Maximum Junction Temperature ..... 150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Application Information* section for details. The junction temperature must not exceed +150°C.

Note 2: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) (Notes 3, 4) ..... +36°C/W

Junction-to-Case Thermal Resistance (θ_{JC}) (Notes 1, 4) ..... +10°C/W

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **china.maximintegrated.com/thermal-tutorial**.

3.3V DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.15V to 3.45V, V_{CTRL} = 1V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, no RF signals applied, all input and output ports terminated with 50Ω through DC blocks, T_C = -40°C to +100°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.15	3.3	3.45	V
Supply Current	I_{CC}			9.5	14	mA
Control Voltage Range	V_{CTRL}		1.0		2.5	V
CTRL Input Resistance	R_{CTRL}			1.0		MΩ
Input CurrentLogic-High	I_{IH}		-1.0		+1.0	µA
Input Current Logic-Low	I_{IL}		-1.0		+1.0	µA
REF_IN Voltage				1.4		V
REF_IN Input Resistance				1.0		MΩ
DAC Number of Bits		Monotonic			10	bits
Input Voltage Logic-High	V_{IH}		2.0			V
Input Voltage Logic-Low	V_{IL}				0.8	V
COMP_OUT Logic-High		RDBK_EN (D9, REG3) = Logic 1, R_{LOAD} = 47kΩ		3.3		V
COMP_OUT Logic-Low		RDBK_EN (D9, REG3) = Logic 1, R_{LOAD} = 47kΩ		0		V

5V DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, no RF signals applied, all input and output ports terminated with 50Ω through DC blocks, T_C = -40°C to +100°C, unless otherwise noted. Typical values are at V_{CC} = 5.0V, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, T_C = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.0	5.25	V
Supply Current	I_{CC}			13	18.6	mA
Control Voltage Range	V_{CTRL}		1.0		4.0	V
CTRL Input Resistance	R_{CTRL}			124		kΩ
Input Current Logic-High	I_{IH}		-1.0		+1.0	µA
Input Current Logic-Low	I_{IL}		-1.0		+1.0	µA
REF_IN Voltage Range				1.4		V
REF_IN Input Resistance				1.0		MΩ
DAC Number of Bits		Monotonic		10		Bits
Input Voltage Logic-High	V_{IH}		2.0			V
Input Voltage Logic-Low	V_{IL}				0.8	V
COMP_OUT Logic-High		RDBK_EN (D9, REG3) = Logic 1, R_{LOAD} = 47kΩ		3.3		V
COMP_OUT Logic-Low		RDBK_EN (D9, REG3) = Logic 1, R_{LOAD} = 47kΩ		0		V

Recommended AC Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Note 6)	10		500	MHz
RF Port Input Power	P_{RF}	Continuous operation			15	dBm

3.3V AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, one attenuator, V_{CC} = 3.15V to 3.45V, RF ports are driven from 50Ω sources and loaded into 50Ω, input P_{RF} = 0dBm, f_{RF} = 10MHz to 500MHz, V_{CTRL} = 1V to 2.5V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, T_C = -40°C to +100°C. Typical values are for T_C = +25°C, V_{CC} = 3.3V, input P_{RF} =0dBm, f_{RF} = 55MHz, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, unless otherwise noted.) (Notes 5, 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss	IL	One attenuator		1.5		dB
		Two attenuators, f_{RF} = 55MHz, V_{CTRL} = 1.0V		3.0	5.0	
Loss Variation Over Temperature		T_C = -40°C to +100°C		0.28		dB
Input P1dB	IP1dB			16.4		dBm
Minimum Input Second-Order Intercept Point Over Full Attenuation Range (Note 8)	IIP2	One attenuator f_{RF1} +f_{RF2} term, f_{RF1} - f_{RF2} = 1MHz V_{CTRL} = 1.0V to 2.5V P_{RF} = 0dBm/tone applied to attenuator input		44.9		dBm
		Two attenuators f_{RF1} + f_{RF2} term, f_{RF1} - f_{RF2} = 1MHz V_{CTRL} = 1.0V to 2.0V P_{RF} = 0dBm/tone applied to attenuator input		42.7		
Minimum Input Third-Order Intercept Point Over Full Attenuation Range (Note 8)	IIP3	One attenuator V_{CTRL} =1.0V to 2.5V f_{RF1} - f_{RF2} = 1MHz P_{RF} = 0dBm/tone applied to attenuator input		30.8		dBm
		Two attenuators V_{CTRL} =1.0V to 2.0V f_{RF1} - f_{RF2} = 1MHz P_{RF} = 0dBm/tone applied to attenuator input		29.9		
Second Harmonic				62		dBc
Third Harmonic				89.7		dBc
Attenuation Control Range		One attenuator, V_{CTRL} = 1.0V to 2.5V, f_{RF} = 55MHz		22.5		dB
		Two attenuators, V_{CTRL} = 1.0V to 2.5V, f_{RF} = 55MHz	38.5	45		dB
Average Attenuation-Control Slope		V_{CTRL} = 1.4V to 2.3V		22.5		dB/V
Maximum Attenuation-Control Slope		V_{CTRL} = 1.0V to 2.5V		40		dB/V
S21 Attenuation Deviation from a straight line		V_{CTRL} = 1.4V to 2.1V		±0.4		dB

5V AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, one attenuator, V_{CC} = 4.75V to 5.25V, RF ports are driven from 50Ω sources and loaded into 50Ω, input P_{RF} = 0dBm, f_{RF} = 10MHz to 500MHz, V_{CTRL} = 1V to 4V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, T_C = -40°C to +100°C. Typical values are for T_C = +25°C, V_{CC} = 5.0V, input P_{RF} = 0dBm, f_{RF} = 55MHz, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, unless otherwise noted.) (Notes 5, 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Insertion Loss	IL	One attenuator		1.5		dB
		Two attenuators		3.0	5.0	dB
Loss Variation Over Temperature		T_C = -40°C to +100°C		0.29		dB
Input P_{1dB}	IP_{1dB}			21.8		dBm
Minimum Input Second-Order Intercept Point Over Full Attenuation Range (Note 8)	IIP2	One attenuator f_{RF1} + f_{RF2} term, f_{RF1} - f_{RF2} = 1MHz V_{CTRL} = 1.0V to 4.0V P_{RF} = 0dBm/tone applied to attenuator input		48.1		dBm
		Two attenuators f_{RF1} +f_{RF2} term, f_{RF1} - f_{RF2} = 1MHz V_{CTRL} = 1.0V to 4.0V P_{RF} = 0dBm/tone applied to attenuator input		46.5		
Minimum Input Third-Order Intercept Point Over Full Attenuation Range (Note 8)	IIP3	One attenuator V_{CTRL} from 1.0V to 4.0V f_{RF1} - f_{RF2} = 1MHz P_{RF} = 0dBm/tone applied to attenuator input		34.4		dBm
		Two attenuators V_{CTRL} from 1.0V to 4.0V f_{RF1} - f_{RF2} = 1MHz P_{RF} = 0dBm/tone applied to attenuator input		32.3		
Second Harmonic				63		dBc
Third Harmonic				97		dBc
Attenuation Control Range		One attenuator, V_{CTRL} = 1.0V to 4.0V, f_{RF} = 55MHz		22.4		dB
		Two attenuators V_{CTRL} = 1.0V to 4.0V, f_{RF} = 55MHz	38.5	44.7		dB
Average Attenuation-Control Slope		V_{CTRL} = 1.5V to 3.1V		8.0		dB/V
		V_{CTRL} = 1.5V to 3.5V		9.4		
Maximum Attenuation-Control Slope		V_{CTRL} = 1.5V to 3.5V		30		dB/V
Attenuation Flatness over any 125MHz band		V_{CTRL} = 1.0V to 3.1V, f_{RF} = 10MHz to 250MHz		0.15		dB
		V_{CTRL} = 1.0V to 3.1V, f_{RF} = 250MHz to 500MHz		0.2		

5V AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, one attenuator, V_{CC} = 4.75V to 5.25V, RF ports are driven from 50Ω sources and loaded into 50Ω, input P_{RF} = 0dBm, f_{RF} = 10MHz to 500MHz, V_{CTRL} = 1V to 4V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, T_C = -40°C to +100°C. Typical values are for T_C = +25°C, V_{CC} = 5.0V, input P_{RF} = 0dBm, f_{RF} = 55MHz, V_{CTRL} = 1.0V, V_{DAC_LOGIC} = 0V, RDBK_EN (D9, REG3) = Logic 0, unless otherwise noted.) (Notes 5, 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
CTRL Switching Time (Note 9)		15dB to 0dB range		390		ns
		0dB to 15dB range		780		
$\overline{CS}$ Switching Time (Note 10)		15dB to 0dB range		700		ns
		0dB to 15dB range		2600		
MODE Switching Time (Note 11)		15dB to 0dB range (MODE 1 to 0)		700		ns
		0dB to 15dB range (MODE 0 to 1)		2600		
Input Return Loss				31		dB
Output Return Loss				28		dB
Group Delay				40		ps
Group Delay Flatness		f_{RF} = 30MHz to 88MHz		25		ps
Group Delay Change		V_{CTRL} = 1.0V to 4.0V		-400		ps
Insertion Phase Change vs. Attenuation Control		V_{CTRL} = 1.0V to 4.0V		5		deg
S21 Attenuation Deviation from a Straight Line		V_{CTRL} = 1.5V to 3.1V		±0.35		dB
SERIAL PERIPHERAL INTERFACE (SPI)						
Maximum Clock Speed				20		MHz
Data-to-Clock Setup Time	t_{CS}	(Note 12)		2		ns
Data-to-Clock Hold Time	t_{CH}	(Note 12)		2.5		ns
$\overline{CS}$ to CLK Setup Time	t_{EWS}	(Note 12)		3		ns
$\overline{CS}$ Positive Pulse Width	t_{EW}	(Note 12)		7		ns
Clock Pulse Width	t_{CW}	(Note 12)		5		ns

Note 5: Production tested at T_C = +100°C. All other temperatures are guaranteed by design and characterization.

Note 6: Recommended functional range. Not production tested. Operation outside this range is possible, but with degraded performance of some parameters.

Note 7: All limits include external component losses, connectors and PCB traces. Output measurements taken at the RF port of the Typical Application Circuit,.

Note 8: f_{RF1} = 56MHz, f_{RF2} = 55MHz, P_{RF} = 0dBm/tone applied to attenuator input.

Note 9: Switching time is measured from 50% of the CTRL signal to when the RF output settles to ±1dB. R3 = 0Ω

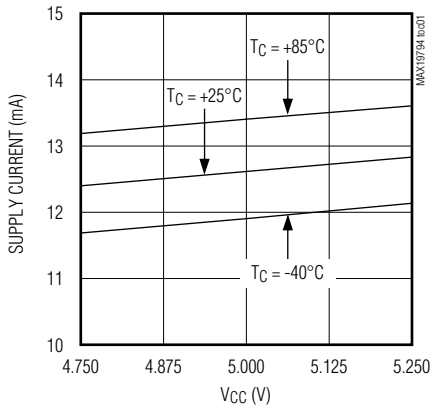
Note 10: Switching time is measured from when $\overline{CS}$ is asserted to when the RF output settles to ±1dB.

Note 11: Switching time is measured from when MODE is asserted to when the RF output settles to ±1dB.

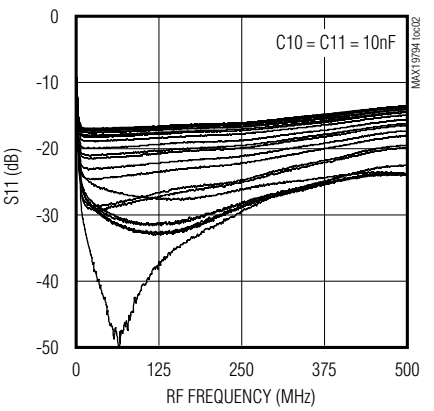
Note 12: Typical minimum time for proper SPI operation.

(*Typical Application Circuit*, **V_{CC} = 5.0V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

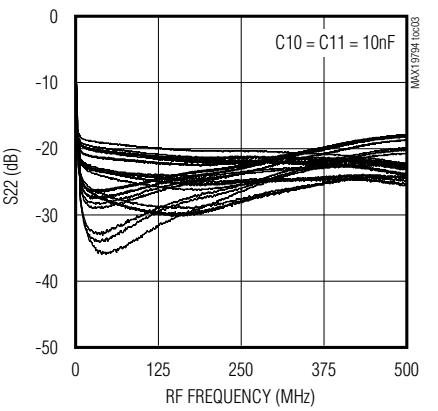
SUPPLY CURRENT vs. V_{CC}



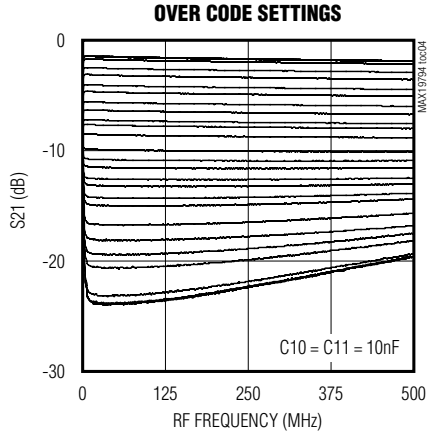
INPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



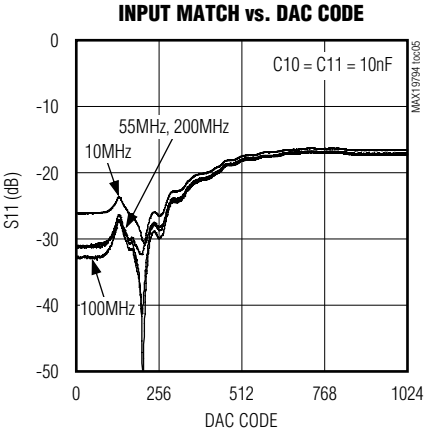
OUTPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



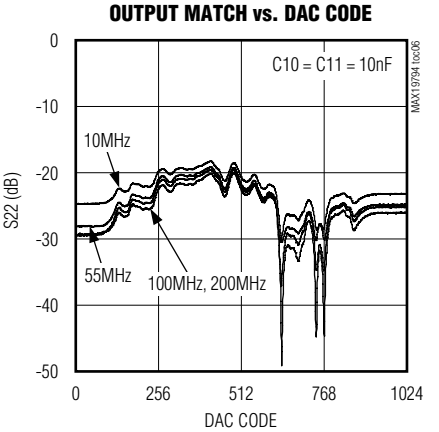
ATTENUATION vs. RF FREQUENCY OVER CODE SETTINGS



INPUT MATCH vs. DAC CODE



OUTPUT MATCH vs. DAC CODE



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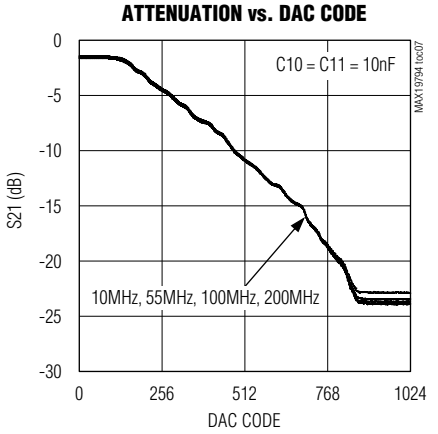

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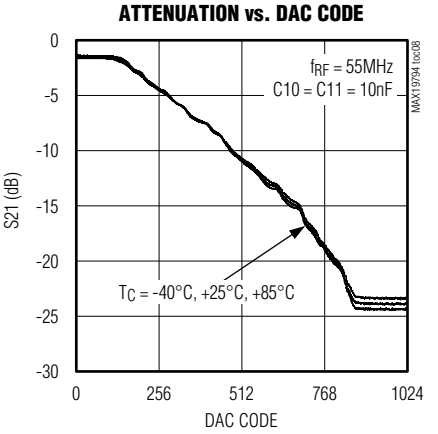
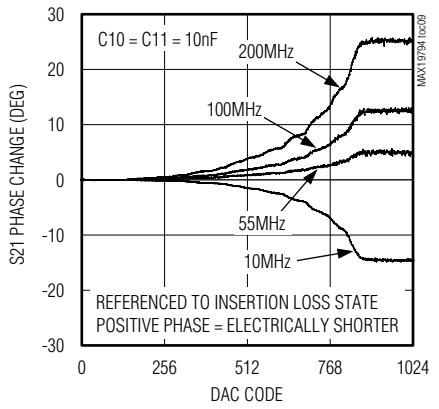
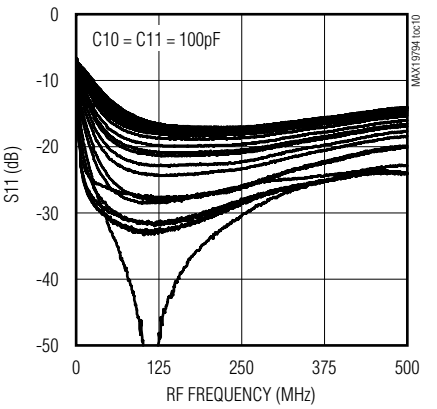


(*Typical Application Circuit*, **V_{CC} = 5.0V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

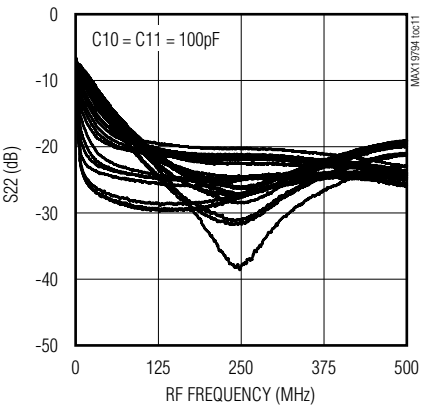
S21 PHASE CHANGE vs. DAC CODE



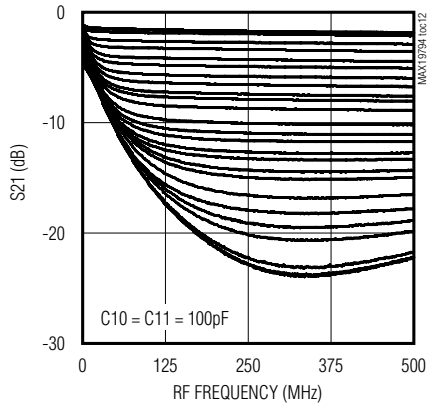
INPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



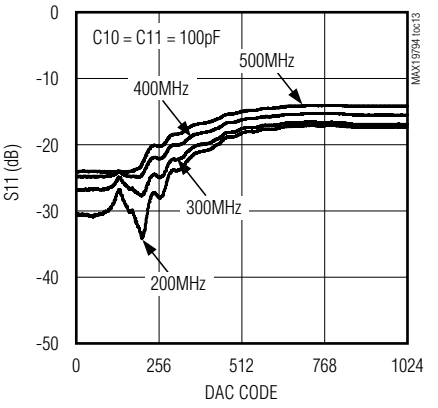
OUTPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



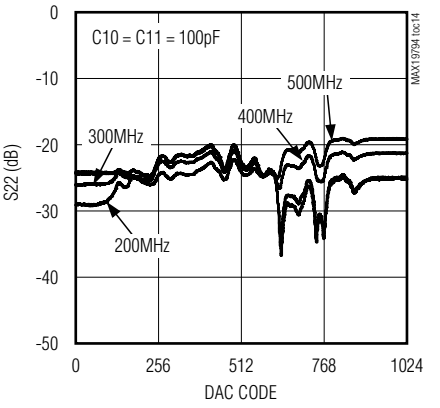
ATTENUATION vs. RF FREQUENCY OVER CODE SETTINGS



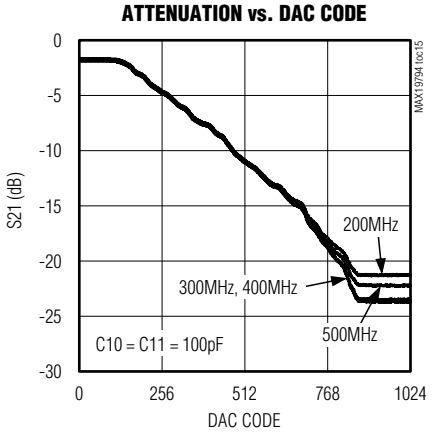
INPUT MATCH vs. DAC CODE



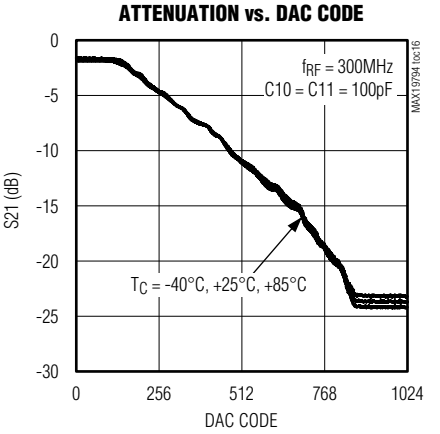
OUTPUT MATCH vs. DAC CODE



ATTENUATION vs. DAC CODE



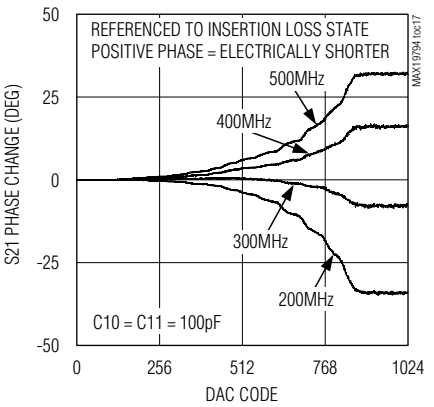
ATTENUATION vs. DAC CODE



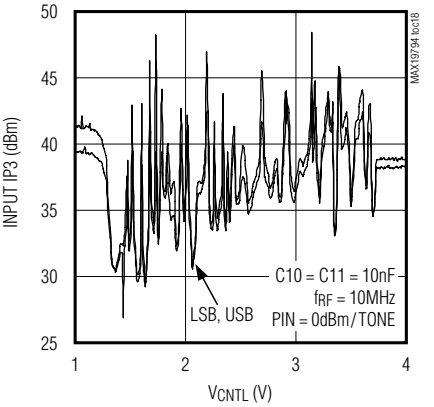
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = 5.0V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

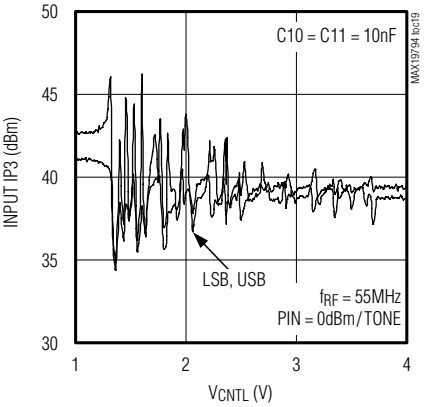
S21 PHASE CHANGE vs. DAC CODE



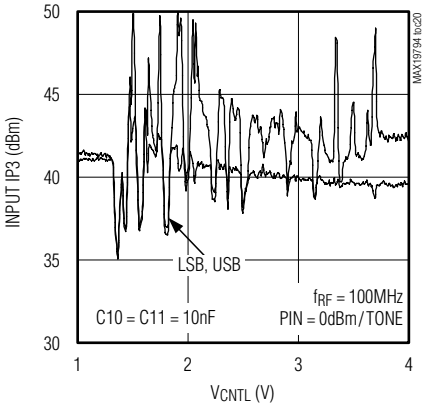
INPUT IP3 vs. V_{CNTL}



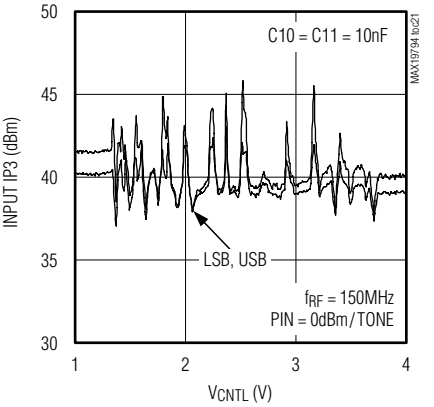
INPUT IP3 vs. V_{CNTL}



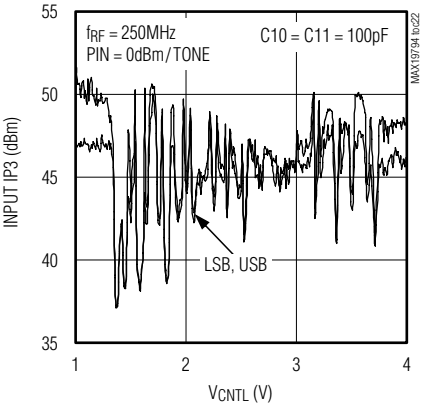
INPUT IP3 vs. V_{CNTL}



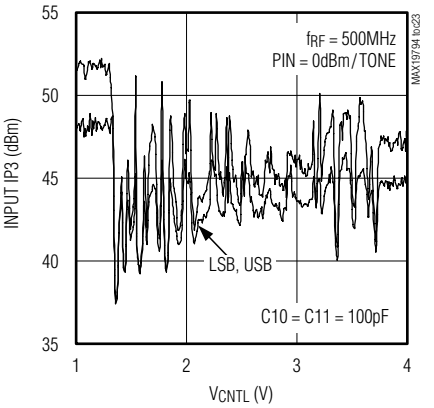
INPUT IP3 vs. V_{CNTL}



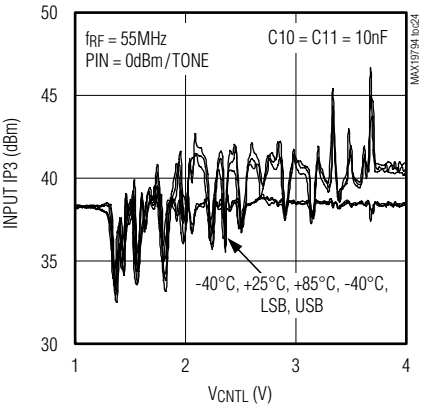
INPUT IP3 vs. V_{CNTL}



INPUT IP3 vs. V_{CNTL}



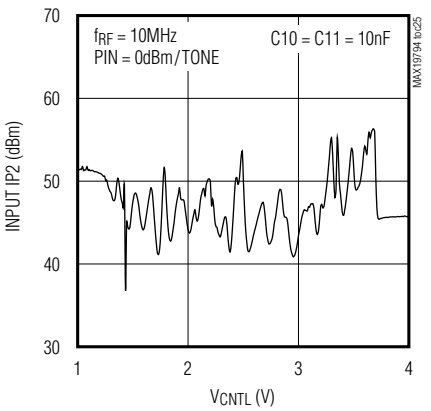
INPUT IP3 vs. V_{CNTL}



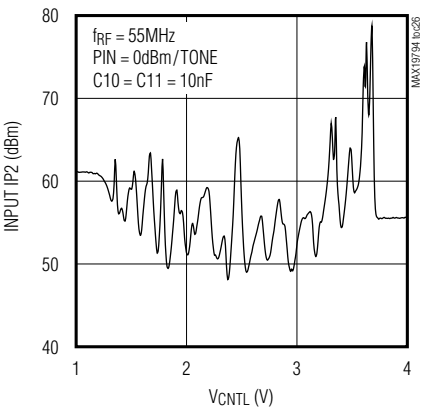
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = 5.0V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = 25°C, unless otherwise noted.).

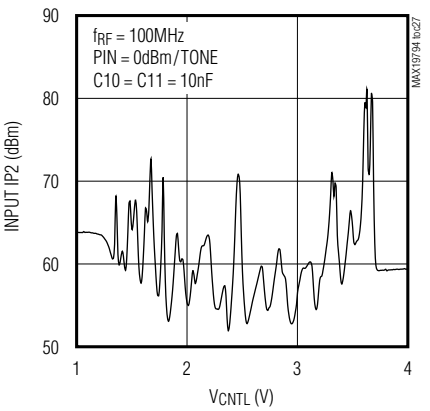
INPUT IP2 vs. V_{CNTL}



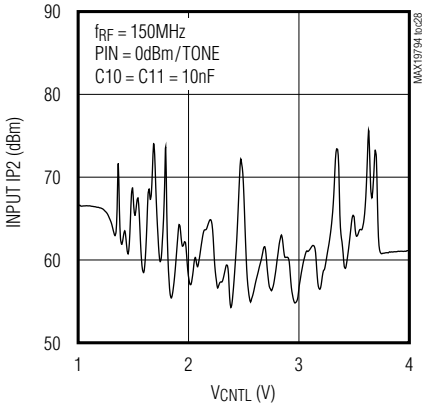
INPUT IP2 vs. V_{CNTL}



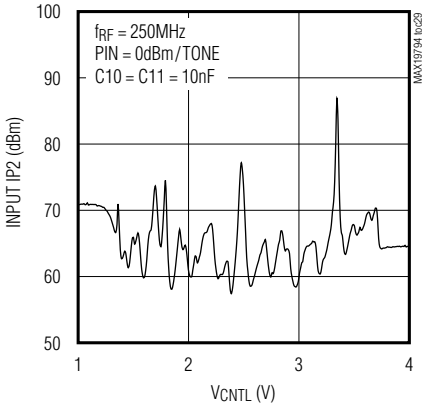
INPUT IP2 vs. V_{CNTL}



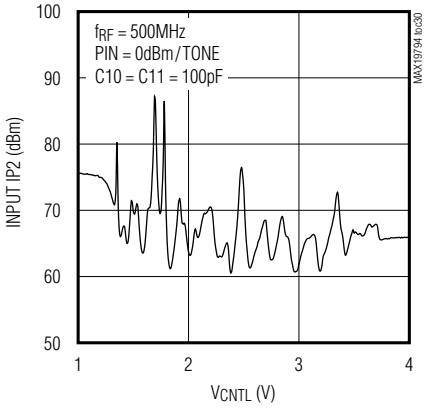
INPUT IP2 vs. V_{CNTL}



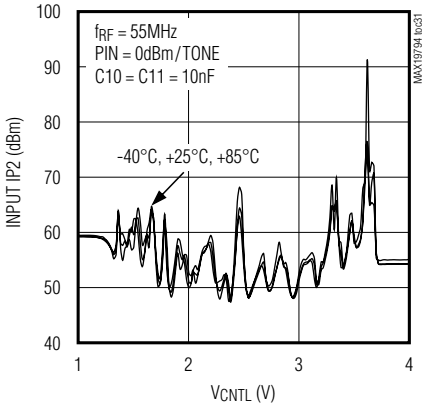
INPUT IP2 vs V_{CNTL}



INPUT IP2 vs V_{CNTL}



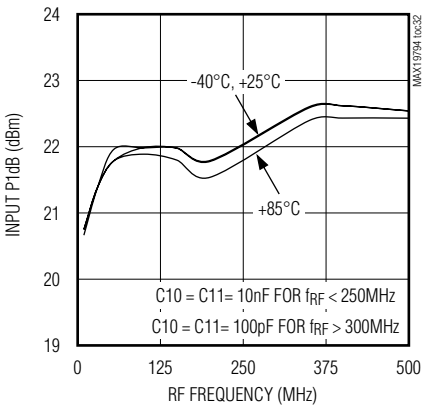
INPUT IP2 vs V_{CNTL}



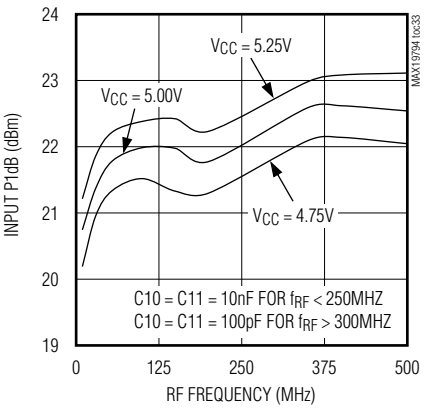
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = 5.0V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = 25°C, unless otherwise noted.).

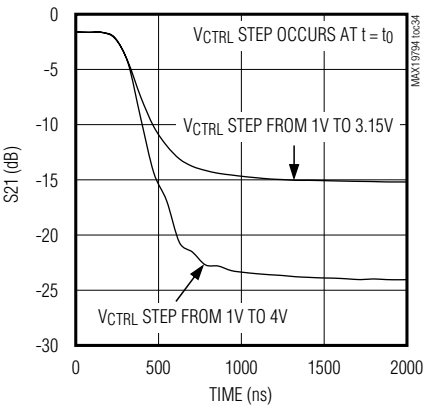
INPUT P1dB vs. RF FREQUENCY



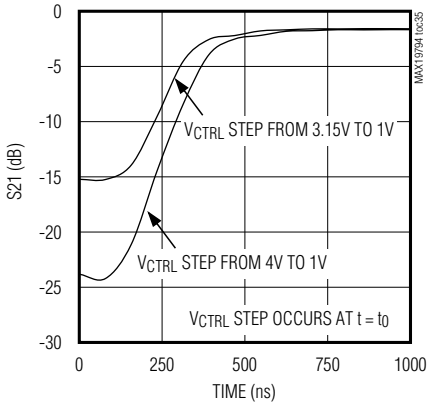
INPUT P1dB vs. RF FREQUENCY



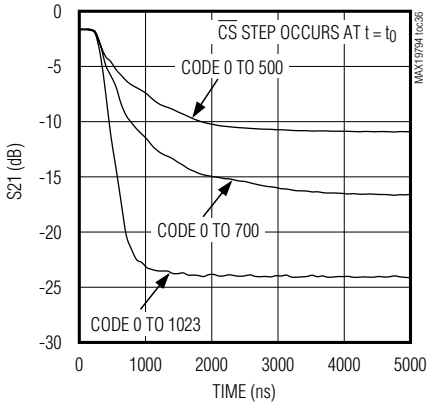
RESPONSE TIME V_{CTRL} STEP



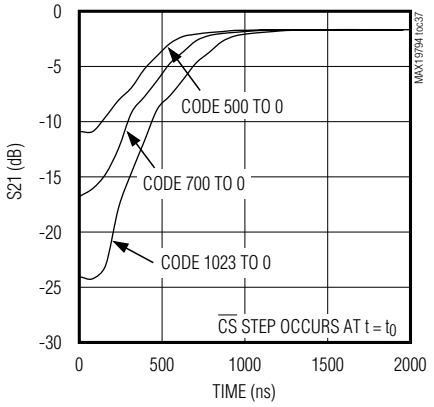
RESPONSE TIME V_{CTRL} STEP



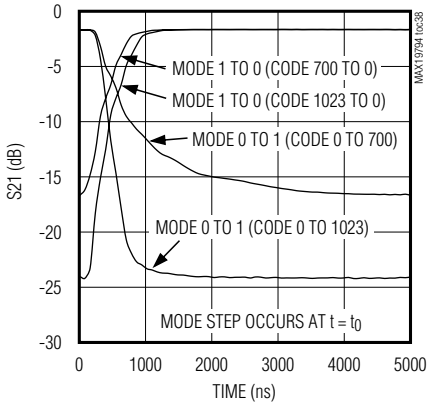
RESPONSE TIME WITH $\overline{CS}$ STEP



RESPONSE TIME WITH $\overline{CS}$ STEP



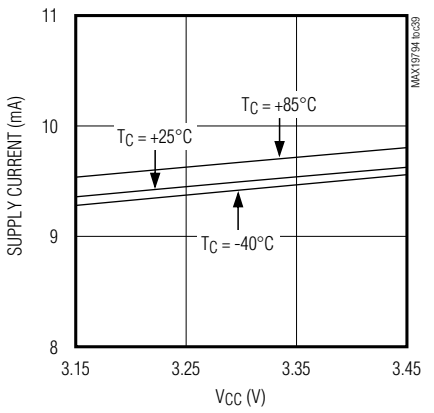
RESPONSE TIME WITH MODE STEP



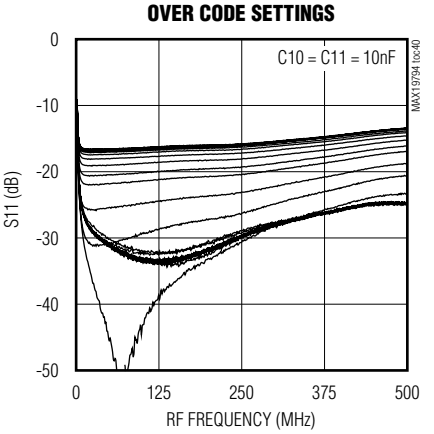
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = 3.3V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

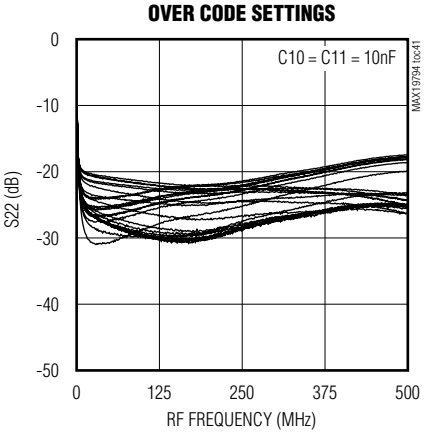
SUPPLY CURRENT vs. V_{CC}



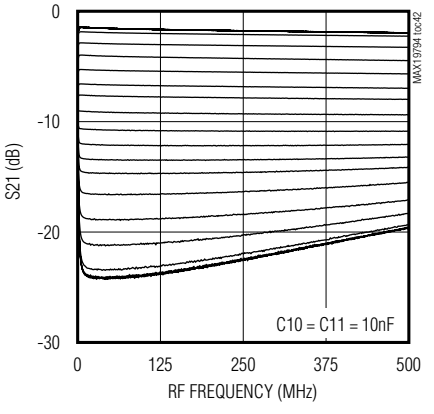
INPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



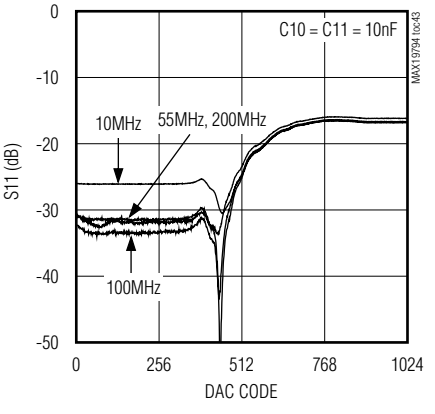
OUTPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



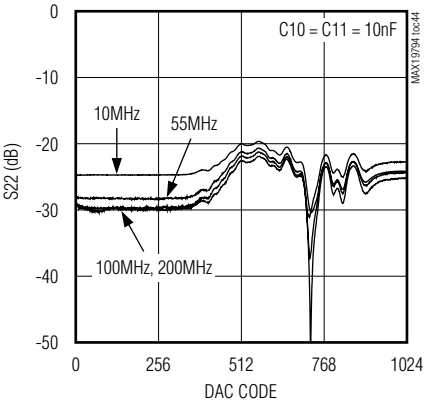
ATTENUATION vs. RF FREQUENCY OVER CODE SETTINGS



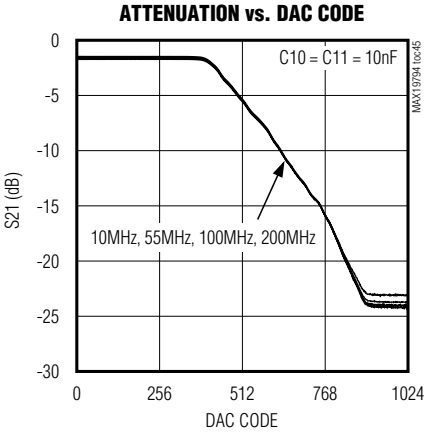
INPUT MATCH vs. DAC CODE



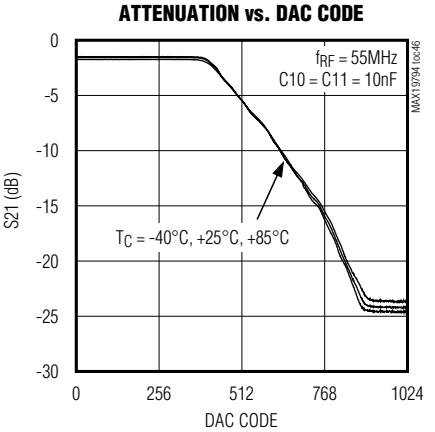
OUTPUT MATCH vs. DAC CODE



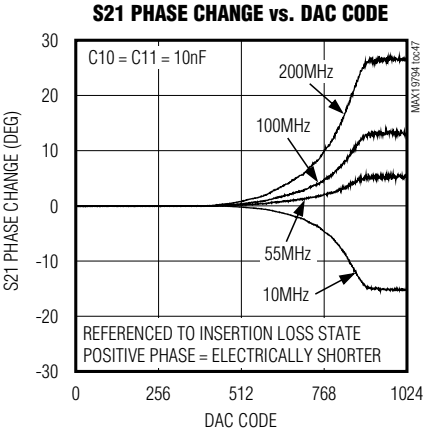
ATTENUATION vs. DAC CODE



ATTENUATION vs. DAC CODE



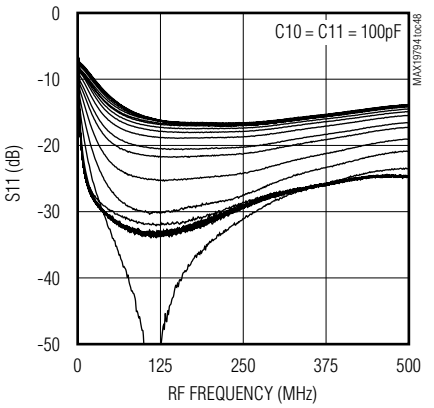
S21 PHASE CHANGE vs. DAC CODE



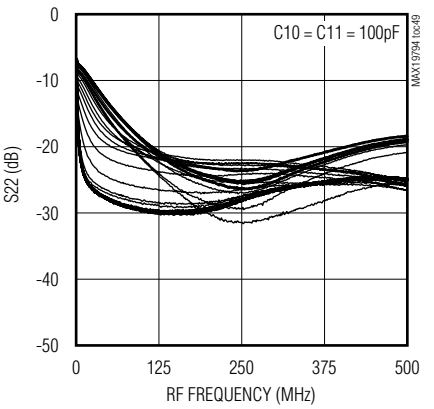
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = 3.3V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

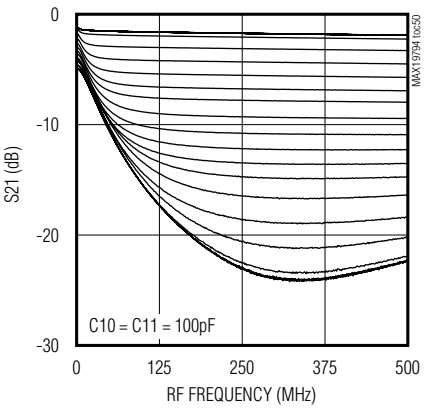
INPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



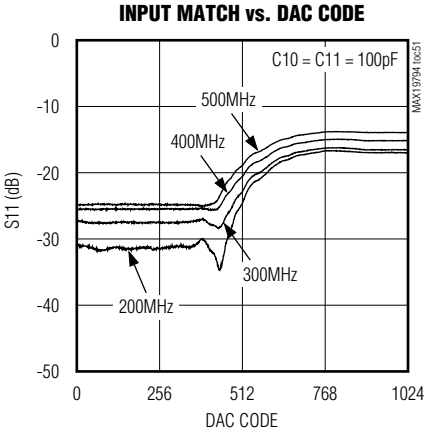
OUTPUT MATCH vs. RF FREQUENCY OVER CODE SETTINGS



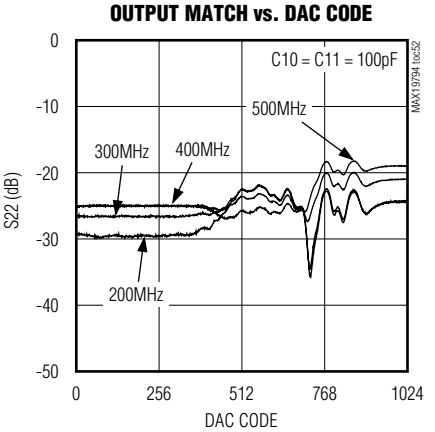
ATTENUATION vs. RF FREQUENCY OVER CODE SETTINGS



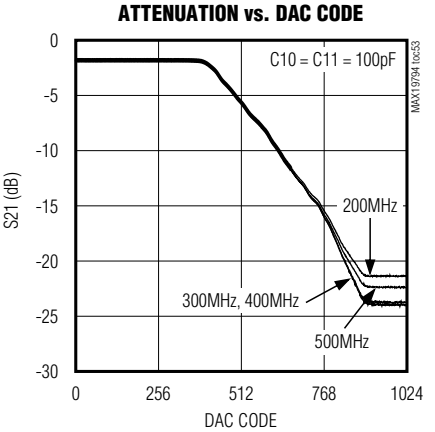
INPUT MATCH vs. DAC CODE



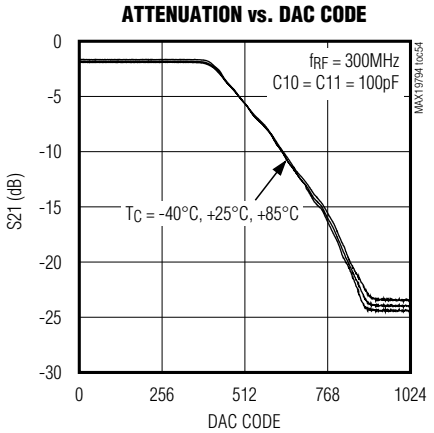
OUTPUT MATCH vs. DAC CODE



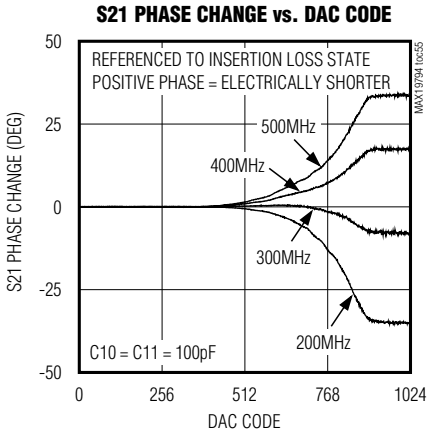
ATTENUATION vs. DAC CODE



ATTENUATION vs. DAC CODE



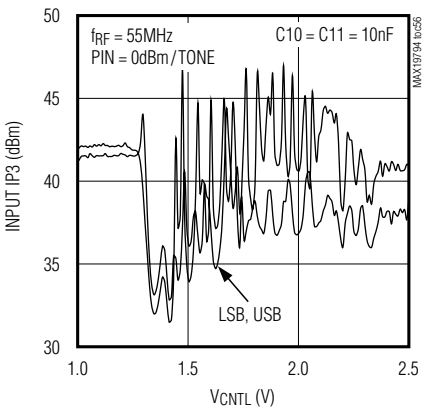
S21 PHASE CHANGE vs. DAC CODE



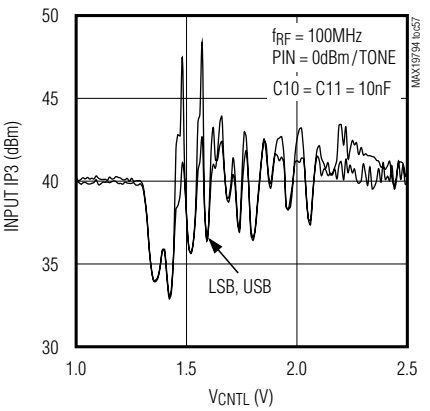
典型工作特性(续)

([*Typical Application Circuit*](), **V_{CC} = 3.3V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

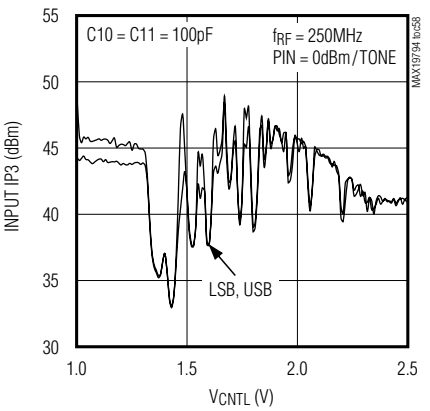
INPUT IP3 vs. V_{CNTL}



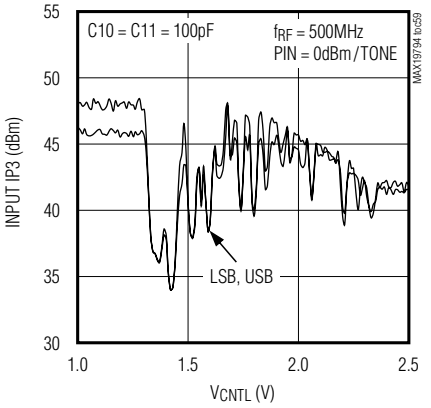
INPUT IP3 vs. V_{CNTL}



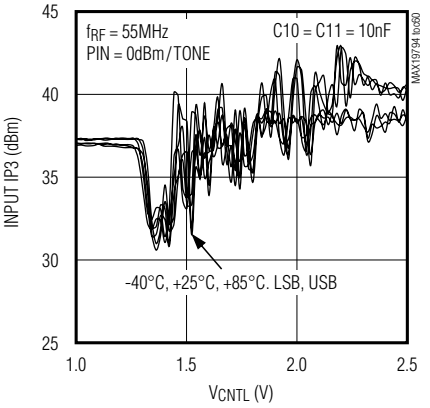
INPUT IP3 vs. V_{CNTL}



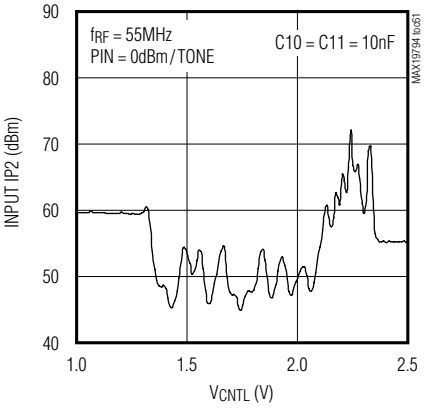
INPUT IP3 vs. V_{CNTL}



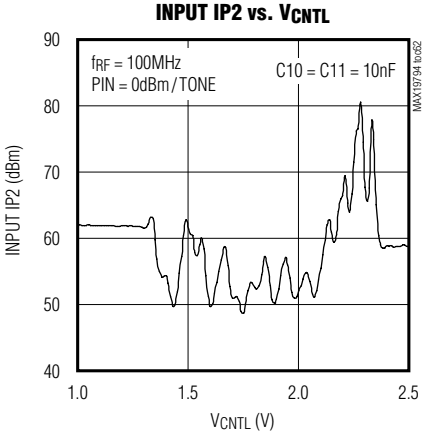
INPUT IP3 vs. V_{CNTL}



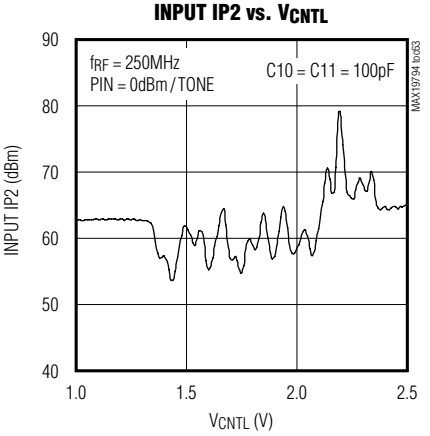
INPUT IP2 vs. V_{CNTL}



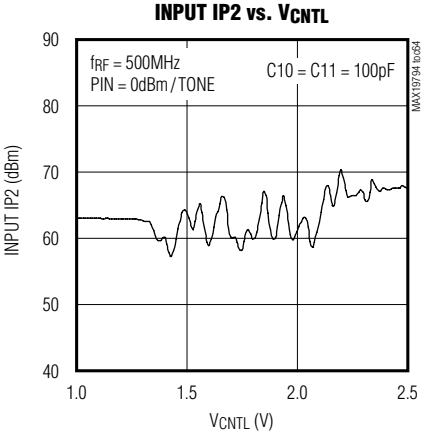
INPUT IP2 vs. V_{CNTL}



INPUT IP2 vs. V_{CNTL}



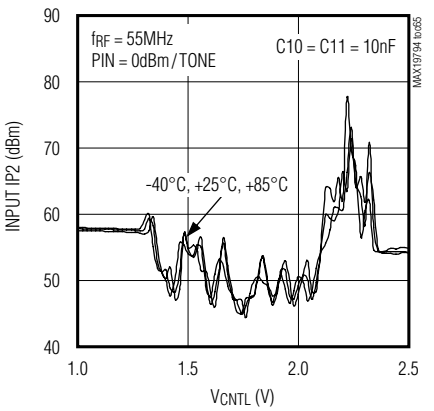
INPUT IP2 vs. V_{CNTL}



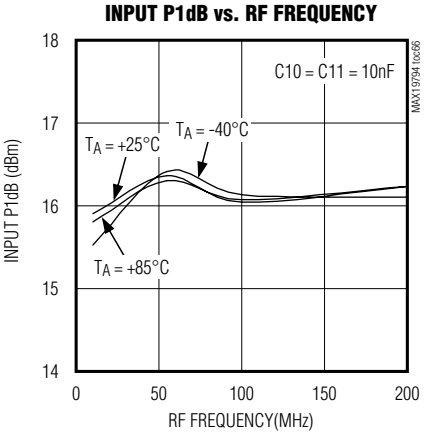
典型工作特性(续)

(*Typical Application Circuit*, **V_{CC} = 3.3V**, configured for single attenuator, RF ports are driven from 50Ω sources and loaded into 50Ω, V_{DAC_LOGIC} = 0V, RDBK_EN = logic 0, V_{CTRL} = 1.0V, P_{IN} = 0dBm, f_{RF} = 55MHz, T_C = +25°C, unless otherwise noted.).

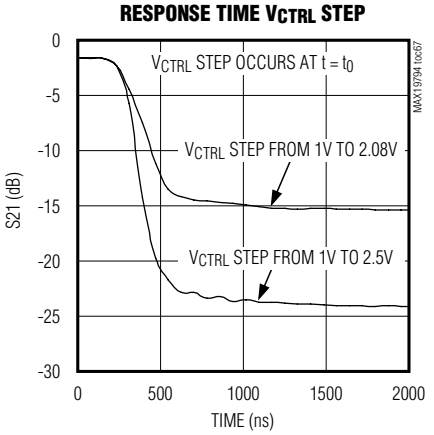
INPUT IP2 vs. V_{CNTL}



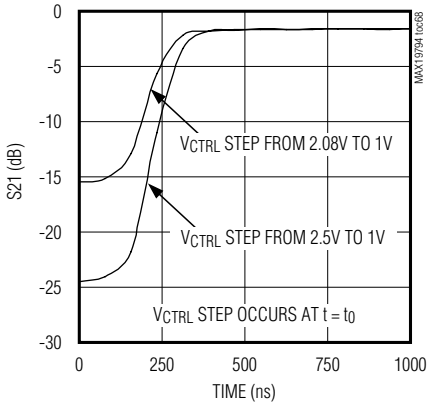
INPUT P1dB vs. RF FREQUENCY



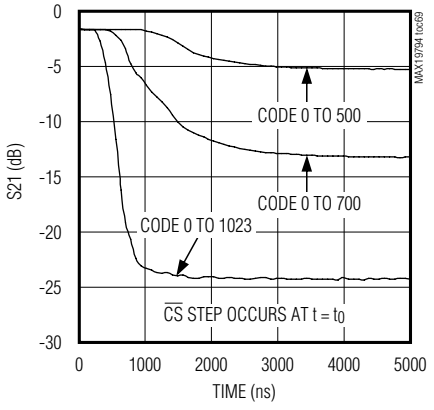
RESPONSE TIME V_{CTRL} STEP



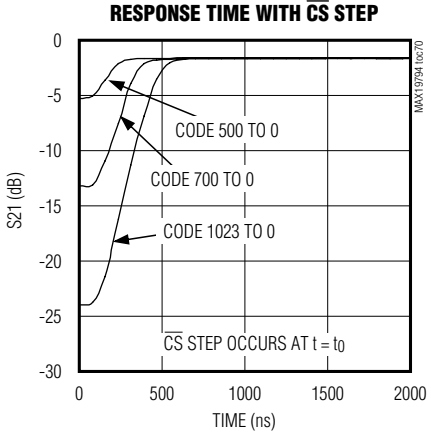
RESPONSE TIME V_{CTRL} STEP



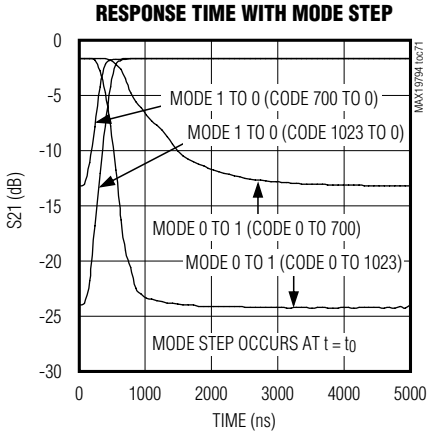
RESPONSE TIME WITH $\overline{CS}$ STEP



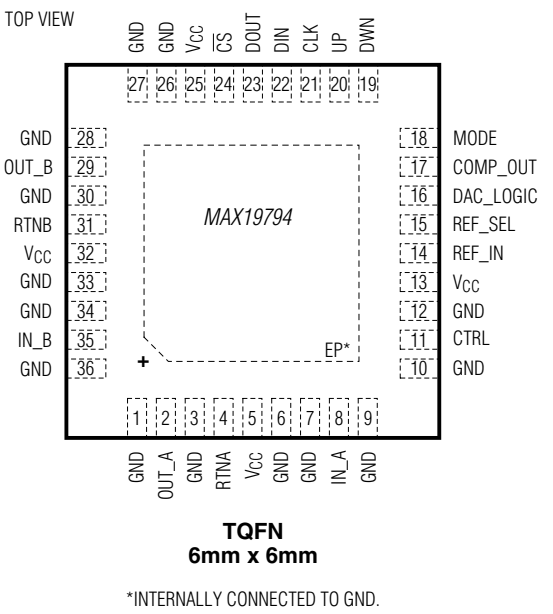
RESPONSE TIME WITH $\overline{CS}$ STEP



RESPONSE TIME WITH MODE STEP



引脚配置



TQFN
6mm x 6mm

*INTERNALLY CONNECTED TO GND.

引脚说明

引脚	名称	说明
1, 3, 6, 7, 9, 10, 12, 26, 27, 28, 30, 33, 34, 36	GND	地，采用低电感布线连接至电路板的接地区域。
2	OUT_A	衰减器A的RF输出，在工作频率范围内由内部匹配至50Ω。使用该引脚时需要隔直流电容；如果不使用该衰减器，可以不连接该引脚。
4, 31	RTNA, RTNB	衰减器的地返回端，这些引脚需要通过一个电容接地，电容应靠近引脚放置。电容选择依据RF工作带宽，详见*典型工作特性*部分。
5	V_{CC}	衰减器A供电电源，通过一个电容和电阻旁路至GND，如*典型应用电路*所示。
8	IN_A	衰减器A的RF输入，在工作频率范围内由内部匹配至50Ω。使用该引脚时需要隔直流电容；如果不使用该衰减器，可以不连接该引脚。
11	CTRL	衰减控制电压输入。**但在测试模式下，不能在该引脚施加任何电压。**必须连接V_{CC}后方可作用控制电压，否则应使用限流电阻，如*应用信息*部分所述。

引脚说明(续)

引脚	名称	说明
13	V_{CC}	模拟电源电压，利用电容旁路至GND，电容尽量靠近器件放置，*参见典型应用电路*。
14	REF_IN	DAC基准电压输入(可选)。
15	REF_SEL	DAC基准电压选择逻辑输入。 逻辑0时，使能片上DAC基准。 逻辑1时，使用片外DAC基准(引脚14)。
16	DAC_LOGIC	DAC逻辑控制输入，参见表1。
17	COMP_OUT	比较器逻辑输出，外部对地连接一个4.7pF电容，以便在比较器状态变化时抑制上升时刻的尖峰脉冲。
18	MODE	衰减器模式控制逻辑输入。 逻辑1，使能衰减器步增控制。 逻辑0，使能衰减器SPI控制。
19	DWN	步降脉冲输入。 每个低电平逻辑脉冲步降一级。
20	UP	步增脉冲输入。 每个低电平逻辑脉冲步增一级。
19, 20	DWN/UP	两个引脚均为逻辑0时，将衰减器复位至最小衰减状态。
21	CLK	SPI时钟输入。
22	DIN	SPI数据输入。
23	DOUT	SPI数据输出。
24	$\overline{CS}$	SPI片选输入。
25	V_{CC}	数字电源，利用电容旁路至GND，电容尽量靠近器件放置，*参见典型应用电路*。
29	OUT_B	衰减器B的RF输出，在工作频率范围内由内部匹配至50Ω。使用该引脚时需要隔直流电容；如果不使用该衰减器，可以不连接该引脚。
32	V_{CC}	衰减器B的供电电源，通过一个电容和电阻旁路至GND，如*典型应用电路*所示。
35	IN_B	衰减器B的RF输入，在工作频率范围内由内部匹配至50Ω。使用该引脚时需要隔直流电容；如果不使用该衰减器，可以不连接该引脚。
—	EP	裸焊盘，内部连接至GND。采用多个接地过孔将该裸焊盘焊接至PCB，使器件热量有效散发至PCB接地区域。为了获得良好的RF性能，也需要多过孔接地，*参见布局考虑*部分。

10MHz至500MHz、双通道、模拟电压可变增益衰减器，内置10位、SPI控制DAC

详细说明

MAX19794为双通道、通用模拟可变增益衰减器(VVA)，设计工作在10MHz至500MHz频率范围的50Ω系统。每路衰减器提供22.4dB衰减范围，线性控制斜率为8dB/V。两路衰减器共用一个模拟控制信号，可以级联产生44.7dB的总动态范围，获得16dB/V的线性控制斜率。也可以使用4线SPI控制内部10位DAC，进而控制两个衰减器。步增/步降功能允许用户控制衰减器按照指令脉冲步进调整增益，无需重新编程SPI接口。

应用信息

衰减控制和特性

器件具有各种不同的工作模式，用于控制模拟衰减器以及部分监测条件。器件可由外部控制电压、内部SPI总线或两者组合进行控制。有关各种不同工作模式的说明，请参考表1。如果器件没有配置在仅由模拟电压控制的模式下，则可通过SPI总线配置多个寄存器，进而控制器件的工作状态。对于使用CTRL的情况，V_{CC} = 5V时，控制电压范围为1V至4V；V_{CC} = 3.3V时，控制电压为1V至2.5V。

每路衰减器可提供高达22.4dB衰减控制范围。在设置插入损耗时，单个衰减器的损耗约为1.5dB。如果需要更大的衰减控制范围，可以串联第二个内部衰减器，提供额外的22.4dB增益控制范围。

片上控制驱动器同时调节两个片上衰减器。建议在CTRL引脚增加一个串联电阻，将电流限制在40mA以下，以便在没有施加V_{CC}的情况下作用控制电压时提供有效保护。采用大于200Ω的串联电阻，能够在+5.0V控制电压范围内提供有效保护。

模拟控制模式

表1中的状态(0，0)，衰减器由作用在器件CTRL引脚的电压控制，禁止片上DAC工作。如果不需要SPI总线控制，可将引脚14-25接地，使器件单纯工作在模拟控制模式。

DAC模式控制

表1中的状态(1，0)，衰减器由片上10位DAC寄存器控制，参见寄存器/模式部分。该工作条件下，CTRL引脚没有施加信号，CTRL引脚的负载应大于100kΩ。DAC由SPI总线装载的寄存器代码和MODE引脚控制。

带报警监测的模拟控制模式

表1中的状态(0，1)，衰减器由作用在器件CTRL引脚的电压控制，参见寄存器/模式部分。该工作条件下，DAC使能并在CTRL引脚施加一个电压。片上开关配置将DAC电压与比较器输入端的CTRL电压进行比较，当VCTRL超过片上DAC电压时，比较器输出COMP_OUT从高电平跳变到低电平。

表1. 衰减器控制逻辑状态

DAC_LOGIC	RDBK_EN (D9, REG3)	内部开关状态	衰减器	10位DAC
0	0	S1 = closed S2, S3, S4 = open	由CTRL (引脚11)的外部模拟电压控制。	Disabled
1	0	S1, S3, S4 = open S2 = closed	由片上DAC控制，引脚11不施加电压。	Enabled
0	1	S1, S3, S4 = closed S2 = open	由CTRL (引脚11)的外部模拟电压控制。将CTRL与DAC输出进行比较，比较器驱动COMP_OUT (引脚17)。	Enabled (update DAC code to estimate CTRL voltage on pin 11)
1	1	S1, S2 = closed S3, S4 = open	由片上DAC控制，DAC输出连接至引脚11。该状态可用于测试DAC输出，**这种条件下，引脚11不能施加任何电压，引脚11负载必须大于100kΩ。**	Enabled

DAC测试模式

表1中的状态(1，1)，衰减器由片上10位DAC寄存器控制，参见*寄存器模式步增/步降控制*部分。该工作条件下，DAC使能，DAC电压作用到CTRL引脚。此时，外部不能在CTRL引脚施加任何信号，CTRL引脚负载应大于100kΩ。该模式仅用于生产过程中对DAC电压进行测试，不推荐用户使用。

寄存器模式步增/步降控制

器件具有四个13位寄存器，用于器件控制。第1位为读/写位，随后是2位地址位，其余10位为相应的数据位。读/写位决定对寄存器执行写操作还是读操作，后续的2个地址位选择进行读/写操作的寄存器。地址位配置参见表2，表3给出了四个寄存器的内容说明。

图1所示为器件内部寄存器的配置，图2所示为SPI总线时序。寄存器0设置所要求的DAC码，寄存器1选择步增码，寄存器2选择步降码。

器件还包括模式控制位(表4)，以及UP和DWN控制(表5)。MODE为0时，寄存器0的内容装载到10位DAC寄存器，设置片上DAC输出。这种情况下，UP和DWN控制引脚对器件没有影响。

MODE 1状况下，送入10位DAC寄存器的有效DAC编码等于：

$$m \times Register\ 1 - n \times Register\ 2$$

式中，m和n分别为UP和DWN控制的累积步进数。

器件上电后，UP和DWN均应置0，将m和n计数器复位为0，使图1所示运算电路的输出编码为10位全0，作用到DAC驱动的10位DAC寄存器。为利用UP (DWN)引脚增大(减小)编码，DWN (UP)引脚必须为高电平，UP (DWN)引脚驱动脉冲应为低电平到高电平的跳变。器件设计在利用UP、DWN步进控制时不产生重叠，所以DAC编码最大为1023或不低于0。关于UP、DWN控制的详细信息，请参见图3。

返回MODE 0时，得到与之前装载到寄存器0相同的10位DAC编码；返回MODE = 1时，得到与之前来自寄存器1和2加法器/乘法器电路的10位DAC编码。

寄存器3用于写模式下设置RDBK_EN寄存器，或在读模式下读取RDBK_EN寄存器和COMP_OUT。

SPI接口

器件可由4线SPI兼容串行接口控制，图2所示为接口时序图。进行写操作时，$\overline{CS}$置为低电平，通过DIN引脚将13位字装载到器件内部。该字节的第一位在写操作下为0，随后2位选择待写入的寄存器地址，参见表2，后续10位是需要写入到所选寄存器的数据。移入13位数据后，$\overline{CS}$由低变高，将10位数据锁存到所选寄存器。如果在成功获取最后一位数据之前将$\overline{CS}$由低拉至高电平，器件将忽略整个写命令。

执行读操作时，第一位移入数据为1，表示读取寄存器。随后2位代表待读取寄存器的地址，参见表2。读操作下，收到A0后，数据开始从DOUT引脚移出。完成10位数据传输，或在传输期间$\overline{CS}$跳变到高电平后，DOUT引脚变为高阻态。

电压基准

器件内部集成了电压基准支持DAC工作，DAC也可配合外部基准工作，表6给出了基准选择的详细信息。

表2. 寄存器地址

R/W	A1	A0	DESCRIPTION
0	0	0	Write to register 0 using DIN
0	0	1	Write to register 1 using DIN
0	1	0	Write to register 2 using DIN
0	1	1	Write to register 3 using DIN
1	0	0	Read from register 0 using DOUT
1	0	1	Read from register 1 using DOUT
1	1	0	Read from register 2 using DOUT
1	1	1	Read from register 3 using DOUT

表3. 寄存器定义

Register 0 (Read/Write 10-Bit DAC Code)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DAC MSB									DAC LSB

Register 1 (Read/Write 10-Bit Step-Up Code)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Step-up MSB									Step-up LSB

Register 2 (Read/Write 10-Bit Step-Down Code)

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Step-down MSB									Step-down LSB

Register 3 Write Bits

RDBK_EN = 使能位，用于驱动COMP_OUT (引脚17)的电压比较器。

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDBK_EN	Not used, set = 0								

Register 3 Read Bits

RDBK_EN = 使能位，用于驱动COMP_OUT (引脚17)的电压比较器。

COMP_OUT = COMP_OUT (引脚17)的读逻辑电平。

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RDBK_EN	COMP_OUT	Not used, set = 0							

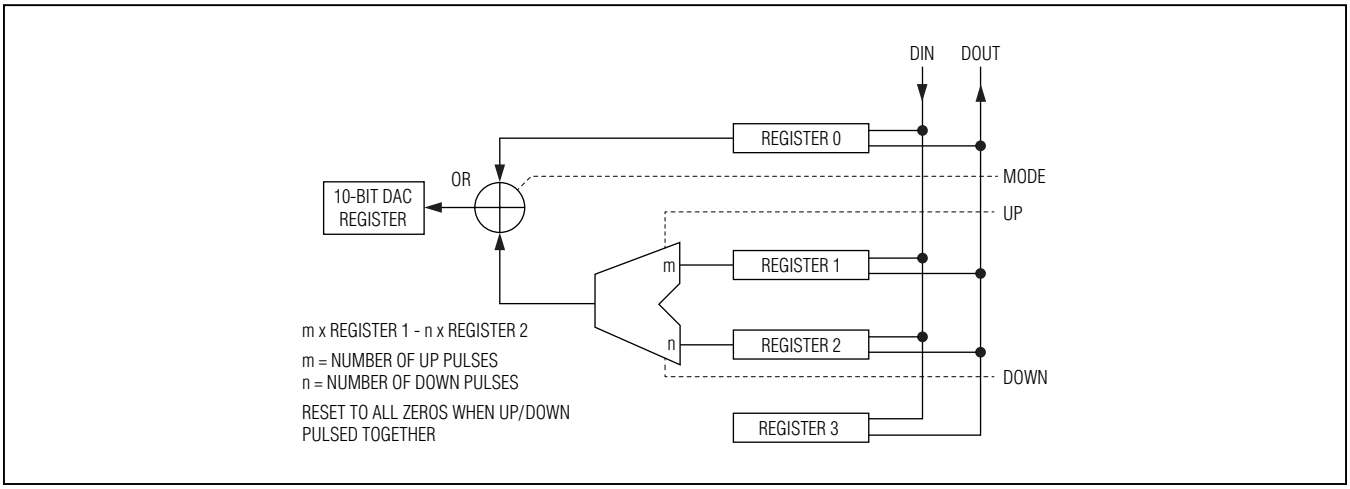


图1. 寄存器配置框图

表4. 衰减器控制模式逻辑状态

MODE (PIN 17)	ATTENUATOR
0	SPI Control Mode (DAC code is located in register 0)
1	Step Control Mode using UP and DWN pins. The step-up code is located in register 1 and step-down code in register 2).

表5. 步进模式逻辑状态(MODE = 1)

UP	DWN	ATTENUATOR
Logic 0	Logic 0	Reset DAC for minimum attenuation state (DAC code = 0000000000).
Logic 0 Pulse	Logic 1	Increase DAC code* by amount located in register 1. UP pulsed from high to low to high (Figure 3).
Logic 1	Logic 0 Pulse	Decrease DAC code* by amount located in register 2. DWN pulsed from high to low to high (Figure 3).

** 连续的UP或DWN步进造成饱和(无编码溢出)。*

表6. REF_SEL逻辑状态

REF_SEL	DAC REFERENCE
0	Uses on-chip DAC reference.
1	User provides off-chip DAC reference voltage on REF_IN (pin 14).

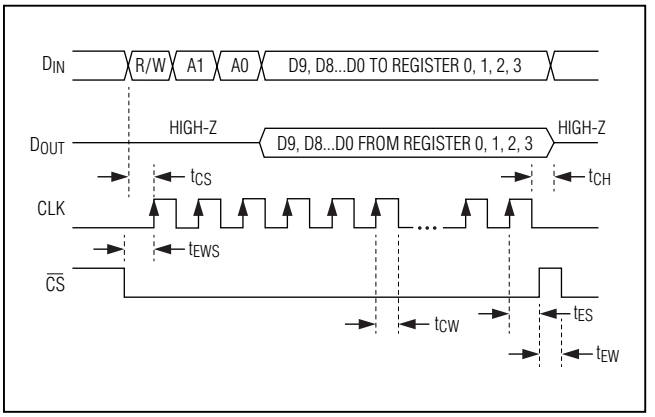


图2. SPI时序图

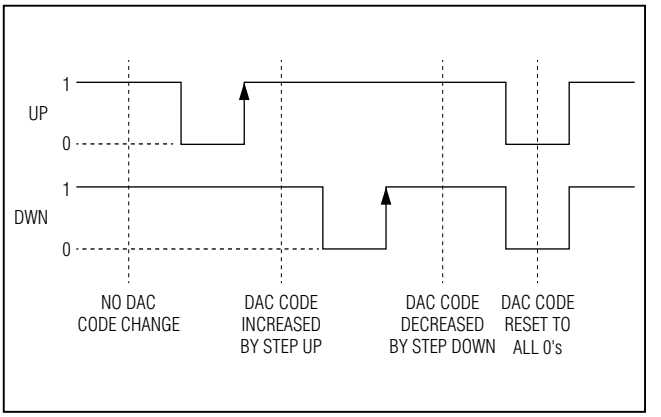


图3. UP/DWN控制图 (MODE = 1)

表7. 典型应用电路元件

DESIGNATION	QTY	DESCRIPTION	
C1, C2, C4	3	0.01µF ±5% 50V X7R ceramic capacitors (0402).	
C3	0	Not installed for two attenuators in cascade	
C5–C9	5	1000pF ±5% 50V COG ceramic capacitors (0402)	
C10, C11	2	10MHz to 200MHz	0.01µF ±10% 50V X7R ceramic capacitors (0402)
		250MHz to 500MHz	100pF ±5% 50V COG ceramic capacitors (0402)
C12	1	120pF ±5% 50V COG CER CAP (0402).Provides some external noise filtering along with R3.	
C13	0	Not installed. A 4.7pF capacitor could be used to reduce any potential rise time glitching when the comparator changes state.	
R1*, R2*	2	10Ω ±5% resistor (0402)	
R3	1	200Ω ±5% resistor (0402). This resistor is used to provide some lowpass noise filtering when used with C12. The value of R3 slows down the response time. R3 also provides protection for the device in case V_{CTRL} is applied without V_{CC} present.	
U1	1	MAX19794	

** 在V_{CC}引脚额外增加2个10Ω电阻，分别与C5和C6串联，否则应采用独立的电源层。*

布局考虑

对于任何RF/微波电路来说，合理设计PCB至关重要。RF信号线应尽可能短，以减小损耗、辐射和寄生电感。为获得最佳性能，接地引脚须直接与封装底部的裸焊盘连接。裸焊盘必须通过器件底部的多个过孔连接到电路板的接地区域，以获得良好的RF和散热通路。将器件封装底部的裸焊盘焊接至PCB。

RF地返回电容

器件需要连接RF地返回电容：C10和C11。这些电容有助于在所要求的RF带宽内优化动态范围和频响平坦度。表7列出了推荐电容，性能测试结果请参考*典型工作特性*部分。

10MHz至500MHz、双通道、模拟电压可变增益衰减器，内置10位、SPI控制DAC

电源旁路

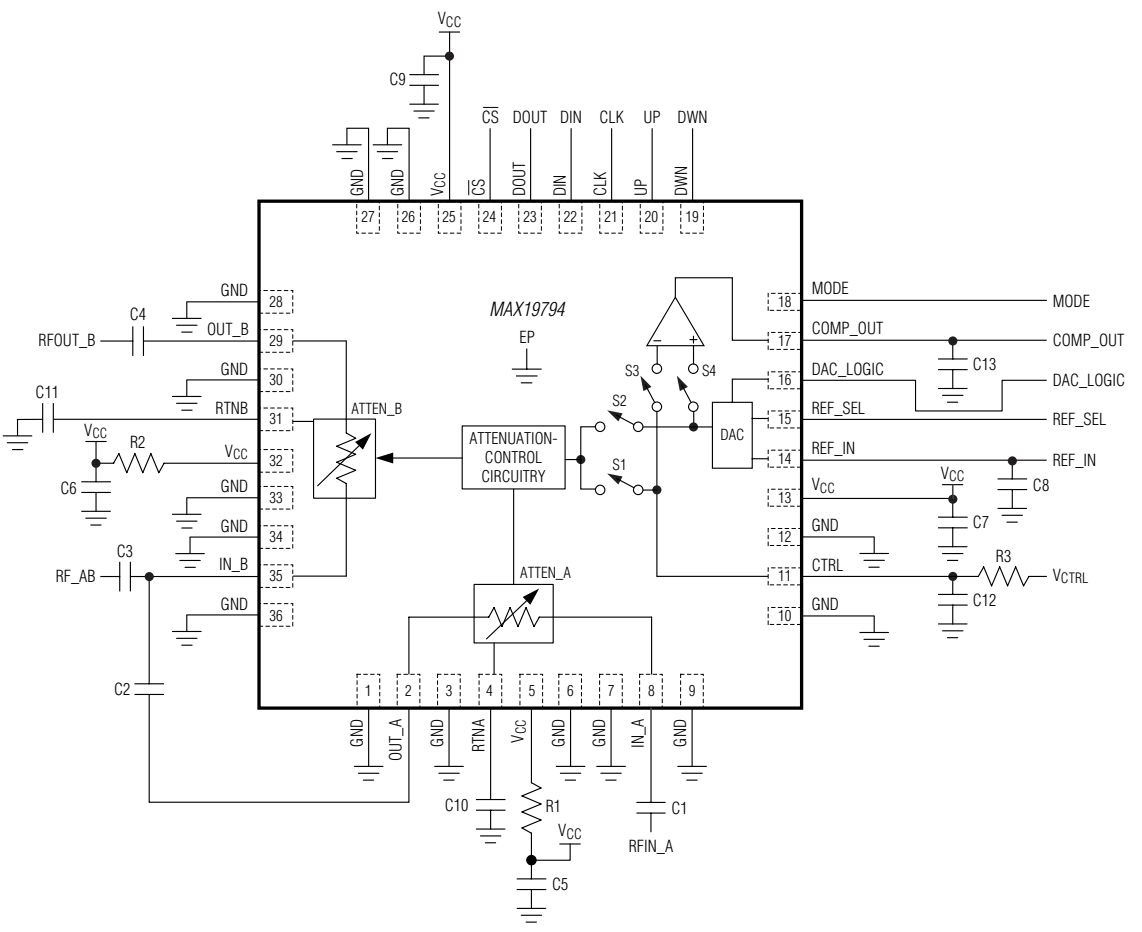
合理的电源旁路对高频电路的稳定性至关重要，利用电容旁路每个V_{CC}引脚，电容尽量靠近器件放置，小容值电容距离器件最近。详细信息请参见*典型应用电路*和表7。

裸焊盘的RF和散热考虑

器件采用36引脚、TQFN封装，其裸焊盘(EP)提供了至管芯的低热阻通路。通过该裸焊盘提供IC至PCB的导热通道非常重要。

此外，为EP提供低电感RF接地通路，EP必须直接或通过一系列电镀过孔焊接到PCB的接地区域。将裸焊盘焊接到地对于改善散热同样重要，尽可能使用连续的地层。

典型应用电路



NOTE: FOR ATTENUATOR A ONLY CONFIGURATION, REMOVE C3 AND MOVE C2 DIAGONALLY TO CONNECT PIN 2 TO THE OUTPUT CONNECTION RF_AB.
FOR ATTENUATOR B ONLY CONFIGURATION, REMOVE C2.
FOR CASCADED CONFIGURATION, REMOVE C3 AND USE C2 TO CONNECT OUT_A TO IN_B.

10MHz至500MHz、双通道、模拟电压可变增益衰减器，内置10位、SPI控制DAC

定购信息

器件	温度范围	引脚-封装
MAX19794ETX+	-40°C至+100°C	36 TQFN-EP*
MAX19794ETX+T	-40°C至+100°C	36 TQFN-EP*

+表示无铅(Pb)/符合RoHS标准的封装。
**EP = 裸焊盘。*
T = 卷带包装。

芯片信息

PROCESS: BiCMOS

封装信息

如需最近的封装外形信息和焊盘布局(占位面积)，请查询china.maximintegrated.com/packages。请注意，封装编码中的“+”、“#”或“-”仅表示RoHS状态。封装图中可能包含不同的尾缀字符，但封装图只与封装有关，与RoHS状态无关。

封装类型	封装编码	外形编号	焊盘布局编号
36 TQFN	T3666+2	21-0141	90-0049

10MHz至500MHz、双通道、模拟电压可变增益衰减器，内置10位、SPI控制DAC

修订历史

修订号	修订日期	说明	修改页
0	6/12	最初版本。	—

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