Data Sheet

ADMV4630

14.0 GHz to 14.5 GHz, SATCOM, Ku Band Upconverter

FEATURES

- IF to Ku band upconverter with integrated PLL
- RF output frequency range: 14.0 GHz to 14.5 GHz
- Internal LO frequency range: 8.7 GHz to 10.7 GHz
- Noise floor density: <−140 dBm/Hz
- Matched 50 Ω single-ended RF output and IF input
- On-chip power detector
- On-chip ADC
- Provides transmitter synthesizer lock detect
- Programmable at 20 MHz via 4-wire SPI interface
- Transmitter mute function
- 40-lead, 6 mm × 6 mm LFCSP package

APPLICATIONS

- SATCOM user terminals

FUNCTIONAL BLOCK DIAGRAM

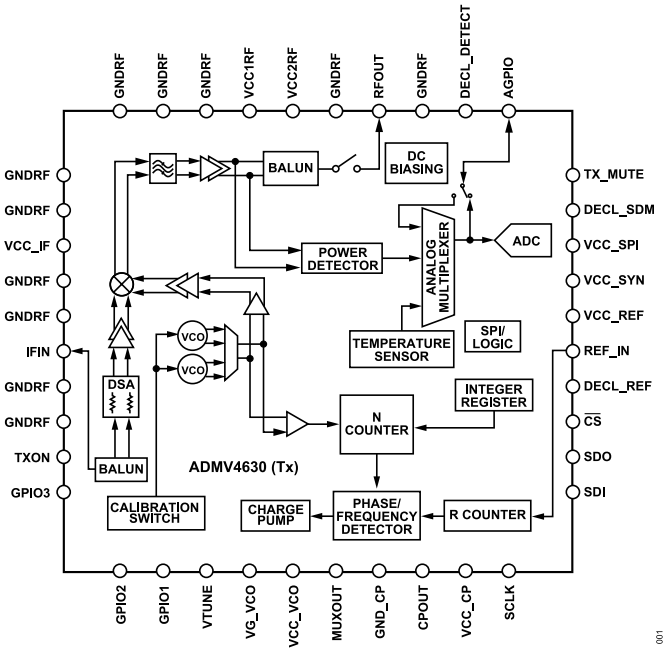

Figure 1.

GENERAL DESCRIPTION

The ADMV4630 is a Ku band upconverter optimized for various satellite communication (SATCOM) user terminals that operate in the 14.0 GHz to 14.5 GHz frequency range.

The ADMV4630 local oscillator (LO) signal is generated internally via the on-chip Integer N (INT) synthesizer. The internal synthesizer enables LO frequency coverage from 8.7 GHz to 10.7 GHz. The input intermediate frequency (IF) signals from 3 GHz to 5 GHz are upconverted to an RF of 14.0 GHz to 14.5 GHz. The chip includes filtering to attenuate both the LO feedthrough and unwanted lower sideband. The chip also includes a digital step attenuator at the IF input to provide up to 31 dB of gain control range with 1 dB steps to adjust for preceding cable losses. The transmitter output is automatically muted if the synthesizer becomes unlocked.

The digital serial peripheral interface (SPI) allows fast frequency and gain programming. In addition to the digital SPI control, an analog control pin (TX_MUTE) quickly powers down all circuits and places the receiver in standby mode for power saving. Another analog general-purpose input/output (AGPIO) pin can be used either as an input to be read by the on-chip analog-to-digital converter (ADC), or as an analog output for proportional to absolute temperature (PTAT) voltages. There are also three digital GPIO pins that output logic levels to control external devices using the SPI.

The ADMV4630 upconverter comes in a compact, thermally enhanced, 6 mm × 6 mm, 40-lead lead frame chip scale package (LFCSP). The ADMV4630 operates over the −40°C to +85°C case temperature range.

Rev. B

TABLE OF CONTENTS

REVISION HISTORY

2/2024—Rev. A to Rev. B

Changed Master to Controller (Throughout) ... 1
Changes to Table 4 ... 6
Added Figure 29, Renumbered Sequentially ... 12

7/2022—Revision A: Initial Version

...

SPECIFICATIONS

T_A = 25°C, IF = 4 GHz, VCC = VCC_IF = VCC_VCO = VCC_CP = VCC_REF = VCC_SYN = VCC_SPI = VCC2RF = VCC1RF = 3.3 V, digital signal attenuation (DSA) Register 0x300 = 31, clock reference input power = 3 dBm, upper sideband selected, unless otherwise noted. VCC refers to the voltage of all VCC_xxx pins.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF OUTPUT FREQUENCY RANGE		14.0		14.5	GHz
LO FREQUENCY RANGE		8.7		10.7	GHz
LO Lock Time				370	µs
LO REFERENCE FREQUENCY			25		MHz
REFERENCE INPUT POWER		0		5	dBm
LO PHASE NOISE PERFORMANCE					
1 kHz Offset from Carrier			−85		dBc/Hz
10 kHz Offset from Carrier			−90		dBc/Hz
100 kHz Offset from Carrier			−95		dBc/Hz
1 MHz Offset from Carrier			−125		dBc/Hz
10 MHz Offset from Carrier			−135		dBc/Hz
100 MHz Offset from Carrier	Measured at the RF output		−138		dBc/Hz
Integrated Single Sideband Phase Noise Performance	1 kHz to 20 MHz		−34		dBc/Hz
IF INPUT FREQUENCY RANGE		3		5	GHz
IF Channel Bandwidth		±62			MHz
IF Input Power				4	dBm
IF UPCONVERTER PERFORMANCE					
Maximum Conversion Gain		16	19		dB
Gain Control Range			31		dB
Gain Flatness	Over 20 MHz bandwidth	−0.15		+0.15	dB/20 MHz[1]
Output Noise Density				−140	dBm/Hz
Output Third-Order Intercept (IP3)	Minimum attenuation	19.5	22		dBm
Output 1 dB Compression Point (P1dB)	Minimum attenuation		11		dBm
Sideband Rejection	Noise floor limited	70	95		dBc
LO to RF Feedthrough			−40	−30	dBm
Transmitter Mute On/Off Ratio	Output switch only	25			dB
Transmitter Mute On/Off Ratio	Switch plus power-down LO	40			dB
Adjacent Channel Power Ratio (ACPR)			−35		dBc
Error Vector Magnitude (EVM)			2.0		%
TRANSMITTER DETECTOR PERFORMANCE					
Input Frequency		14.0		14.5	GHz
Input Power Range	At RFOUT pin	−2		+13	dBm
Detector Accuracy	Not calibrated		±1		dB
ADC PERFORMANCE					
ADC Bits			8		Bits
ADC Sampling Rate			100		kHz
POWER INTERFACE					
Power Supply (VCC_xxx)[2]		3.135	3.3	3.465	V
VCC_IF Supply Current			60		mA
VCC_VCO Supply Current			80		mA
VCC_CP Supply Current			15		mA
VCC_REF Supply Current			2		mA
VCC_SYN Supply Current			100		mA
VCC_SPI Supply Current			3.5		mA

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VCC2RF Supply Current			80		mA
VCC1RF Supply Current			40		mA
VCC Total Current			381		mA
Total Power Dissipation				1.7	W
Mute Time				15	µs
Unmute Time				15	µs

[1] dB/20 MHz is gain flatness over 20 MHz bandwidth.

[2] VCC_xxx = VCC_IF = VCC_VCO = VCC_CP = VCC_REF = VCC_SYN = VCC_SPI = VCC2RF = VCC1RF = 3.3 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	
VCC_IF, VCC_VCO, VCC_REF, VCC_CP, VCC_SYN, VCC_SPI, VCC2RF, VCC1RF	4.3 V
IF Input Power	5 dBm
Reference Clock Input Power	12 dBm
Junction Temperature	125°C
Moisture Sensitivity Level (MSL)[1]	3
Peak Reflow Temperature	260°C
Operating Case Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
ESD Sensitivity	
Human Body Model (HBM)	1500 V
Field Induced Charged Device Model (FICDM)	250 V

[1] Based on IPC/JEDEC J-STD-20 MSL classifications.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient (or die to ambient) thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction to case (or die to package) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1, 2]	Unit
CP-40-7[1]	30.7	1.1	°C/W

[1] The thermal impedance simulated values are based on a JEDEC 2S2P test board with 6 mm × 6 mm thermal vias. Refer to JEDEC standard JESD51-2 for additional information.

[2] The cold plate of the θ_{JC} bottom is attached to the bottom side of the PCB using a 100 µm thermal interface material (TIM) (3.56 W/mK).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

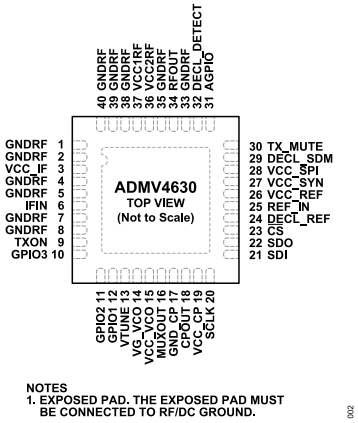

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 5, 7, 8, 33, 35, 38, 39, 40	GNDRF	Grounds. Connect these pins to a low impedance ground plane.
3	VCC_IF	3.3 V Power Supply Connections for IF Section. Decouple the VCC_IF pin with 10 pF and 1000 pF as close as possible to the pin.
6	IFIN	IF Inputs. This pin is internally dc grounded and must be ac-coupled.
9	TXON	Power-Up Pin for Transmitter Chip. Pull the TXON pin to a logic high level in normal operation. Driving the TXON pin to a logic low level disables the chip.
10	GPIO3	General-Purpose Input/Output (GPIO). This pin provides additional digital control line and can be configured to be an input or output, high (3.3 V) or low logic level.
11	GPIO2	GPIO. This pin provides an additional digital control line and can be configured to be an input or output, high (3.3 V) or low logic level.
12	GPIO1	GPIO. This pin provides an additional digital control line and can be configured to be an input or output, high (3.3 V) or low logic level.
13	VTUNE	Voltage Control Oscillator (VCO), Pin Tuning Voltage. This pin is driven by the output of the loop filter.
14	VG_VCO	VCO Internal Node for DC Decoupling. Decouple the VG_VCO pin with 0.1 µF as close as possible to the pin.
15	VCC_VCO	3.3 V Power Supply Connections for VCO. Connect a low noise source power supply to the VCC_VCO pin and decouple this pin with 10 pF and 1000 pF as close as possible to the pin.
16	MUXOUT	Multiplexer Output. See the Register Details section.
17	GND_CP	Multiplexer Output Port.
18	CPOUT	Charge Pump Output Pin.
19	VCC_CP	3.3 V Power Supply Connections for Charge Pump. Decouple the VCC_CP pin with 10 pF and 1000 pF as close as possible to the pin.
20	SCLK	Serial Clock. This pin is the clock input for the SPI interface.
21	SDI	Serial Data Input. See the SPI Configuration section.
22	SDO	Serial Data Output. See the SPI Configuration section.
23	$\overline{CS}$	Chip Select Pin.
24	DECL_REF	Reference Decoupling Pin. Decouple this pin with 0.47 µF and 1000 pF as close as possible to the pin.
25	REF_IN	Reference Frequency Input.
26	VCC_REF	3.3 V Power Supply Connections for Reference. Decouple the VCC_REF pin with 100 pF and 1000 pF as close as possible to the pin.
27	VCC_SYN	3.3 V Power Supply Connections for Synthesizer. Decouple the VCC_SYN pin with 100 pF and 1000 pF as close as possible to the pin.
28	VCC_SPI	3.3 V Power Supply Connections for SPI Control. Decouple the VCC_SPI pin with 100 pF and 1000 pF as close as possible to the pin.
29	DECL_SDM	Internal Low Dropout Regulator (LDO) Decoupling Pin. Decouple the DECL_SDM pin with 0.47 µF and 1000 pF as close as possible to the pin.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 4. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
30	TX_MUTE	Transmitter Output Switch Disable Pin. Drive the TX_MUTE pin to a logic low level in normal operation. Pulling the TX_MUTE pin to a logic high level disables the transmitter output.
31	AGPIO	Bidirectional Analog GPIO. This pin can be configured to be the input or to be the output of the internal ADC. See the AGPIO Control Register section (Register 0x301).
32	DECL_DETECT	Detector Decoupling Pin. Decouple this pin with 0.47 µF as close as possible to the pin.
34	RFOUT	RF Output.
36	VCC2RF	3.3 V Power Supply Connections for RF Section. Decouple the VCC2RF pin with 10 pF and 1000 pF as close as possible to the pin.
37	VCC1RF	3.3 V Power Supply Connections for RF Section. Decouple the VCC1RF pin with 10 pF and 1000 pF as close as possible to the pin.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

TYPICAL PERFORMANCE CHARACTERISTICS

MINIMUM ATTENUATION PERFORMANCE: DSA (REGISTER 0X300) = 31

T_A = 25°C, IF = 4 GHz, VCC = 3.3 V, clock reference input power = 3 dBm, upper sideband selected, unless otherwise noted.

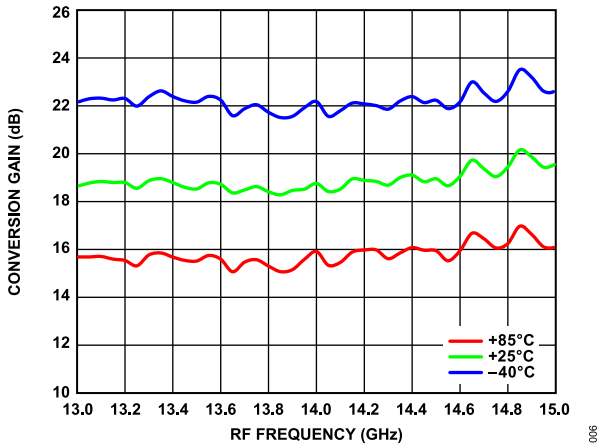

Figure 3. Conversion Gain vs. RF Frequency over Temperature

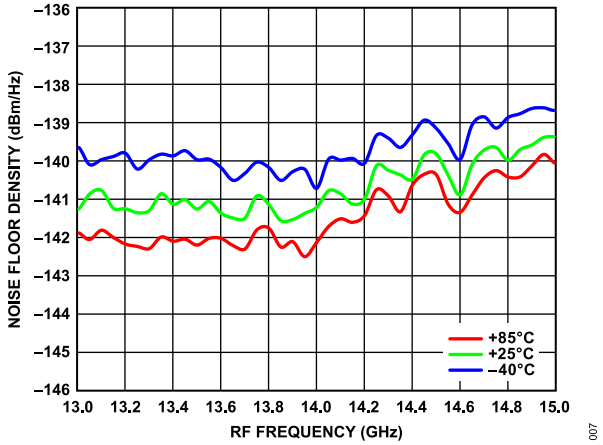

Figure 4. Noise Floor Density vs. RF Frequency over Temperature

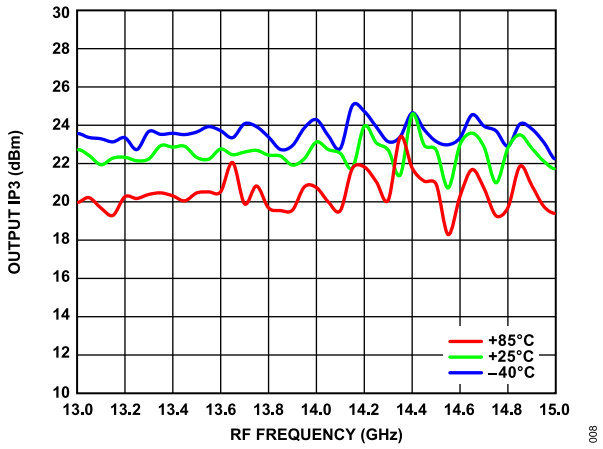

Figure 5. Output IP3 vs. RF Frequency over Temperature

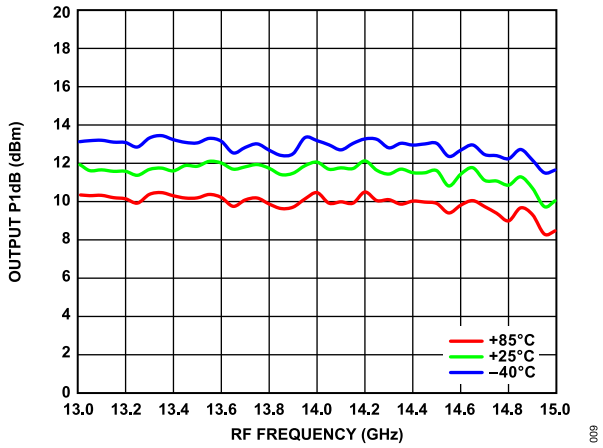

Figure 6. Output P1dB vs. RF Frequency over Temperature

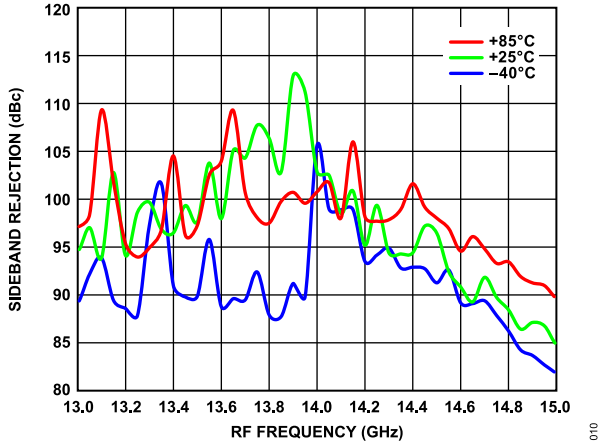

Figure 7. Sideband Rejection vs. RF Frequency over Temperature

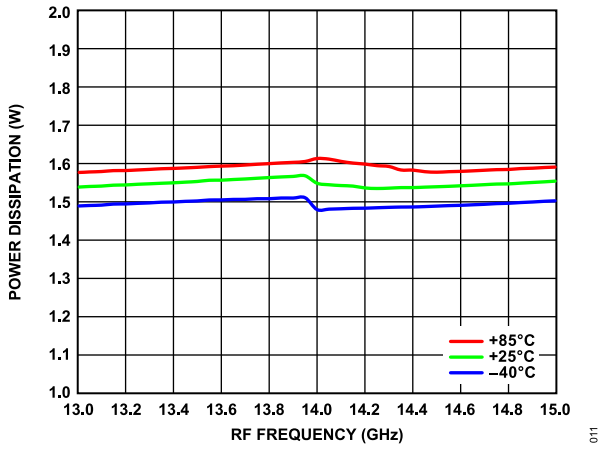

Figure 8. Power Dissipation vs. RF Frequency over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

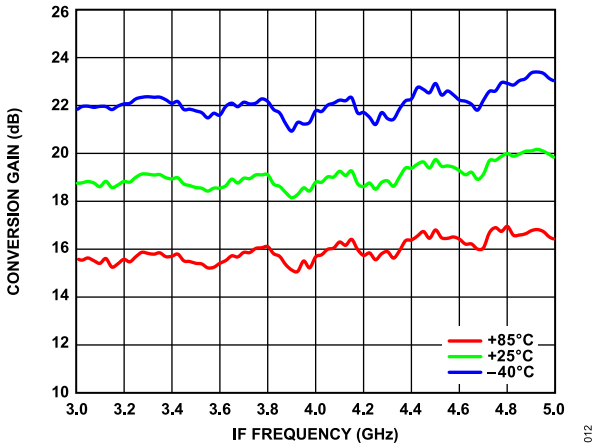

Figure 9. Conversion Gain vs. IF Frequency over Temperature

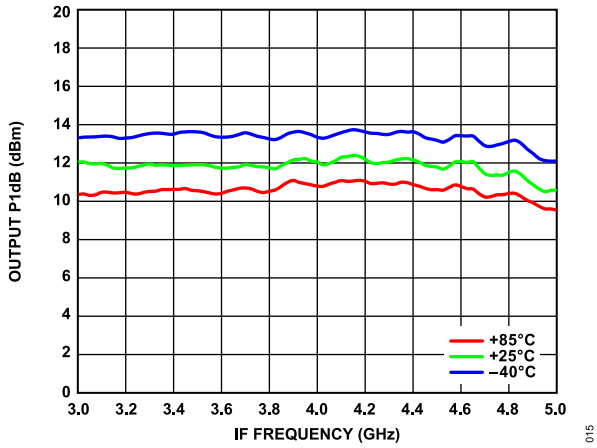

Figure 12. Output P1dB vs. IF Frequency over Temperature

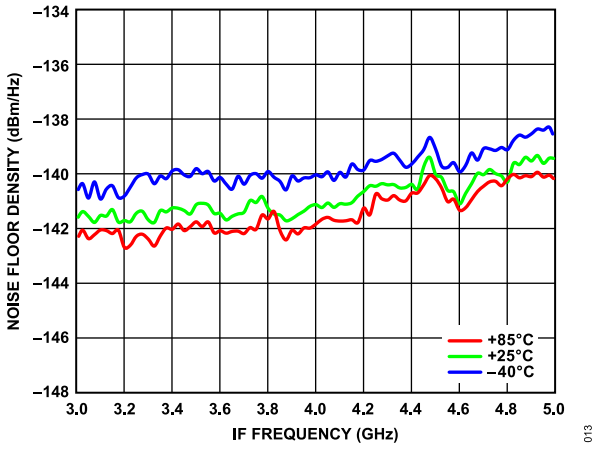

Figure 10. Noise Floor Density vs. IF Frequency over Temperature

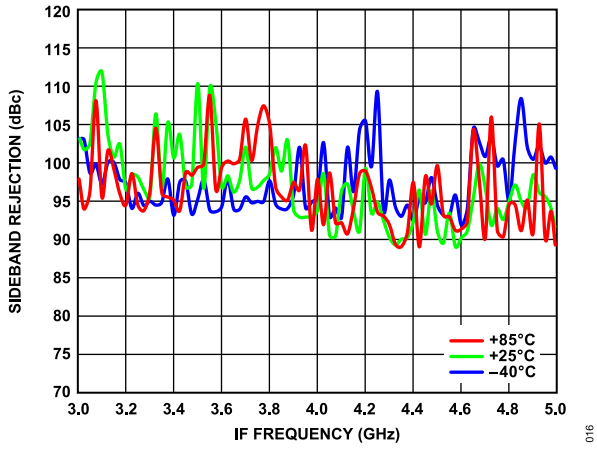

Figure 13. Sideband Rejection vs. IF Frequency over Temperature

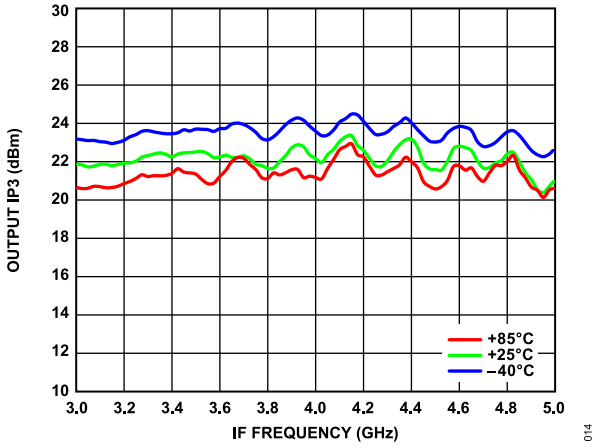

Figure 11. Output IP3 vs. IF Frequency over Temperature

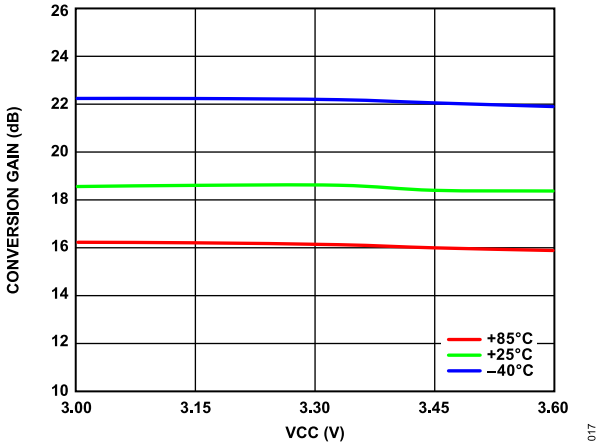

Figure 14. Conversion Gain vs. VCC over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

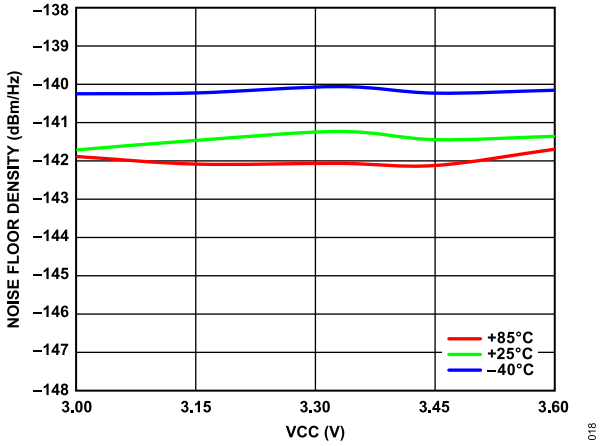

Figure 15. Noise Floor Density vs. VCC over Temperature

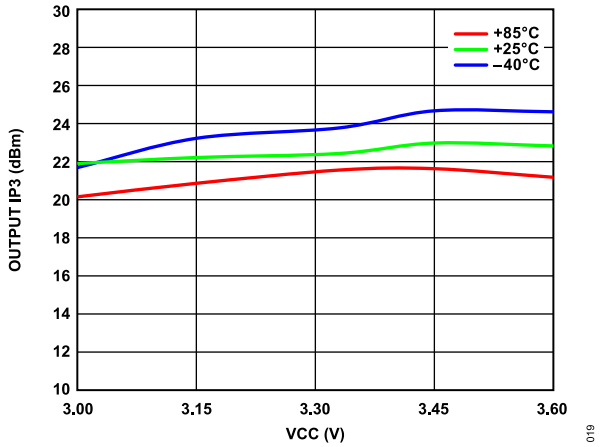

Figure 16. Output IP3 vs. VCC over Temperature

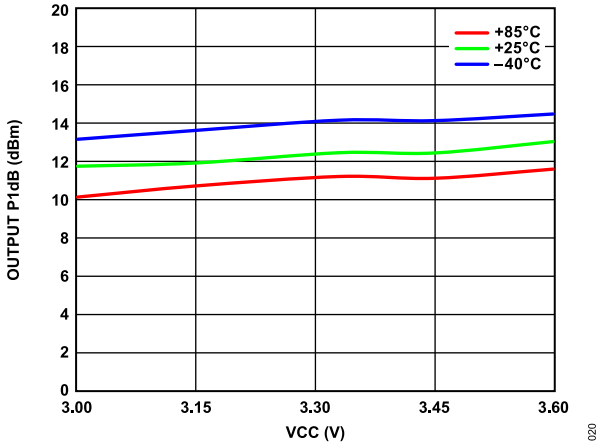

Figure 17. Output P1dB vs. VCC over Temperature

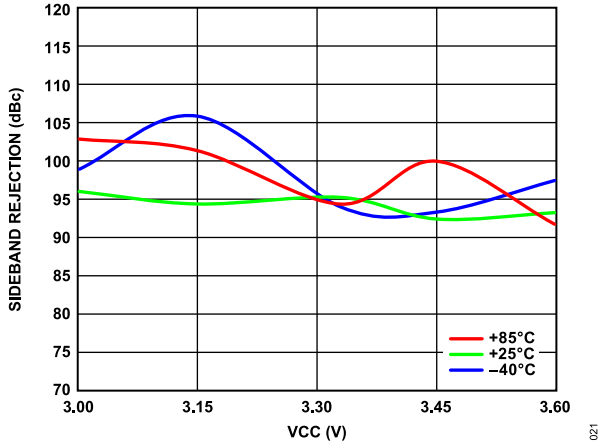

Figure 18. Sideband Rejection vs. VCC over Temperature

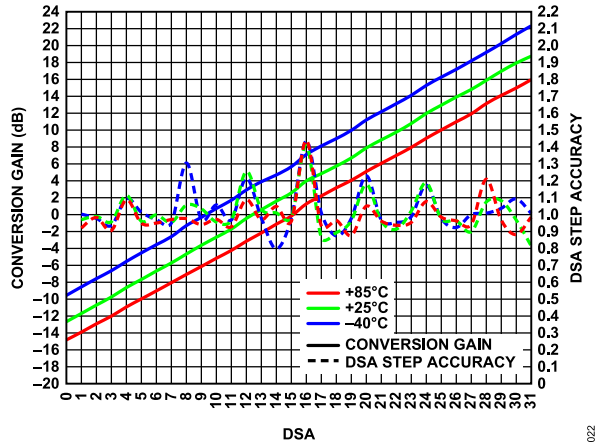

Figure 19. Conversion Gain and DSA Step Accuracy vs. DSA over Temperature

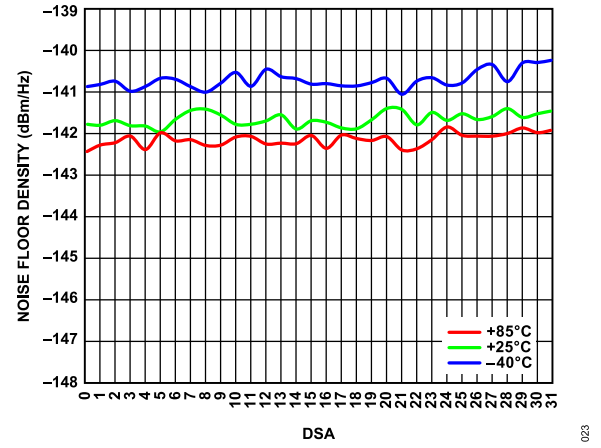

Figure 20. Noise Floor Density vs. DSA over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

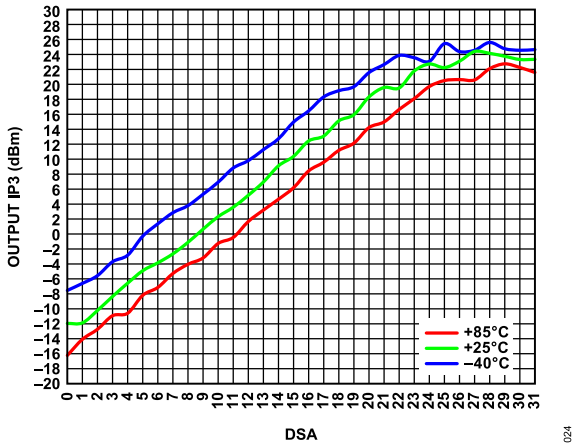

Figure 21. Output IP3 vs. DSA over Temperature

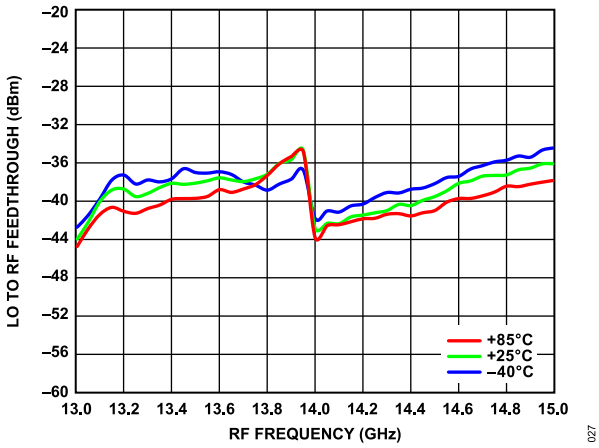

Figure 24. LO to RF Feedthrough vs. RF Frequency over Temperature

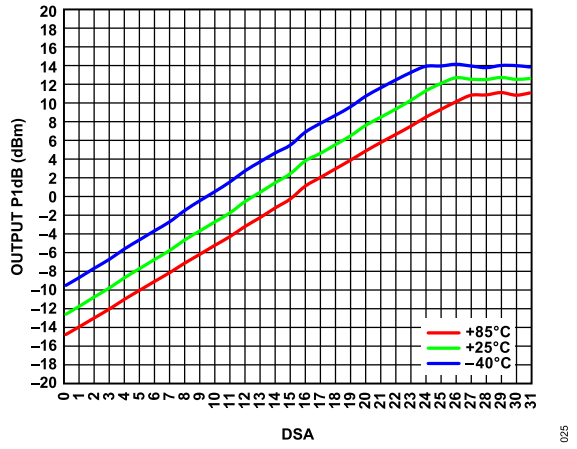

Figure 22. Output P1dB vs. DSA over Temperature

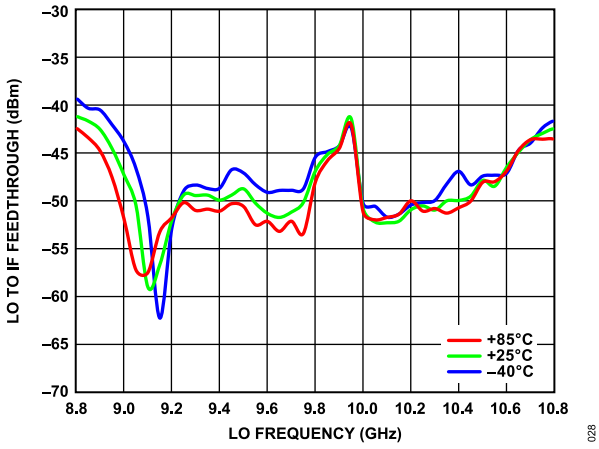

Figure 25. LO to IF Feedthrough vs. LO Frequency over Temperature

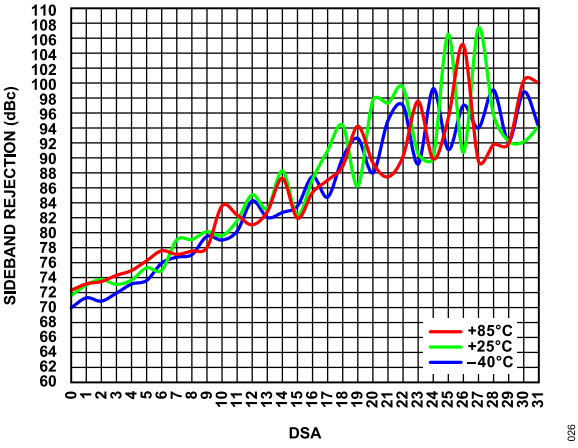

Figure 23. Sideband Rejection vs. DSA over Temperature

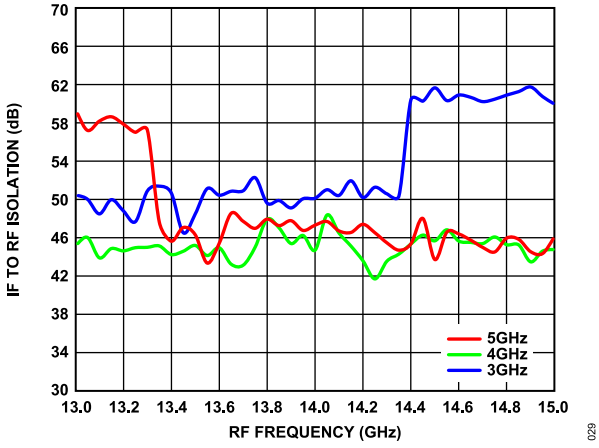

Figure 26. IF to RF Isolation vs. RF Frequency, IF = 3 GHz, 4 GHz, and 5 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

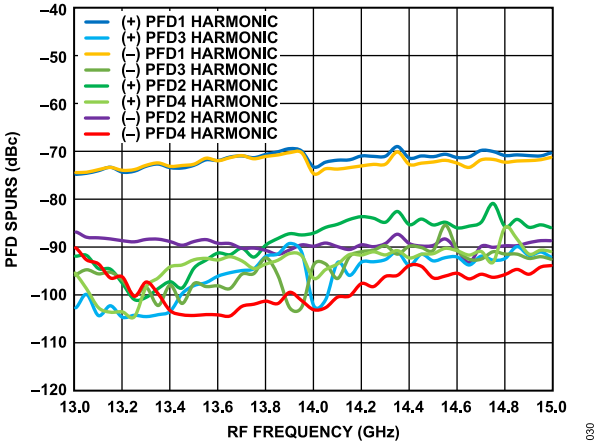

Figure 27. Phase Frequency Detector (PFD) Spurs vs. RF Frequency over Temperature

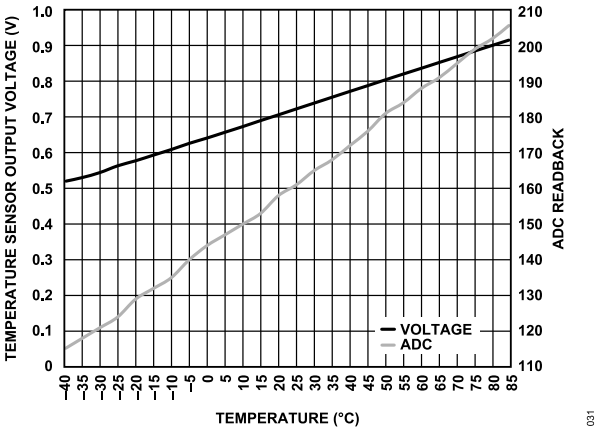

Figure 28. Temperature Sensor Output Voltage and ADC Readback vs. Temperature, LO Frequency = 10 GHz

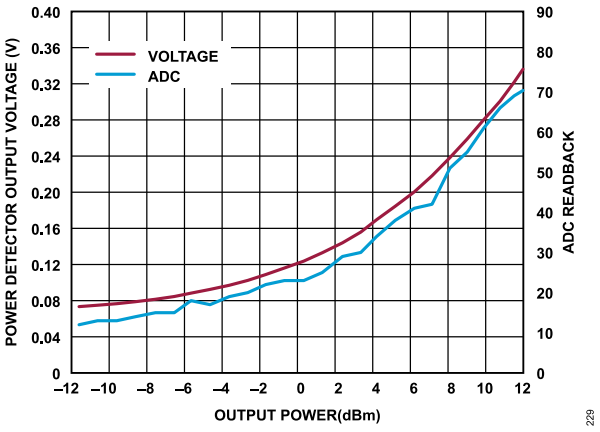

Figure 29. Power Detector Output Voltage and ADC Readback vs. Output Power, LO Frequency = 10 GHz

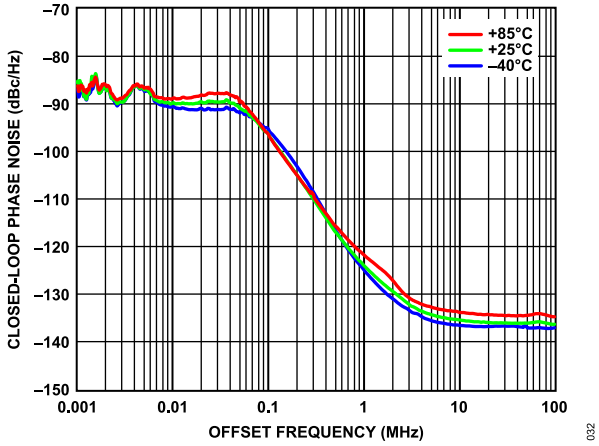

Figure 30. Closed-Loop Phase Noise vs. Offset Frequency over Temperature, LO = 10 GHz

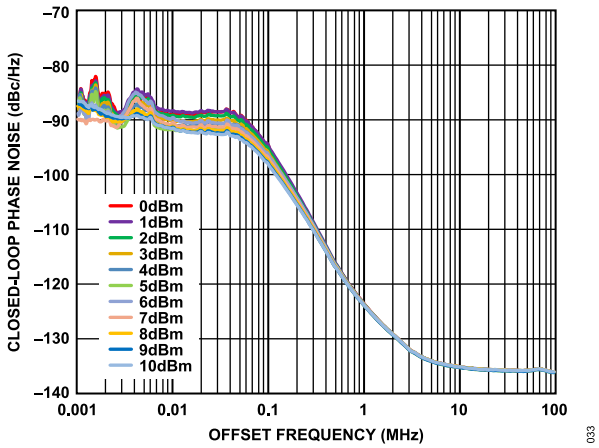

Figure 31. Closed-Loop Phase Noise vs. Offset Frequency over Reference Input Power

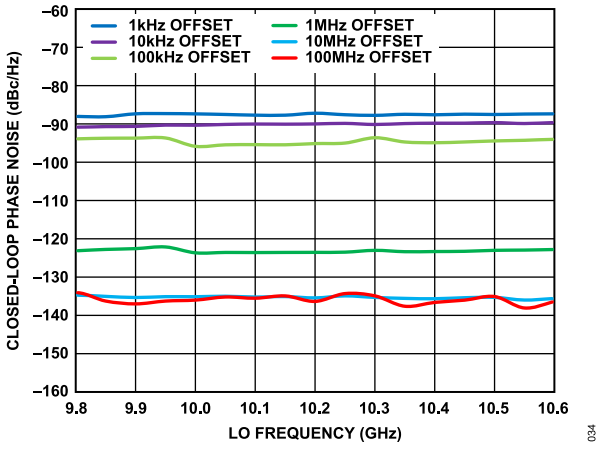

Figure 32. Closed-Loop Phase Noise vs. LO Frequency over Offset Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

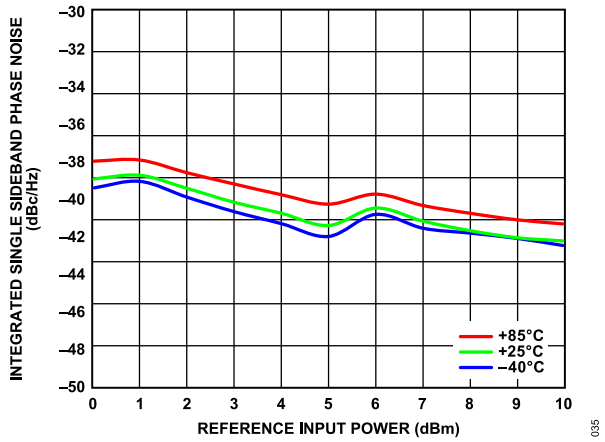

Figure 33. Integrated Single Sideband Phase Noise vs. Reference Input Power over Temperature, 1 kHz to 125 MHz

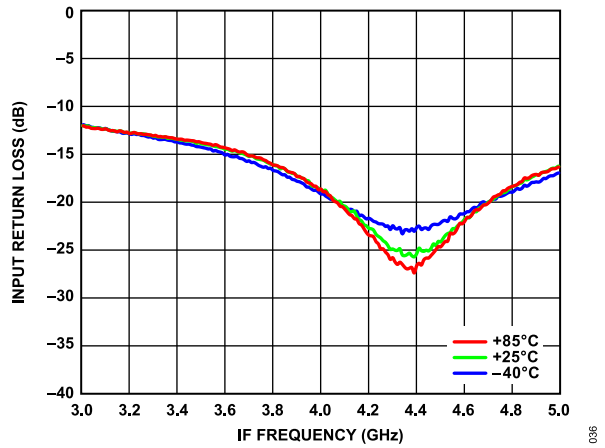

Figure 34. Input Return Loss vs. IF Frequency over Temperature

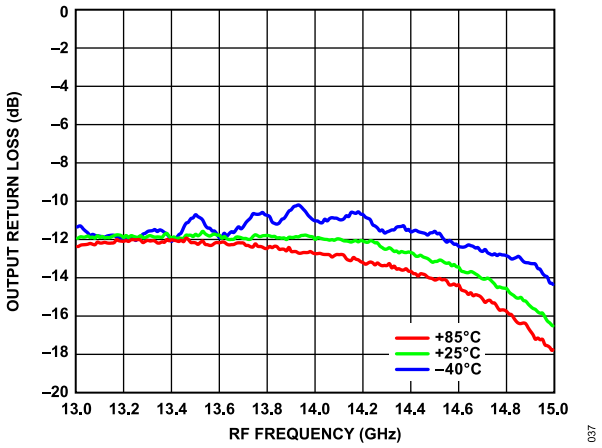

Figure 35. Output Return Loss vs. RF Frequency over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM ATTENUATION PERFORMANCE: DSA (REGISTER 0X300) = 0

T_A = 25°C, IF = 4 GHz, VCC = 3.3 V, clock reference input power = 3 dBm, and upper sideband selected, unless otherwise noted.

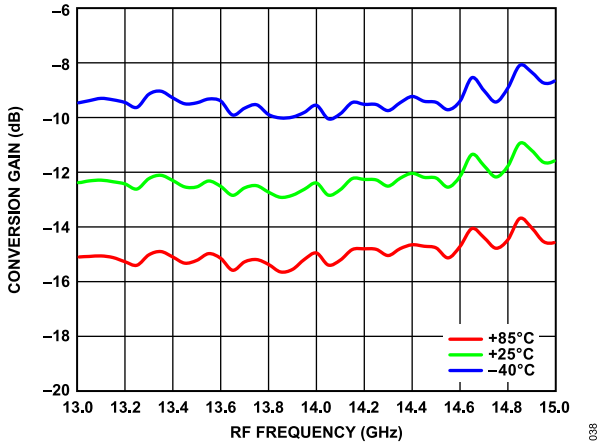

Figure 36. Conversion Gain vs. RF Frequency over Temperature

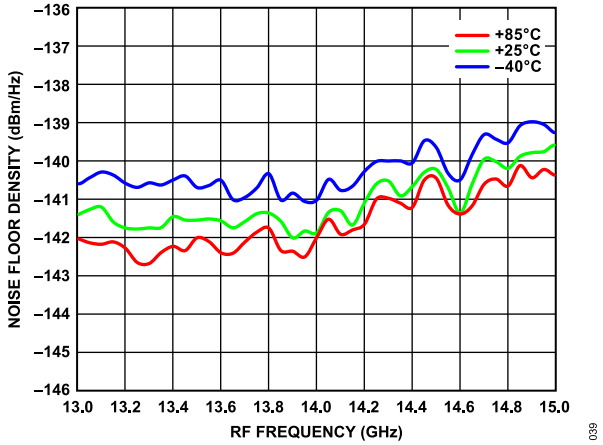

Figure 37. Noise Floor Density vs. RF Frequency over Temperature

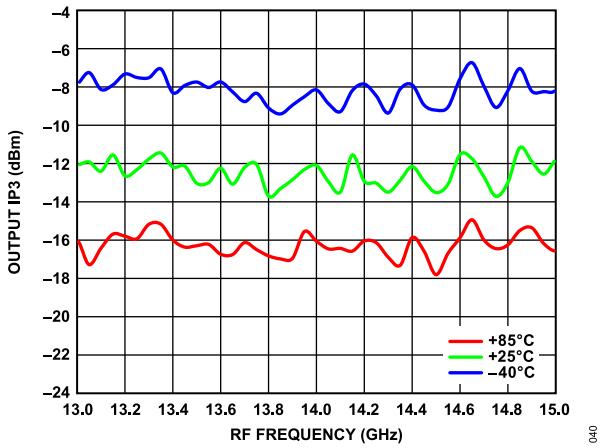

Figure 38. Output IP3 vs. RF Frequency over Temperature

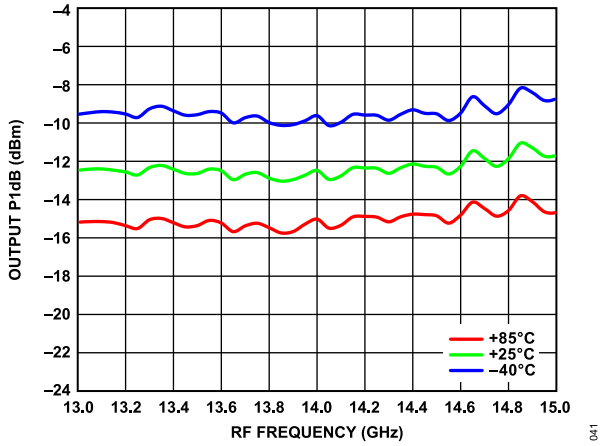

Figure 39. Output P1dB vs. RF Frequency over Temperature

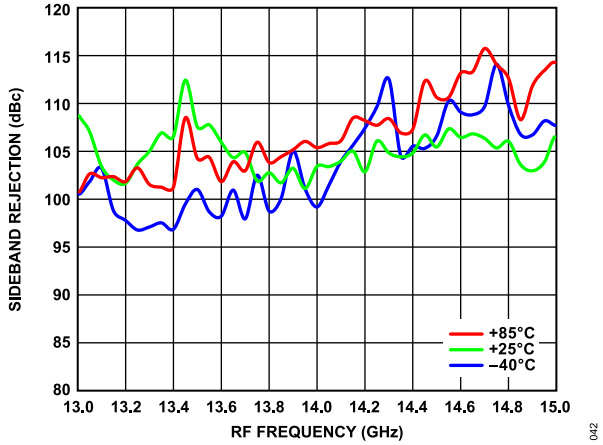

Figure 40. Sideband Rejection vs. RF Frequency over Temperature

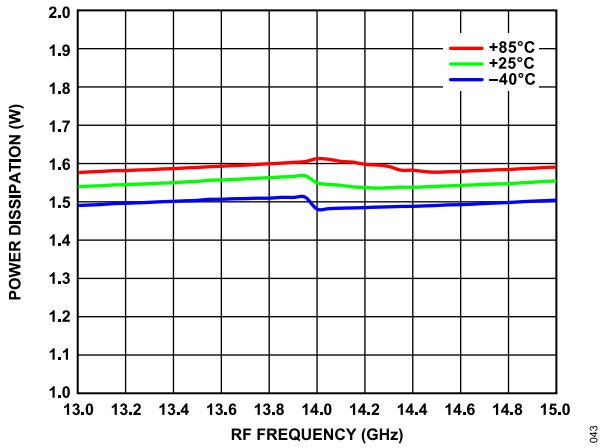

Figure 41. Power Dissipation vs. RF Frequency over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

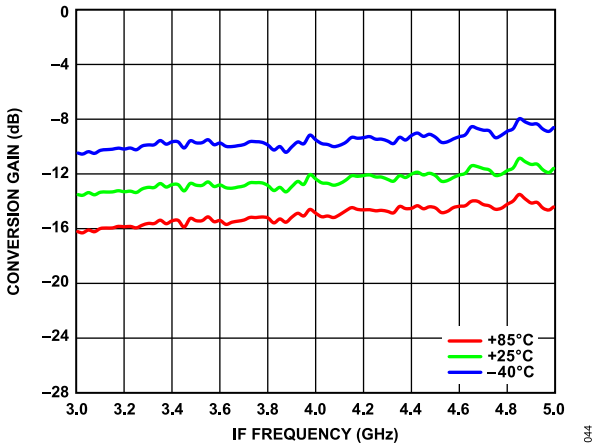

Figure 42. Conversion Gain vs. IF Frequency over Temperature

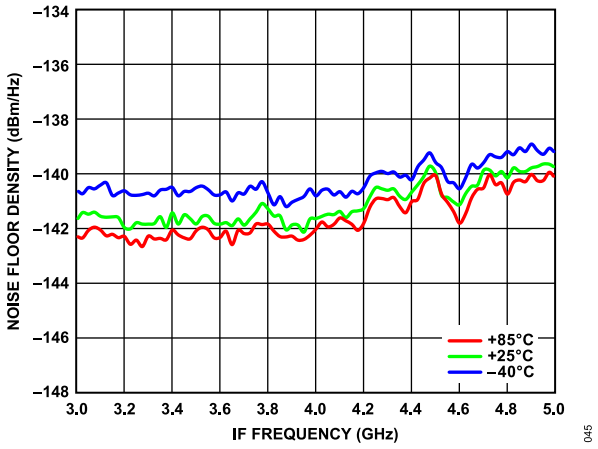

Figure 43. Noise Floor Density vs. IF Frequency over Temperature

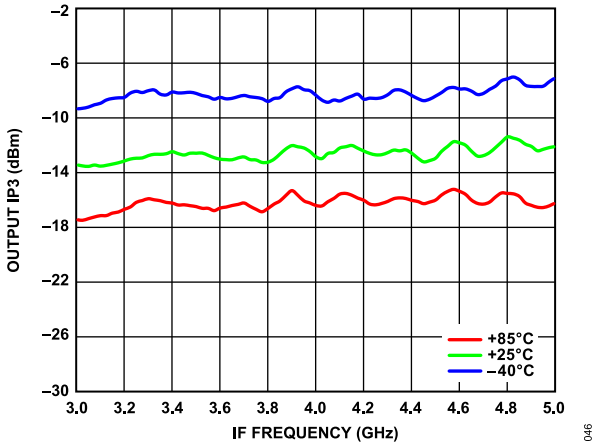

Figure 44. Output IP3 vs. IF Frequency over Temperature

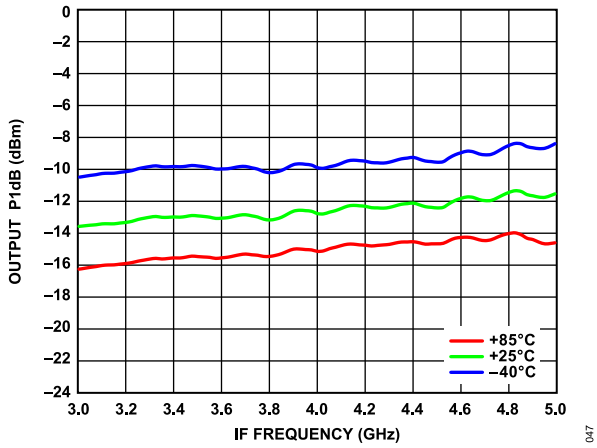

Figure 45. Output P1dB vs. IF Frequency over Temperature

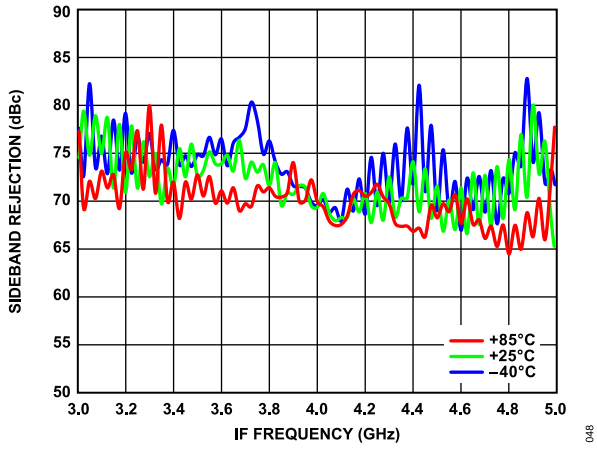

Figure 46. Sideband Rejection vs. IF Frequency over Temperature

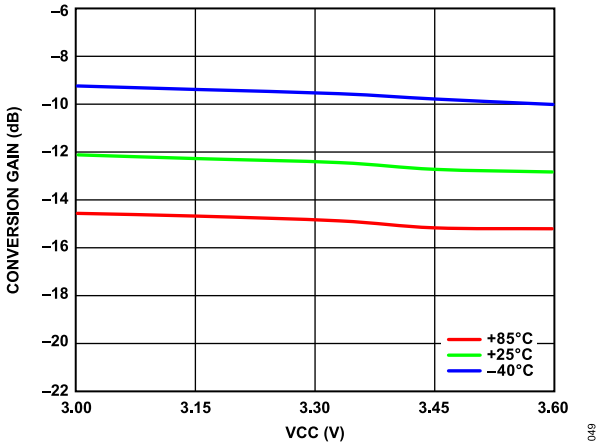

Figure 47. Conversion Gain vs. VCC Frequency over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

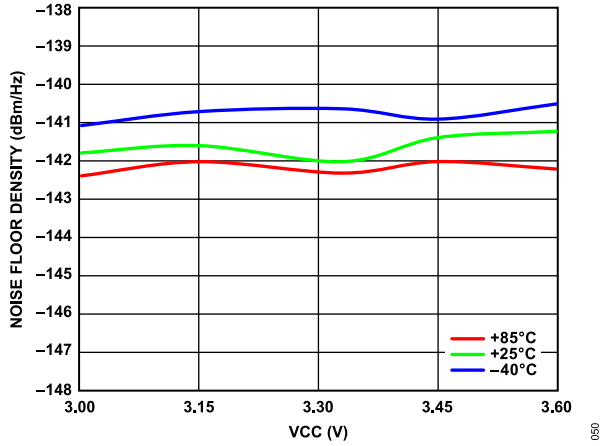

Figure 48. Noise Floor Density vs. VCC over Temperature

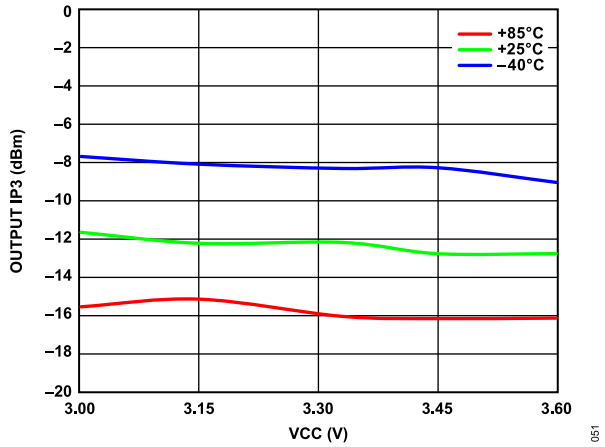

Figure 49. Output IP3 vs. VCC over Temperature

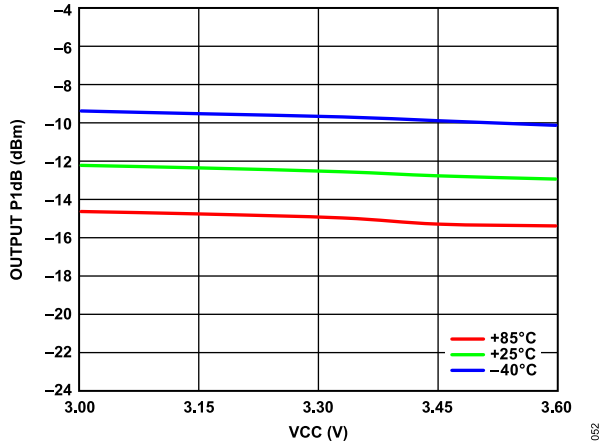

Figure 50. Output P1dB vs. VCC over Temperature

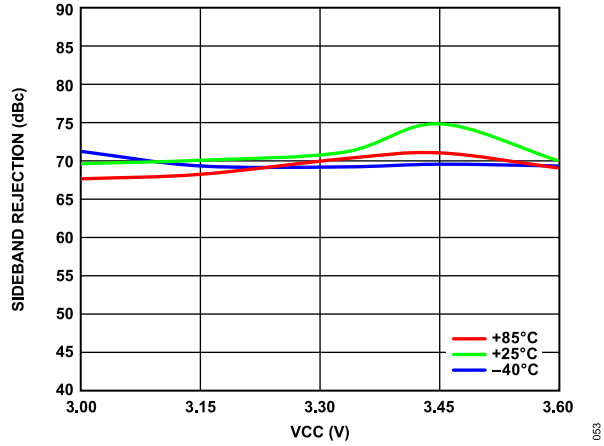

Figure 51. Sideband Rejection vs. VCC over Temperature

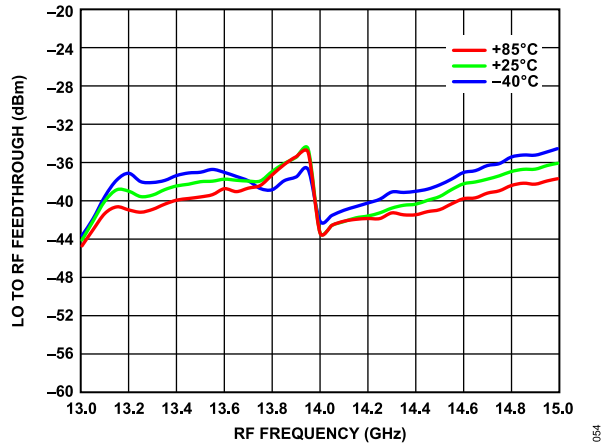

Figure 52. LO to RF Feedthrough vs. RF Frequency over Temperature

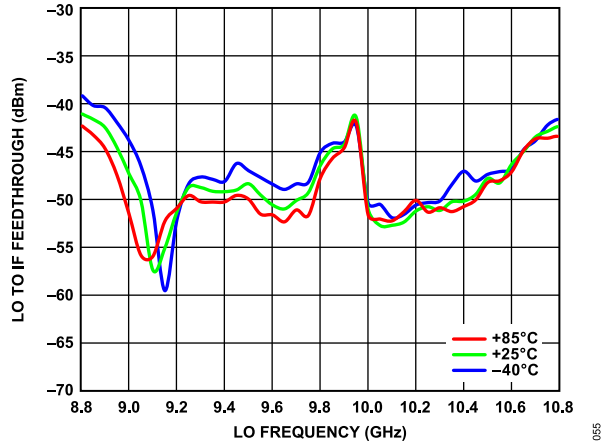

Figure 53. LO to IF Feedthrough vs. LO Frequency over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

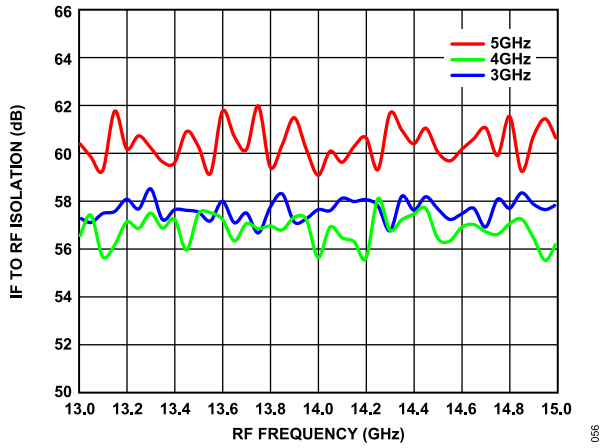

Figure 54. IF to RF Isolation vs. RF Frequency, IF = 3 GHz, 4 GHz, and 5 GHz

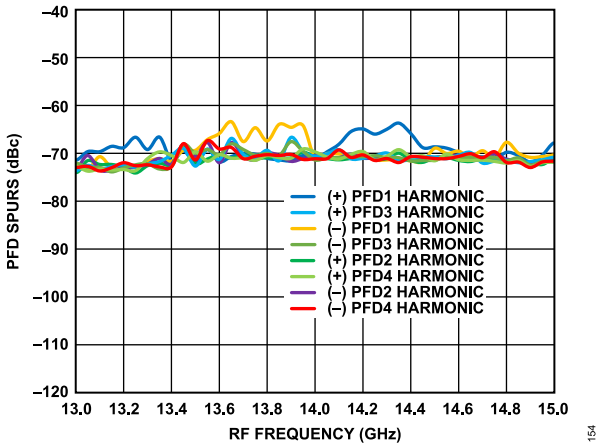

Figure 55. PFD Spurs vs. RF Frequency over Temperature, Measured from the RF Output Power Level

TYPICAL PERFORMANCE CHARACTERISTICS

SPURIOUS PERFORMANCE

T_A = 25°C, IF = 4 GHz, VCC = 3.3 V, minimum attenuation (DSA = 31), clock reference input power = 3 dBm, and upper sideband is selected. Mixer spurious products are measured in dBc from the RF output power level. Spur values are (M × IF) + (N × LO).

M × N Spurious Outputs, RF = 14 GHz, LO = 10 GHz

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	40	35	≥100	≥100	≥100
	1	77	0	94	≥100	≥100	≥100
	2	≥100	92	78	≥100	≥100	≥100
	3	54	≥100	≥100	≥100	≥100	≥100
	4	56	75	≥100	≥100	≥100	≥100
	5	34	≥100	≥100	≥100	≥100	≥100

M × N Spurious Outputs, RF = 14.25 GHz, LO = 10.25 GHz

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	40	35	98	≥100	≥100
	1	77	0	95	≥100	≥100	≥100
	2	≥100	96	81	≥100	≥100	≥100
	3	96	≥100	≥100	≥100	≥100	≥100
	4	92	≥100	≥100	≥100	≥100	≥100
	5	≥100	≥100	≥100	≥100	≥100	≥100

M × N Spurious Outputs, RF = 14.5 GHz, LO = 10.5 GHz

		N × LO					
		0	**1**	**2**	**3**	**4**	**5**
M × IF	**0**	N/A	38	34	≥100	≥100	≥100
	1	77	0	≥100	≥100	≥100	≥100
	2	≥100	99	86	≥100	≥100	≥100
	3	96	≥100	≥100	≥100	≥100	≥100
	4	87	≥100	≥100	≥100	≥100	≥100
	5	≥100	≥100	≥100	≥100	≥100	≥100

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REFERENCE INPUT STAGE

The reference input stage is shown in Figure 56 and can be driven by an external singled-ended 25 MHz source. Ensure the external dc block is used at the reference input.

REFERENCE DOUBLER, R COUNTER, AND REFERENCE DIVIDE BY 2

There is an internal reference multiply by 2 block (×2 doubler, see Figure 56) that generates higher phase frequency detector frequencies (f_{PFD}). Use the DOUBLER_EN bit (Register 0x20E, Bit 3) to enable the reference doubler.

There are two frequency dividers: a 5-bit R divider counter (1 to 32 allowed) and a divide by 2 block. These dividers divide the input reference frequency (f_{REF}) down to produce a lower f_{PFD}. Set the R counter by using the R_DIV bit in Register 0x20C, Bits[4:0].

The reference divide by 2 block is enabled by using the RDIV2_EN in Register 0x20E, Bit 0.

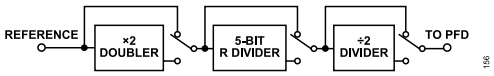

Figure 56. Reference Input Path Block Diagram

INT MODE AND N COUNTER

The ADMV4630 synthesizer operates in INT mode.

The N counter allows a division ratio in the phase-locked loop (PLL) feedback path from the VCO. The division ratio is determined by the INT bit value. The applicable registers for setting the INT bit values are Register 0x200 and Register 0x201.

The INT value, in conjunction with the reference path, can generate VCO frequencies spaced by the resolution of the f_{PFD}.

The f_{PFD} is calculated from the reference frequency (f_{REF}) and the reference path configuration parameters with the following equation:

$$f_{PFD} = f_{REF} \times \frac{1 + D}{R \times (1 + T)} \quad (1)$$

where:
D is the reference doubler bit (0 or 1).
R is the reference divide ratio of the binary, 5-bit programmable counter (1 to 31).
T is the reference divide by 2 bit (0 or 1).

The VCO frequency (f_{VCO}) is calculated with the following equation:

$$f_{VCO} = \frac{f_{LO}}{2} = f_{PFD} \times N \quad (2)$$

where:
f_{LO} is the frequency of the LO driving the mixer.
N is the desired value of INT, where INT is the 16-bit integer value (0 to 65,535).

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP (CP)

The PFD takes inputs from the R counter and N counter to produce an output that is proportional to the phase and frequency differences between the two counters. This proportional information is output to a CP circuit that generates current to drive an external loop filter, which is then used to appropriately increase or decrease the VTUNE tuning voltage.

Figure 57 shows a simplified schematic of the PFD and CP. U1 and U2 are two D type flip flops and U3 is an AGND gate. Note that the PFD includes a fixed delay element, which is used to ensure that there is no dead zone in the PFD transfer function for consistent reference spur levels.

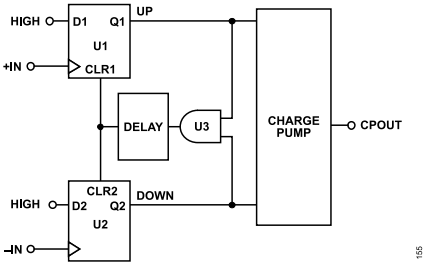

Figure 57. PFD and CP Simplified Schematic

LOOP FILTER AND CHARGE PUMP CURRENT

Defining a loop filter for a PLL depends on several dynamics, such as the PFD frequency, the N counter value, the tuning sensitivity characteristics (k_{VCO}) of the VCO, and the selected CP current. A lower f_{PFD} allows the PLL to operate in INT mode, which can eliminate integer boundary spurs at the expense of higher in band phase noise performance. Given the trade-offs, care must be taken with frequency planning and f_{PFD} selection to ensure the appropriate in band phase noise performance is met with acceptable spur levels for the end application.

The loop filter that is implemented in the EVAL-ADMV4630Z evaluation board is shown in Figure 58. The CP current (I_{CP}) is set by Register 0x22E. The default register value is recommended.

For additional guidance with loop filter simulations on the ADMV4630, contact Analog Devices, Inc., for technical support.

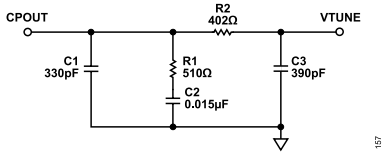

Figure 58. Recommended Loop Filter Schematic

ON-CHIP MUXOUT PIN

The MUXOUT pin allows access to various internal signals and provides a digital lock detect function. A diagram of the MUXOUT

THEORY OF OPERATION

pin output is shown in Figure 59. The state of the MUXOUT pin is determined from the MUX_SEL value in Register 0x24E.

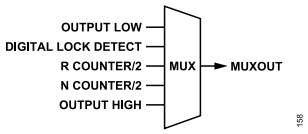

Figure 59. MUXOUT Pin Diagram

ANALOG MUX BLOCK, AGPIO PIN, AND ADC

The on-chip AGPIO pin can be used either as an external analog input or output of the device analog multiplexer (mux) signal. When used as an input, the AGPIO signal is transferred to the on-chip analog multiplexer. The analog mux selects between the temperature sensor, the power detector, and the AGPIO signal. There is an on-chip ADC sampling the signals from analog mux.

To enable the ADC to sample the analog mux signal, take the following steps:

1. Make sure the reference input is fed to the ADMV4630.
2. Set Register 0x301, Bits[2:0] to 0, 110, or 111 to select between the temperature sensor, the power detector, or the AGPIO signal as the analog mux output. If the AGPIO signal is selected to sample the ADC, set Register 0x301, Bit 3 to 1. Setting this bit sets AGPIO as the external signal input.
3. Set Register 0x302, Bits[3:0] to 0x00 to disable the ADC log scale and reset ADC.
4. Set Register 0x302 Bits[1:0] to 0x03 to enable and start ADC sampling.
5. Wait for 1 ms.
6. Set Register 0x302, Bit 1 to 0.
7. Read the ADC value from Register 0x304.
8. Set Register 0x302, Bits[1:0] to 0x00 to turn off the ADC.

The default ADC input voltage range is 0 V to 1.1 V. If a higher input range is required, set Register 0x302, Bit 2 to 1 to halve the input voltage before sampling. The voltage range is then 0 V to 2.2 V.

Enable or disable the ADC output log scale by setting Register 0x302, Bit 3 to 1 or 0.

The AGPIO pin can also be used as an output to transfer the analog mux signal to the AGPIO pin. Take the following steps to set the AGPIO pin as the output:

1. Set Register 0x301, Bit 3 to 0 to set the AGPIO pin as the output.
2. Set the Register 0x301, Bits[2:0] value to 0 or 110 to set either the temperature sensor or the power detector as the analog mux output.
3. Set Register 0x302, Bit 0 to 0 to turn off the ADC.

GPIOX PINS

There are three GPIOx pins, where x is 1, 2, or 3, for input/output control. Use Register 0x307 to set the GPIO settings and see the Register Details section for more information.

DIGITAL LOCK DETECT AND MUTE_IF_UNLOCK BIT

The digital lock detect function that is output on the MUXOUT pin has two adjustable settings in Register 0x214. The first setting, LD_BIAS, adjusts an internal precision window and the second setting, LD_COUNT, adjusts the consecutive cycle count to declare the PLL lock. It is recommended to keep the default register value for these adjustable settings. The lock detect status can also be obtained from Register 0x24D, Bit 0.

The MUTE_IF_UNLOCK bit (Register 0x103, Bit 0) provides the function to mute the output if the PLL is unlocked. Set this bit to 1 to enable the mute function.

SIGNAL CHAIN BIAS, MASK, TX_MUTE PIN, AND TXON PIN

TXON and TX_MUTE are two on-chip pins. These pins are signal masks commanding the chip to block or enable certain stages. These two pins can be pulled to high (3.3 V) or low (ground). Use Register 0x101, mute mask control, and Register 0x102, on mask control, to determine which stages in the signal path the two pins mask.

Register 0x100 (bias control), Register 0x101 (mute mask control), and Register 0x102 (on mask control) control the on and off status for each stage in the signal path.

Register 0x100 is a bias control register. Set each bit in this register to 1 or 0 to enable or disable the corresponding stage bias.

Register 0x101 is a mute mask control register. Set each bit in this register to 1 to allow the TX_MUTE pin to mask the corresponding stage.

For example, when the LO amplifier mute mask control bit is on (Bit 1 in Register 0x101 set to 1) and the TX_MUTE pin on the chip is pulled to high, the LO amplifier is blocked.

Table 5 is the truth table detailing how the TX_MUTE pin and mute mask control register work together to block signal stages. Note that the MUTE_IF_UNLOCKED bit, (Register 0x103, Bit 0) has the same muting effect as the TX_MUTE pin when enabled.

Register 0x102 is an on mask control register. Set each bit in this register to 1 to allow the TXON pin to mask the corresponding stage. Note that for the TXON pin to work, the corresponding stage bias control in Register 0x100 must be on and the TX_MUTE pin and mute mask control must be disabled.

For example, when the LO amplifier on mask control bit is on by setting Register 0x102, Bit 1 to 1, and the on-chip TXON pin is pulled low, the LO amplifier is blocked.

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Table 6 is the truth table detailing how the TXON pin and on mask control register work together to block the signal stages.

SPI CONFIGURATION

The ADMV4630 SPI configures the device for specific functions or operations via the 4-pin SPI port. This interface provides users with added flexibility and customization. The SPI consists of the following four control lines: SCLK, SDI, SDO, and $\overline{CS}$. The ADMV4630 protocol consists of a write or read bit, followed by 15 register address bits and 8 data bits. The address field and data field are organized LSB first and end with the MSB.

Set the MSB to 0 for a write operation and set the MSB to 1 for a read operation.

The write cycle sampling must be performed on the rising edge of the SCLK control line. The 24 bits of the serial write address and data are shifted in on the SDI control line. The ADMV4630 input logic level for the write cycle supports a 3.3 V interface.

For a read cycle, the read/write (R/W) bit and the 15 bits of address shift in on the rising edge of the SCLK pin on the SDI pin. Then, eight bits of serial read data shift out on the SDO pin LSB first on the falling edge of SCLK. The output logic level for a read cycle is 3.3 V. The output drivers of the SDO are enabled after the last rising edge of SCLK of the instruction cycle and remain active until the end of the read cycle. When the $\overline{CS}$ pin is deasserted in a read operation, SDO returns to high impedance until the next read transaction. The $\overline{CS}$ pin is active low and must be deasserted at the end of the write or read sequence.

An active low input on the $\overline{CS}$ pin starts and gates a communication cycle. The $\overline{CS}$ pin allows multiple devices, not just the ADMV4630, to be used on the same serial communications lines. The SDO pin goes to a high impedance state when the input on the $\overline{CS}$ pin is high. During the communication cycle, the $\overline{CS}$ pin must stay low.

The SPI communications protocol follows the Analog Devices SPI standard. For more information, see the ADI-SPI Serial Control Interface Standard (Rev 1.0) guide.

VCO AUTOCALIBRATION AND AUTOMATIC LEVEL CONTROL

The multicore VCO uses an internal autocalibration and automatic level control (ALC) routine that optimizes the VCO settings for a user defined frequency and locks the PLL after the lower portion of the N counter integer value (Register 0x200) is programmed.

DOUBLE BUFFERED REGISTERS

Register 0x20C, Register 0x20E, and Register 0x201 are double buffered registers that take effect only after a write to the lower portion of the integer value (Register 0x200). Register 0x200 applies any changes to these double buffered registers and initiates the autocalibration routine.

The following steps describe the recommended programming sequence (users set the values) for double buffered registers:

1. Program Register 0x20C.
2. Program the RDIV2_EN bit (Register 0x20E, Bit 0).
3. Program the DOUBLER_EN bit (Register 0x20E, Bit 3).
4. Program Register 0x201.
5. Program Register 0x200.

INITIALIZATION REGISTERS

Write the specified code to the following registers to initialize the device with maximum gain and LO at 10 GHz:

1. Register 0x000 = 0x99
2. Register 0x000 = 0x18
3. Register 0x103 = 0x00
4. Register 0x22B = 0x0B
5. Register 0x22F = 0x27
6. Register 0x30A = 0x00
7. Register 0x309 = 0x88
8. Register 0x30D = 0x09
9. Register 0x30E = 0x09
10. Register 0x300 = 0x1F

THEORY OF OPERATION

Table 5. Signal Stage Status Truth Table Using the TX_MUTE Pin and Mute Mask Control

TX_MUTE Pin || MUTE_IF_UNLOCKED[1]	Mute Mask Control Register 0x101[1]	TXON Pin[1]	On Mask Control Register 0x102[1]	Bias Enable Control Register 0x100[1]	Result (1 is On, 0 is Off)[1]
1	1	0 or 1	0 or 1	0 or 1	0
1	0	Controlled by TXON pin			
0	1	Controlled by TXON pin			

[1] The 0 and 1 settings apply to all user specified bits in the listed register.

Table 6. Signal Stage Status Truth Table Using the TXON Pin and On Mask Control

TX_MUTE Pin || MUTE_IF_UNLOCKED Bit (Register 0x103)[1]	Mute Mask Control (Register 0x101)[1]	TXON Pin[1]	On Mask Control (Register 0x102)[1]	Bias Enable Control (Register 0x100)[1]	Result (1 is On, 0 is Off)[1]
0 or 1	0	0 or 1	0	0	0
0 or 1	0	0 or 1	0	1	1
0 or 1	0	0	1	0 or 1	0
0 or 1	0	1	1	0	0
0 or 1	0	1	1	1	1
0	0 or 1	0 or 1	0	0	0
0	0 or 1	0 or 1	0	1	1
0	0 or 1	0	1	0 or 1	0
0	0 or 1	1	1	0	0
0	0 or 1	1	1	1	1

[1] The 0 and 1 settings apply to all user specified bits in the listed register.

REGISTER SUMMARY

Table 7. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x000	SPI_ CONFIG_1	[7:0]	SOFT-RESET_	LSB_ FIRST_	ENDIAN_	SDO-ACTIVE_	SDOACTIVE	ENDIAN	LSB_ FIRST	SOFT-RESET	0x00	R/W
0x004	PRODUCT_ ID_L	[7:0]	PRODUCT_ID_L								0x30	R
0x005	PRODUCT_ ID_H	[7:0]	PRODUCT_ID_H								0x46	R
0x100	BIAS_ CONTROL	[7:0]	RF_ CONTROLLER_ BIAS_ CONTROL	SYNTH_ BIAS_ CONTROL	DET_ BIAS_ CONTROL	TXOUTPUT _SWITCH	AMPRF-DRIVER_ BIAS_ CONTROL	AMPRFPRE-DRIVER_ BIAS_ CONTROL	AMPLO_ BIAS_ CONTROL	AMPIF_ BIAS_ CONTROL	0xDF	R/W
0x101	MUTE_ MASK_ CONTROL	[7:0]	RF_ CONTROLLER_ MUTE_ MASK_ CONTROL	SYNTH_ MUTE_ MASK_ CONTROL	DET_ MUTE_ MASK_ CONTROL	SWITCHRF _MUTE_ MASK_ CONTROL	AMPRF-DRIVER_ MUTE_ MASK_ CONTROL	AMPRFPRE-DRIVER_ MUTE_MASK_ CONTROL	AMPLO_ MUTE_ MASK_ CONTROL	AMPIF_ MUTE_ MASK_ CONTROL	0xBF	R/W
0x102	ON_MASK_ CONTROL	[7:0]	RF_ CONTROLLER_ ON_MASK_ CONTROL	SYNTH_ ON_ MASK_ CONTROL	DET_ON_ MASK_ CONTROL	SWITCHRF _ON_MASK _CONTROL	AMPRF-DRIVER_ ON_MASK_ CONTROL	AMPRFPRE-DRIVER_ ON_MASK_ CONTROL	AMPLO_ ON_MASK_ CONTROL	AMPIF_ ON_ MASK_ CONTROL	0xFF	R/W
0x103	MUTE_ UNLOCK	[7:0]	RESERVED							MUTE_ IF_ UNLOCKED	0x01	R/W
0x200	INT_L	[7:0]	INT[7:0]								0x90	R/W
0x201	INT_H	[7:0]	INT[15:8]								0x01	R/W
0x20B	SYNTH	[7:0]	RESERVED						PRE_SEL	EN_FBDIV	0x01	R/W
0x20C	R_DIV	[7:0]	RESERVED			R_DIV					0x01	R/W
0x20E	REFERENCE	[7:0]	RESERVED				DOUBLER_ EN	RESERVED		RDIV2_EN	0x04	R/W
0x214	LOCK_ DETECT_ CONFIG	[7:0]	LD_BIAS		LD_COUNT			RESERVED			0x48	R/W
0x218	SYNTH_ LOCK_ TIMEOUT	[7:0]	RESERVED			SYNTH_LOCK_TIMEOUT					0x1F	R/W
0x21C	VCO_ TIMEOUT_L	[7:0]	VCO_TIMEOUT[7:0]								0x19	R/W
0x21D	VCO_ TIMEOUT_H	[7:0]	RESERVED						VCO_TIMEOUT[9:8]		0x00	R/W
0x21E	VCO_ BAND_DIV	[7:0]	VCO_BAND_DIV								0x10	R/W
0x22B	MULTI_ FUNC_ SYNTH_ CTRL_022B	[7:0]	RESERVED						RF_PBS		0x09	R/W
0x22E	CP_CURR	[7:0]	RESERVED				CP_CURRENT				0x0E	R/W
0x22F	BICP	[7:0]	BICP								0x08	R/W
0x24D	LOCK_ DETECT	[7:0]	RESERVED							LOCK_ DETECT	0x00	R
0x24E	MUXOUT	[7:0]	MUX_SEL								0x00	R/W

REGISTER SUMMARY

Table 7. Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x300	DSA_ CONTROL	[7:0]	RESERVED			SEL_DSA_ATTEN					0x00	R/W
0x301	AGPIO_ CONTROL	[7:0]	RESERVED				SEL_AGPIO	SEL_AMUX			0x00	R/W
0x302	ADC_ CONTROL	[7:0]	SEL_ADC_CLKDIV				SEL_ADC_ LOG_SCALE	SEL_ADCHALF	ADC_ START	EN_ADC	0xCA	R/W
0x303	ADC_ STATUS	[7:0]	RESERVED					ADC_ LATCHDATA	ADC_ BUSY	ADC_EOC	0x01	R
0x304	ADC_DATA	[7:0]	ADC_DATA								0xEF	R
0x305	GPIO_ WRITEVALS	[7:0]	RESERVED				GPIO_WRITEVALS			RESERVED	0x00	R/W
0x306	GPIO_ READVALS	[7:0]	RESERVED				GPIO_READVALS			RESERVED	0x0E	R
0x307	GPIO_ CONTROL	[7:0]	RESERVED	EN_GPIO_OUT			SEL_GPIO_LEVELS			RESERVED	0x00	R/W
0x308	RFBIAS_ CONTROL1	[7:0]	RESERVED				SEL_BIAS_AMPIF				0x08	R/W
0x309	RFBIAS_ CONTROL2	[7:0]	SEL_BIAS_AMPRFDRIVER				SEL_BIAS_AMPRFPREDRIVER				0x88	R/W
0x30A	RFBIAS_ CONTROL3	[7:0]	SEL_BIAS_AMPLO2				SEL_BIAS_AMPLO1				0x88	R/W
0x30C	DETECTOR_ CONTROL	[7:0]	RESERVED			SEL_DET_TRIM					0x00	R/W
0x30D	MIXER_ CONTROL1	[7:0]	RESERVED			SEL_MIXLOCM_COARSE_P					0x08	R/W
0x30E	MIXER_ CONTROL2	[7:0]	RESERVED			SEL_MIXLOCM_COARSE_N					0x08	R/W

REGISTER DETAILS

SPI CONFIGURATION REGISTER

Address: 0x000, Reset: 0x00, Name: SPI_CONFIG_1

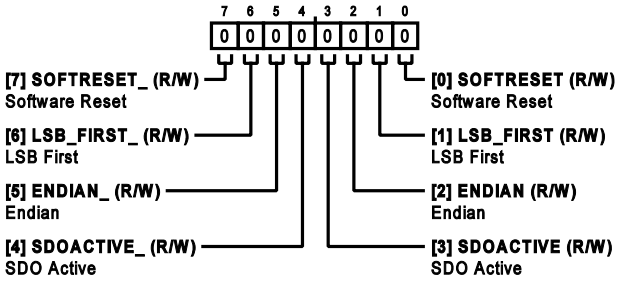
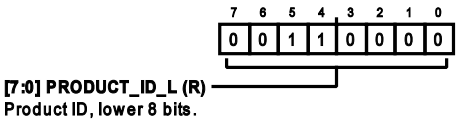


Table 8. Bit Descriptions for SPI_CONFIG_1

Bits	Bit Name	Description	Reset	Access
7	SOFTRESET_	Software Reset. 1: reset asserted. 0: reset not asserted.	0x0	R/W
6	LSB_FIRST_	LSB First. 0: LSB first. 1: MSB first.	0x0	R/W
5	ENDIAN_	Endian. 0: little endian. 1: big endian.	0x0	R/W
4	SDOACTIVE_	SDO Active. 1: SDO active. 0: SDO inactive.	0x0	R/W
3	SDOACTIVE	SDO Active. 0: SDO inactive. 1: SDO active.	0x0	R/W
2	ENDIAN	Endian. 0: little endian. 1: big endian.	0x0	R/W
1	LSB_FIRST	LSB First. 0: LSB first. 1: MSB first.	0x0	R/W
0	SOFTRESET	Software Reset. 0: reset not asserted. 1: reset asserted.	0x0	R/W

Product ID Register (Lower Eight Bits)

Address: 0x004, Reset: 0x30, Name: PRODUCT_ID_L



REGISTER DETAILS

Table 9. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID_L	Product ID, lower 8 bits.	0x30	R

Product ID Register (Upper Eight Bits)

Address: 0x005, Reset: 0x46, Name: PRODUCT_ID_H

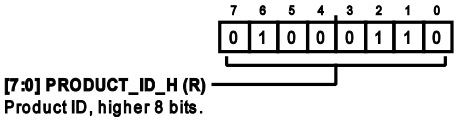


Table 10. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID_H	Product ID, higher 8 bits.	0x46	R

Bias Control Register

Address: 0x100, Reset: 0xDF, Name: BIAS_CONTROL

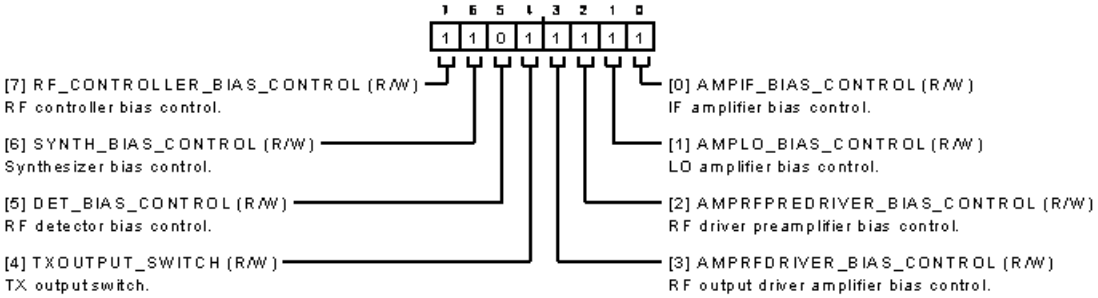


Table 11. Bit Descriptions for BIAS_CONTROL

Bits	Bit Name	Description	Reset	Access
7	RF_CONTROLLER_BIAS_CONTROL	RF controller bias control. 0: disables. 1: enables.	0x1	R/W
6	SYNTH_BIAS_CONTROL	Synthesizer bias control. 0: disables. 1: enables.	0x1	R/W
5	DET_BIAS_CONTROL	RF detector bias control. 0: disables. 1: enables.	0x0	R/W
4	TXOUTPUT_SWITCH	TX output switch. 0: disables. 1: enables.	0x1	R/W
3	AMPRFDRIVER_BIAS_CONTROL	RF output driver amplifier bias control. 0: disables. 1: enables.	0x1	R/W
2	AMPRFPREDRIVER_BIAS_CONTROL	RF driver preamplifier bias control.	0x1	R/W

REGISTER DETAILS

Table 11. Bit Descriptions for BIAS_CONTROL (Continued)

Bits	Bit Name	Description	Reset	Access
		0: disables. 1: enables.		
1	AMPLO_BIAS_CONTROL	LO amplifier bias control. 0: disables. 1: enables.	0x1	R/W
0	AMPIF_BIAS_CONTROL	IF amplifier bias control. 0: disables. 1: enables.	0x1	R/W

Mute Mask Control Register

Address: 0x101, Reset: 0xBF, Name: MUTE_MASK_CONTROL

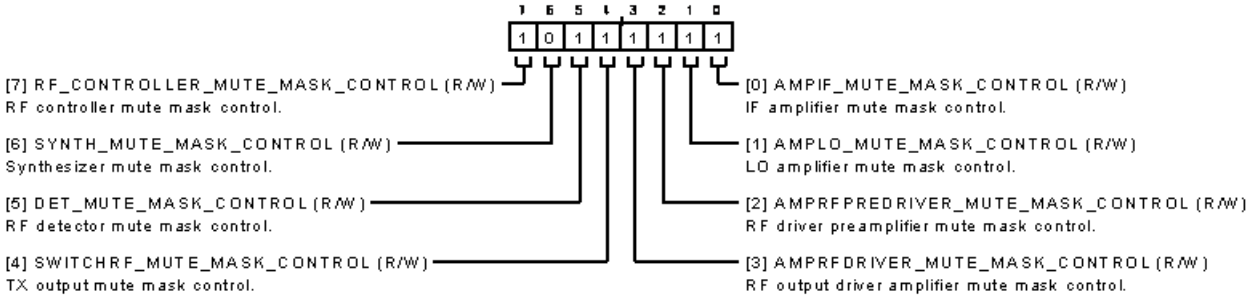


Table 12. Bit Descriptions for MUTE_MASK_CONTROL

Bits	Bit Name	Description	Reset	Access
7	RF_CONTROLLER_MUTE_MASK_CONTROL	RF controller mute mask control. 0: disables mute mask. 1: enables mute mask.	0x1	R/W
6	SYNTH_MUTE_MASK_CONTROL	Synthesizer mute mask control. 0: disables mute mask. 1: enables mute mask.	0x0	R/W
5	DET_MUTE_MASK_CONTROL	RF detector mute mask control. 0: disables mute mask. 1: enables mute mask.	0x1	R/W
4	SWITCHRF_MUTE_MASK_CONTROL	Tx output mute mask control. 0: disables mute mask. 1: enables mute mask.	0x1	R/W
3	AMPRFDRIVER_MUTE_MASK_CONTROL	RF output driver amplifier mute mask control. 0: disables mute mask. 1: enables mute mask.	0x1	R/W
2	AMPRFPREDRIVER_MUTE_MASK_CONTROL	RF driver preamplifier mute mask control. 0: disables mute mask. 1: enables mute mask.	0x1	R/W
1	AMPLO_MUTE_MASK_CONTROL	LO amplifier mute mask control. 0: disables mute mask. 1: enables mute mask.	0x1	R/W

REGISTER DETAILS

Table 12. Bit Descriptions for MUTE_MASK_CONTROL (Continued)

Bits	Bit Name	Description	Reset	Access
0	AMPIF_MUTE_MASK_CONTROL	IF amplifier mute mask control. 0: disables mute mask. 1: enables mute mask.	0x1	R/W

On Mask Control Register

Address: 0x102, Reset: 0xFF, Name: ON_MASK_CONTROL

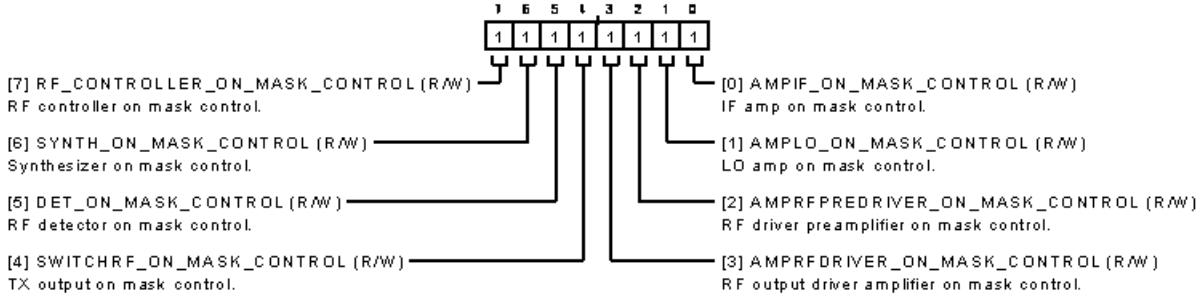


Table 13. Bit Descriptions for ON_MASK_CONTROL

Bits	Bit Name	Description	Reset	Access
7	RF_CONTROLLER_ON_MASK_CONTROL	RF controller on mask control. 0: disables on mask. 1: enables on mask.	0x1	R/W
6	SYNTH_ON_MASK_CONTROL	Synthesizer on mask control. 0: disables on mask. 1: enables on mask.	0x1	R/W
5	DET_ON_MASK_CONTROL	RF detector on mask control. 0: disables on mask. 1: enables on mask.	0x1	R/W
4	SWITCHRF_ON_MASK_CONTROL	Tx output on mask control. 0: disables on mask. 1: enables on mask.	0x1	R/W
3	AMPRFDRIVER_ON_MASK_CONTROL	RF output driver amplifier on mask control. 0: disables on mask. 1: enables on mask.	0x1	R/W
2	AMPRFPREDRIVER_ON_MASK_CONTROL	RF driver preamplifier on mask control 0: disables on mask. 1: enables on mask.	0x1	R/W
1	AMPLO_ON_MASK_CONTROL	LO amp on mask control. 0: disables on mask. 1: enables on mask.	0x1	R/W
0	AMPIF_ON_MASK_CONTROL	IF amp on mask control. 0: disables on mask. 1: enables on mask.	0x1	R/W

REGISTER DETAILS

Mute IF Unlock Register

Address: 0x103, Reset: 0x01, Name: MUTE_UNLOCK

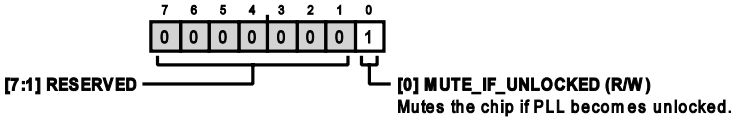


Table 14. Bit Descriptions for MUTE_UNLOCK

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	MUTE_IF_UNLOCKED	Mutes the chip if PLL becomes unlocked. 0: disables. 1: enables.	0x1	R/W

Integer Register (Lower Eight Bits)

Address: 0x200, Reset: 0x90, Name: INT_L

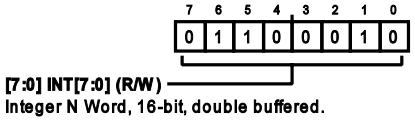


Table 15. Bit Descriptions for INT_L

Bits	Bit Name	Description	Reset	Access
[7:0]	INT[7:0]	Integer N Word, 16-bit, double buffered.	0x90	R/W

Integer Register (Upper Eight Bits)

Address: 0x201, Reset: 0x01, Name: INT_H

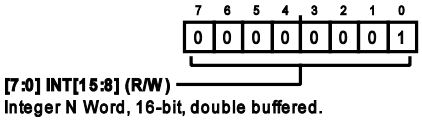
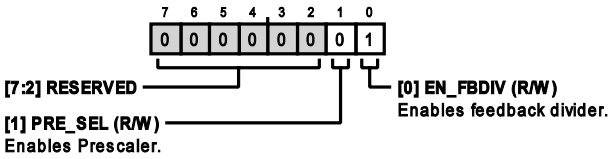


Table 16. Bit Descriptions for INT_H

Bits	Bit Name	Description	Reset	Access
[7:0]	INT[15:8]	Integer N Word, 16-bit, double buffered.	0x1	R/W

Synthesizer Configuration Register

Address: 0x20B, Reset: 0x01, Name: SYNTH



REGISTER DETAILS

Table 17. Bit Descriptions for SYNTH

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	PRE_SEL	Enables Prescaler. 1: enables. 0: disables.	0x0	R/W
0	EN_FBDIV	Enables feedback divider. 1: enables. 0: disables.	0x1	R/W

Reference Divider Register

Address: 0x20C, Reset: 0x01, Name: R_DIV

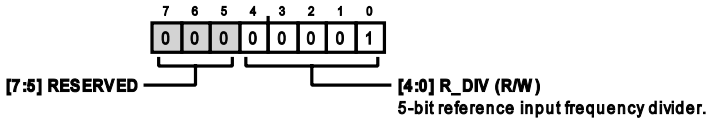


Table 18. Bit Descriptions for R_DIV

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	R_DIV	5-bit reference input frequency divider.	0x1	R/W

Reference Configuration Register

Address: 0x20E, Reset: 0x04, Name: REFERENCE

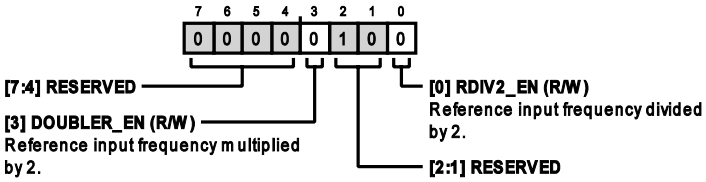


Table 19. Bit Descriptions for REFERENCE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	DOUBLER_EN	Reference input frequency multiplied by 2. 1: enables. 0: disables.	0x0	R/W
[2:1]	RESERVED	Reserved.	0x2	R/W
0	RDIV2_EN	Reference input frequency divided by 2. 1: enables. 0: disables.	0x0	R/W

Lock Detect Configuration Register

Address: 0x214, Reset: 0x48, Name: LOCK_DETECT_CONFIG

REGISTER DETAILS

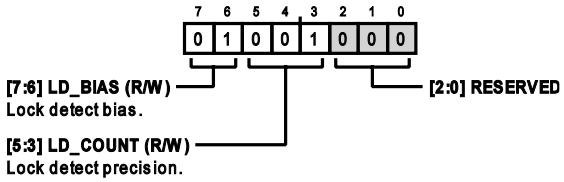


Table 20. Bit Descriptions for LOCK_DETECT_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:6]	LD_BIAS	Lock detect bias. 00: 40 µA. 01: 30 µA. 10: 20 µA. 11: 10 µA.	0x1	R/W
[5:3]	LD_COUNT	Lock detect precision. 000: checks 1024 consecutive PFD cycles to declare lock. 001: checks 2048 consecutive PFD cycles to declare lock. 010: checks 4096 consecutive PFD cycles to declare lock. 011: checks 8192 consecutive PFD cycles to declare lock.	0x1	R/W
[2:0]	RESERVED	Reserved.	0x0	R/W

Synthesizer Lock Timeout Register

Address: 0x218, Reset: 0x1F, Name: SYNTH_LOCK_TIMEOUT

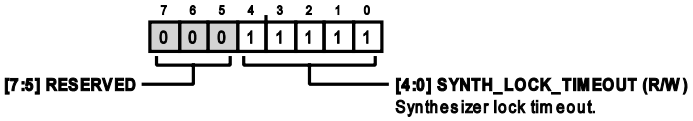


Table 21. Bit Descriptions for SYNTH_LOCK_TIMEOUT

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SYNTH_LOCK_TIMEOUT	Synthesizer lock timeout.	0x1F	R/W

VCO Timeout Register (Lower Eight Bits)

Address: 0x21C, Reset: 0x19, Name: VCO_TIMEOUT_L

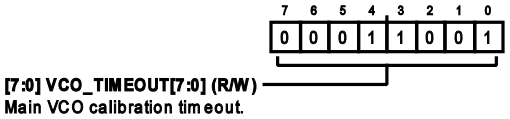


Table 22. Bit Descriptions for VCO_TIMEOUT_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_TIMEOUT[7:0]	Main VCO calibration timeout.	0x19	R/W

VCO Timeout Register (Upper Two Bits)

Address: 0x21D, Reset: 0x00, Name: VCO_TIMEOUT_H

REGISTER DETAILS

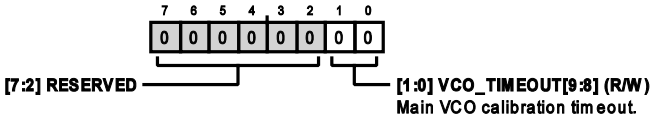


Table 23. Bit Descriptions for VCO_TIMEOUT_H

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	VCO_TIMEOUT[9:8]	Main VCO calibration timeout.	0x0	R/W

VCO Band Divider Register

Address: 0x21E, Reset: 0x10, Name: VCO_BAND_DIV

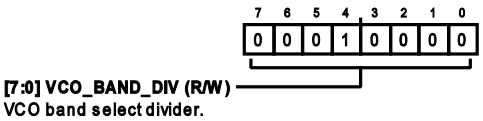


Table 24. Bit Descriptions for VCO_BAND_DIV

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_BAND_DIV	VCO band select divider.	0x10	R/W

Multifunction Synthesizer Configuration Register

Address: 0x22B, Reset: 0x09, Name: MULTI_FUNC_SYNTH_CTRL_022B

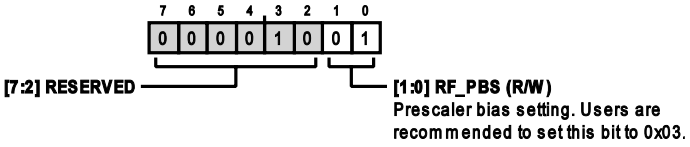


Table 25. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_022B

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x2	R
[1:0]	RF_PBS	Prescaler bias setting. Users are recommended to set this bit to 0x03.	0x1	R/W

Charge Pump Current Register

Address: 0x22E, Reset: 0x0E, Name: CP_CURR

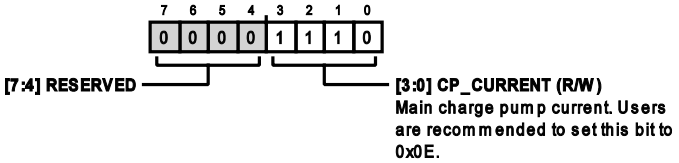


Table 26. Bit Descriptions for CP_CURR

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 26. Bit Descriptions for CP_CURR (Continued)

Bits	Bit Name	Description	Reset	Access
[3:0]	CP_CURRENT	Main charge pump current. Users are recommended to set this bit to 0x0E.	0xE	R/W

Bleed Current Register

Address: 0x22F, Reset: 0x08, Name: BICP

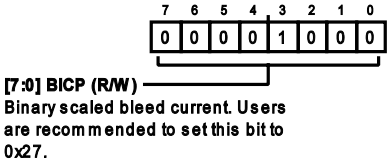


Table 27. Bit Descriptions for BICP

Bits	Bit Name	Description	Reset	Access
[7:0]	BICP	Binary scaled bleed current. Users are recommended to set this bit to 0x27.	0x8	R/W

Lock Detect Register

Address: 0x24D, Reset: 0x00, Name: LOCK_DETECT

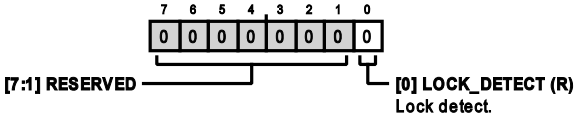


Table 28. Bit Descriptions for LOCK_DETECT

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	LOCK_DETECT	Lock detect. 1: PLL locks. 0: PLL does not lock.	0x0	R

Muxout Select Register

Address: 0x24E, Reset: 0x00, Name: MUXOUT

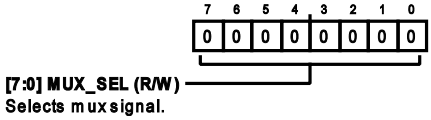


Table 29. Bit Descriptions for MUXOUT

Bits	Bit Name	Description	Reset	Access
[7:0]	MUX_SEL	Selects mux signal. 0001: digital lock detect. 0000: output low. 0100: R counter/2. 0101: N counter/2.	0x0	R/W

REGISTER DETAILS

Table 29. Bit Descriptions for MUXOUT (Continued)

Bits	Bit Name	Description	Reset	Access
		1110: output high.		

DSA Control Register

Address: 0x300, Reset: 0x00, Name: DSA_CONTROL

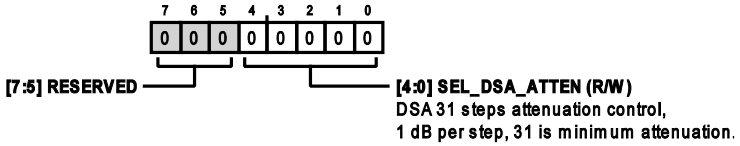


Table 30. Bit Descriptions for DSA_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SEL_DSA_ATTEN	DSA 31 steps attenuation control, 1 dB per step, 31 is minimum attenuation.	0x0	R/W

AGPIO Control Register

Address: 0x301, Reset: 0x00, Name: AGPIO_CONTROL

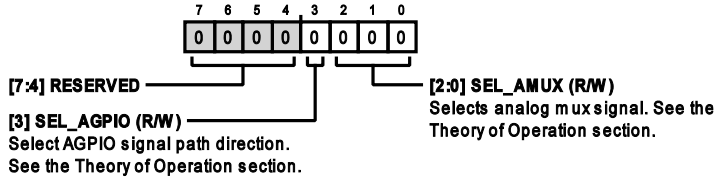


Table 31. Bit Descriptions for AGPIO_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	SEL_AGPIO	Selects AGPIO signal path direction. See the Theory of Operation section. 0: analog mux is output to AGPIO. AGPIO is output. 1: AGPIO signal sent to the analog mux. AGPIO is the input of the external signal.	0x0	R/W
[2:0]	SEL_AMUX	Selects analog mux signal. See the Theory of Operation section. 0: RF power detector. 110: temperature sensor. 111: AGPIO, must also set the SEL_AGPIO bit to 1.	0x0	R/W

ADC Control Register

Address: 0x302, Reset: 0xCA, Name: ADC_CONTROL

REGISTER DETAILS

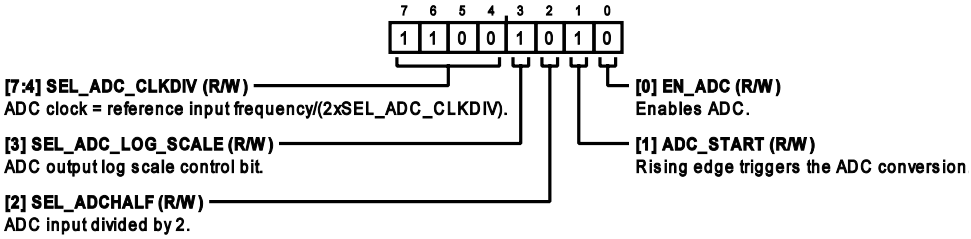


Table 32. Bit Descriptions for ADC_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:4]	SEL_ADC_CLKDIV	ADC clock = reference input frequency/(2 × SEL_ADC_CLKDIV).	0xC	R/W
3	SEL_ADC_LOG_SCALE	ADC output log scale control bit. 1: enables ADC output log scale. 0: disables ADC output log scale.	0x1	R/W
2	SEL_ADCHALF	ADC input divided by 2. 0: disables. 1: enables.	0x0	R/W
1	ADC_START	Rising edge triggers the ADC conversion.	0x1	R/W
0	EN_ADC	Enables ADC. 0: disables. 1: enables.	0x0	R/W

ADC Status Register

Address: 0x303, Reset: 0x01, Name: ADC_STATUS

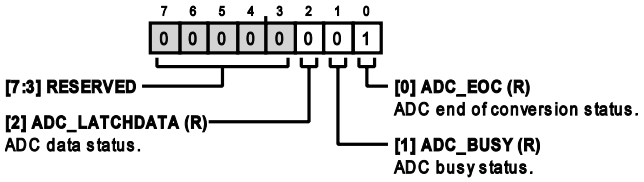


Table 33. Bit Descriptions for ADC_STATUS

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	ADC_LATCHDATA	ADC data status. 1: data is ready. 0: data is not ready.	0x0	R
1	ADC_BUSY	ADC busy status. 1: ADC is busy. 0: ADC is not busy.	0x0	R
0	ADC_EOC	ADC end of conversion status. 0: ADC conversion is not complete. 1: ADC conversion is complete.	0x1	R

ADC Data Register

Address: 0x304, Reset: 0xEF, Name: ADC_DATA

REGISTER DETAILS

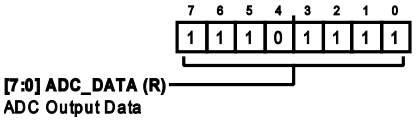


Table 34. Bit Descriptions for ADC_DATA

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_DATA	ADC Output Data	0xEF	R

GPIO Write Register

Address: 0x305, Reset: 0x00, Name: GPIO_WRITEVALS

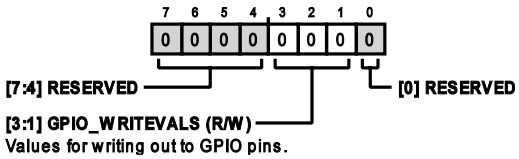


Table 35. Bit Descriptions for GPIO_WRITEVALS

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:1]	GPIO_WRITEVALS	Values for writing out to the GPIO pins.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

GPIO Read Register

Address: 0x306, Reset: 0x0E, Name: GPIO_READVALS

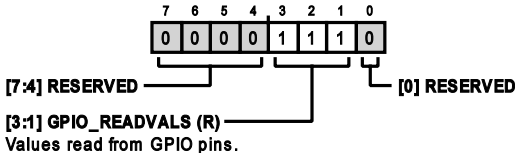


Table 36. Bit Descriptions for GPIO_READVALS

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:1]	GPIO_READVALS	Values read from the GPIO pins.	0x7	R
0	RESERVED	Reserved.	0x0	R

GPIO Control Register

Address: 0x307, Reset: 0x00, Name: GPIO_CONTROL

REGISTER DETAILS

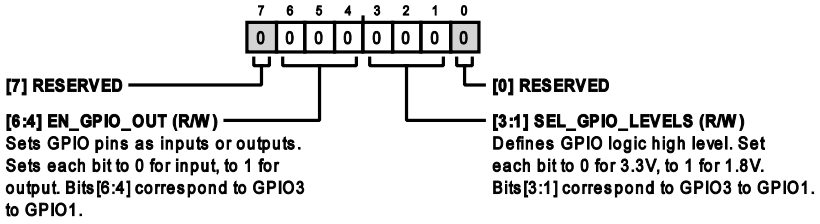


Table 37. Bit Descriptions for GPIO_CONTROL

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:4]	EN_GPIO_OUT	Sets GPIO pins as inputs or outputs. Sets each bit to 0 for input, to 1 for output. Bits[6:4] correspond from GPIO3 to GPIO1.	0x0	R/W
[3:1]	SEL_GPIO_LEVELS	Defines GPIO logic high level. Sets each bit to 0 for 3.3 V, to 1 for 1.8 V. Bits[3:1] correspond to GPIO3 to GPIO1.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

RF Bias Control 1 Register

Address: 0x308, Reset: 0x08, Name: RFBIAS_CONTROL1

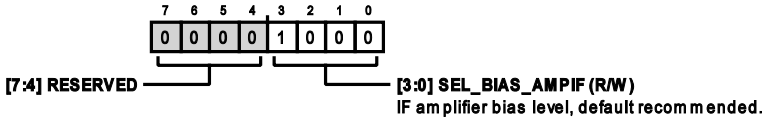


Table 38. Bit Descriptions for RFBIAS_CONTROL1

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	SEL_BIAS_AMPIF	IF amplifier bias level, default recommended.	0x8	R/W

RF Bias Control 2 Register

Address: 0x309, Reset: 0x88, Name: RFBIAS_CONTROL2

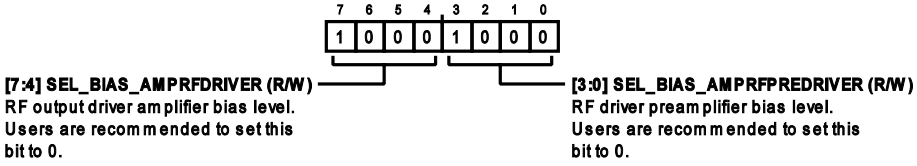


Table 39. Bit Descriptions for RFBIAS_CONTROL2

Bits	Bit Name	Description	Reset	Access
[7:4]	SEL_BIAS_AMPRFDRIVER	RF output driver amplifier bias level. Users are recommended to set this bit to 0.	0x8	R/W
[3:0]	SEL_BIAS_AMPRFPREDRIVER	RF driver preamplifier bias level. Users are recommended to set this bit to 0.	0x8	R/W

RF Bias Control 3 Register

Address: 0x30A, Reset: 0x88, Name: RFBIAS_CONTROL3

REGISTER DETAILS

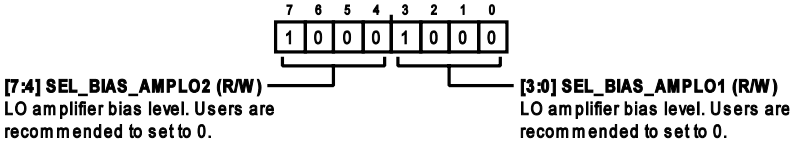


Table 40. Bit Descriptions for RFBIAS_CONTROL3

Bits	Bit Name	Description	Reset	Access
[7:4]	SEL_BIAS_AMPLO2	LO amplifier bias level. Users are recommended to set to 0.	0x8	R/W
[3:0]	SEL_BIAS_AMPLO1	LO amplifier bias level. Users are recommended to set to 0.	0x8	R/W

Detector Control Register

Address: 0x30C, Reset: 0x00, Name: DETECTOR_CONTROL

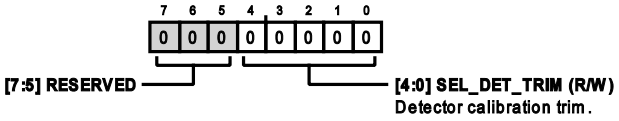


Table 41. Bit Descriptions for DETECTOR_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SEL_DET_TRIM	Detector calibration trim.	0x0	R/W

Mixer Bias Control 1 Register

Address: 0x30D, Reset: 0x08, Name: MIXER_CONTROL1

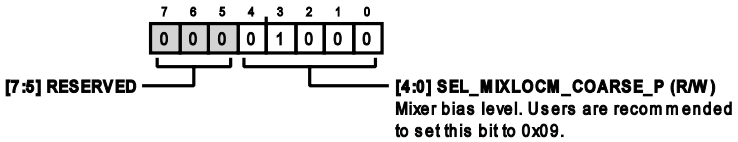
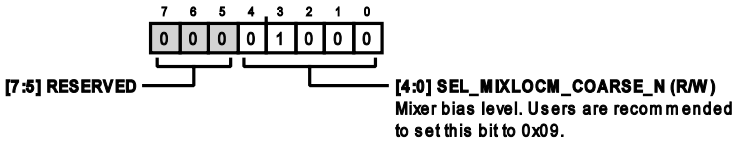


Table 42. Bit Descriptions for MIXER_CONTROL1

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SEL_MIXLOCM_COARSE_P	Mixer bias level. Users are recommended to set this bit to 0x09.	0x8	R/W

Mixer Bias Control 2 Register

Address: 0x30E, Reset: 0x08, Name: MIXER_CONTROL2



REGISTER DETAILS

Table 43. Bit Descriptions for MIXER_CONTROL2

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SEL_MIXLOCM_COARSE_N	Mixer bias level. Users are recommended to set this bit to 0x09.	0x8	R/W

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CP-40-7	LFCSP	40-Lead, Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

Updated: June 30, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADMV4630BCPZN	-40°C to +85°C	40-Lead LFCSP (6mm x 6mm w/ EP)	Reel, 50	CP-40-7
ADMV4630BCPZN-RL7	-40°C to +85°C	40-Lead LFCSP (6mm x 6mm w/ EP)	Reel, 750	CP-40-7

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADMV4630Z	Evaluation Assembly Board

[1] Z = RoHS Compliant Part.