



FEATURES

- Digital gyroscope with range scaling**
±75°/sec, ±150°/sec, ±300°/sec settings
- Triaxis digital accelerometer: ±3 g**
- Wide sensor bandwidth: 330 Hz**
- Autonomous operation and data collection**
No external configuration commands required
Start-up time: 180 ms
Sleep mode recovery time: 4 ms
- Factory-calibrated sensitivity, bias, and alignment**
- Calibration temperature range: -40°C to +85°C**
- SPI-compatible serial interface**
- Embedded temperature sensor**
- Programmable operation and control**
Automatic and manual bias correction controls
Bartlett window FIR filter length, number of taps
Digital I/O: data-ready, alarm indicator, general-purpose
Alarms for condition monitoring
Sleep mode for power management
DAC output voltage
Enable external sample clock input: up to 1.2 kHz
Single-command self-test
- Single-supply operation: 4.75 V to 5.25 V**
- 2000 g shock survivability**
- Operating temperature range: -40°C to +85°C**

APPLICATIONS

- Medical instrumentation
- Robotics
- Platform controls
- Navigation

GENERAL DESCRIPTION

The *iSensor*® ADIS16305 is a complete inertial system that includes a gyroscope and triaxis accelerometer. Each sensor in the ADIS16305 combines industry-leading *iMEMS*® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyro bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements over a variety of conditions.

The ADIS16305 provides a simple, cost-effective method for integrating accurate, multi-axis, inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion

FUNCTIONAL BLOCK DIAGRAM

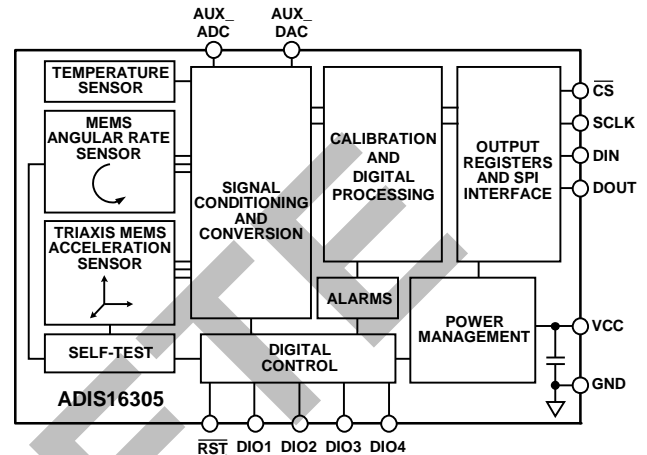


Figure 1.

testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. An improved SPI interface and register structure provide faster data collection and configuration control. The ADIS16305 uses a pinout that is compatible with the ADIS1635x, ADIS1636x, and ADIS1640x families, when used with an interface flex connector.

This compact module is approximately 23 mm × 31 mm × 8 mm and provides a standard connector interface, which enables horizontal or vertical mounting.

Rev. A

[Document Feedback](#)

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

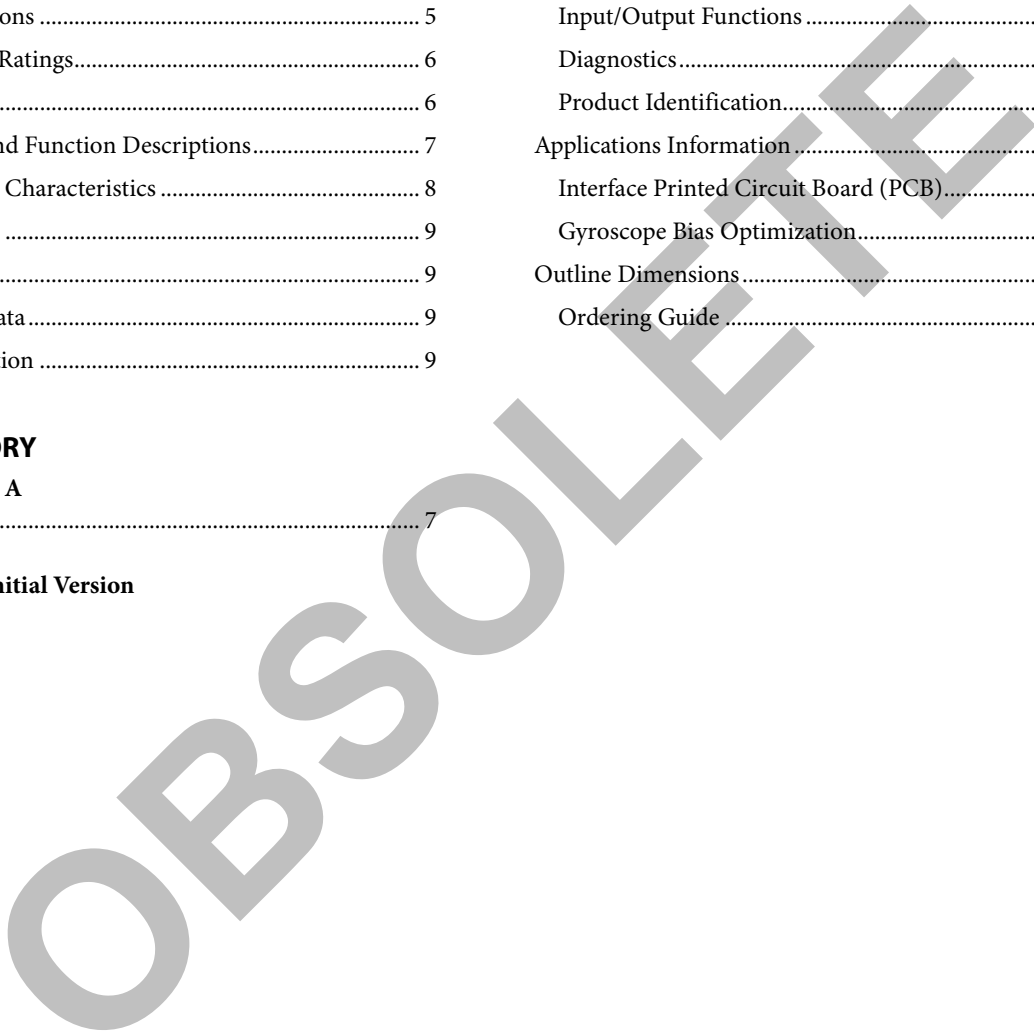
TABLE OF CONTENTS

Features	1	Memory Map	10
Applications.....	1	Burst Read Data Collection	11
Functional Block Diagram	1	Output Data Registers	11
General Description	1	Orientation Angles.....	12
Revision History	2	Calibration.....	13
Specifications.....	3	Operational Control.....	13
Timing Specifications	5	Input/Output Functions	15
Absolute Maximum Ratings.....	6	Diagnostics.....	16
ESD Caution.....	6	Product Identification.....	17
Pin Configuration and Function Descriptions.....	7	Applications Information	18
Typical Performance Characteristics	8	Interface Printed Circuit Board (PCB).....	18
Theory of Operation	9	Gyroscope Bias Optimization.....	18
Basic Operation	9	Outline Dimensions	19
Reading Sensor Data.....	9	Ordering Guide	19
Device Configuration	9		

REVISION HISTORY

6/14—Rev. 0 to Rev. A
 Changes to Figure 6..... 7

7/10—Revision 0: Initial Version



SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, angular rate = $0^\circ/\text{sec}$, dynamic range = $\pm 300^\circ/\text{sec} \pm 1\text{ g}$, unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
GYROSCOPE					
Dynamic Range		± 300	± 350		$^\circ/\text{sec}$
Initial Sensitivity	$T_A = 25^\circ\text{C}$, dynamic range = $\pm 300^\circ/\text{sec}$	0.0495	0.05	0.0505	$^\circ/\text{sec}/\text{LSB}$
	$T_A = 25^\circ\text{C}$, dynamic range = $\pm 150^\circ/\text{sec}$		0.025		$^\circ/\text{sec}/\text{LSB}$
	$T_A = 25^\circ\text{C}$, dynamic range = $\pm 75^\circ/\text{sec}$		0.0125		$^\circ/\text{sec}/\text{LSB}$
Sensitivity Temperature Coefficient	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		20		ppm/ $^\circ\text{C}$
Misalignment	Reference to z-axis accelerometer, $T_A = 25^\circ\text{C}$		± 0.1		Degrees
Nonlinearity	Best-fit straight line		0.1		% of FS
Initial Bias Error	$T_A = 25^\circ\text{C}$, $\pm 1\sigma$		± 3		$^\circ/\text{sec}$
In-Run Bias Stability	$T_A = 25^\circ\text{C}$, 1σ , SMPL_PRD = 0x01		0.006		$^\circ/\text{sec}$
Angular Random Walk	$T_A = 25^\circ\text{C}$, 1σ , SMPL_PRD = 0x01		1.85		$^\circ/\sqrt{\text{hr}}$
Bias Temperature Coefficient	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.006		$^\circ/\text{sec}/^\circ\text{C}$
Linear Acceleration Effect on Bias	Any axis, 1σ (MSC_CTRL Bit[7] = 1)		0.02		$^\circ/\text{sec}/\text{g}$
Voltage Sensitivity	$V_{CC} = 4.75\text{ V}$ to 5.25 V		0.32		$^\circ/\text{sec}/\text{V}$
Output Noise	$T_A = 25^\circ\text{C}$, $\pm 300^\circ/\text{sec}$ range, no filtering		0.73		$^\circ/\text{sec}$ rms
Rate Noise Density	$T_A = 25^\circ\text{C}$, $f = 25\text{ Hz}$, $\pm 300^\circ/\text{sec}$, no filtering		0.04		$^\circ/\text{sec}/\sqrt{\text{Hz}}$ rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			14.5		kHz
Self-Test Change in Output Response	$\pm 300^\circ/\text{sec}$ range setting	± 696	± 1400	± 2449	LSB
ACCELEROMETERS					
	Each axis				
Dynamic Range		± 3	± 3.6		g
Initial Sensitivity	25°C	0.594	0.6	0.606	mg/LSB
Sensitivity Temperature Coefficient	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		25		ppm/ $^\circ\text{C}$
Misalignment	Axis-to-axis, $T_A = 25^\circ\text{C}$, $\Delta = 90^\circ$ ideal		± 0.1		Degrees
	Axis-to-frame (package), $T_A = 25^\circ\text{C}$		± 0.5		Degrees
Nonlinearity	Best-fit straight line		± 0.3		% of FS
Initial Bias Error	$T_A = 25^\circ\text{C}$, $\pm 1\sigma$		± 60		mg
In-Run Bias Stability	$T_A = 25^\circ\text{C}$, 1σ , SMPL_PRD = 0x01		0.037		mg
Velocity Random Walk	$T_A = 25^\circ\text{C}$, 1σ , X axis and Y axis		0.1		m/sec/ $\sqrt{\text{hr}}$
	$T_A = 25^\circ\text{C}$, 1σ , Z axis		0.16		m/sec/ $\sqrt{\text{hr}}$
Bias Temperature Coefficient	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.3		mg/ $^\circ\text{C}$
Output Noise	$T_A = 25^\circ\text{C}$, no filtering, X axis and Y axis		4.25		mg rms
	$T_A = 25^\circ\text{C}$, no filtering, Z axis		6.5		mg rms
Noise Density	$T_A = 25^\circ\text{C}$, no filtering, X axis and Y axis		225		$\mu\text{g}/\sqrt{\text{Hz}}$ rms
	$T_A = 25^\circ\text{C}$, no filtering, Z axis		340		$\mu\text{g}/\sqrt{\text{Hz}}$ rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			5.5		kHz
Self-Test Change in Output Response	X axis and Y axis	500	1100	1700	LSB
	Z axis	90	450	860	LSB
ADC INPUT					
Resolution			12		Bits
Integral Nonlinearity			± 2		LSB
Differential Nonlinearity			± 1		LSB
Offset Error			± 4		LSB
Gain Error			± 2		LSB
Input Range		0		3.3	V
Input Capacitance	During acquisition		20		pF

Parameter	Test Conditions	Min	Typ	Max	Unit
DAC OUTPUT	5 k Ω /100 pF to GND				
Resolution			12		Bits
Relative Accuracy	For Code 101 to Code 4095		± 4		LSB
Differential Nonlinearity			± 1		LSB
Offset Error			± 5		mV
Gain Error			± 0.5		%
Output Range		0		3.3	V
Output Impedance			2		Ω
Output Settling Time			10		μ s
LOGIC INPUTS ¹					
Input High Voltage, V _{INH}		2.0			V
Input Low Voltage, V _{INL}				0.8	V
$\overline{\text{CS}}$ Wake-Up Pulse Width	$\overline{\text{CS}}$ signal to wake up from sleep mode			0.55	V
Logic 1 Input Current, I _{INH}	V _{IH} = 3.3 V		± 0.2	± 10	μ A
Logic 0 Input Current, I _{INL}	V _{IL} = 0 V				
All Pins Except $\overline{\text{RST}}$			-40	-60	μ A
$\overline{\text{RST}}$ Pin			-1		mA
Input Capacitance, C _{IN}			10		pF
DIGITAL OUTPUTS ¹					
Output High Voltage, V _{OH}	I _{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V _{OL}	I _{SINK} = 1.6 mA			0.4	V
FLASH MEMORY					
Data Retention ³	Endurance ²	10,000			Cycles
	T _J = 85°C	20			Years
FUNCTIONAL TIMES ⁴					
Power-On Start-Up Time	Time until data is available Normal mode, SMPL_PRD \leq 0x09 Low power mode, SMPL_PRD \geq 0x0A		180		ms
Reset Recovery Time	Normal mode, SMPL_PRD \leq 0x09 Low power mode, SMPL_PRD \geq 0x0A		250		ms
Sleep Mode Recovery Time	Normal mode, SMPL_PRD \leq 0x09 Low power mode, SMPL_PRD \geq 0x0A		55		ms
Flash Memory Test Time	Normal mode, SMPL_PRD \leq 0x09 Low power mode, SMPL_PRD \geq 0x0A		120		ms
Automatic Self-Test Time			4		ms
CONVERSION RATE	SMPL_PRD = 0x01 to 0xFF	0.413		819.2	SPS
Clock Accuracy				± 3	%
Sync Input Clock				1.2	kHz
POWER SUPPLY					
Power Supply Current	Operating voltage range, VCC	4.75	5.0	5.25	V
	Low power mode at 25°C		18		mA
	Normal mode at 25°C		42		mA
	Sleep mode at 25°C		500		μ A

¹ The digital I/O signals are driven by an internal 3.3 V supply, and the inputs are 5 V tolerant.

² Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at -40°C, +25°C, +85°C, and +125°C.

³ The retention lifetime equivalent is at a junction temperature (T_J) of 85°C as per JEDEC Standard 22, Method A117. Retention lifetime decreases with junction temperature.

⁴ These times do not include thermal settling and internal filter response times (330 Hz bandwidth), which may impact overall accuracy.

TIMING SPECIFICATIONS

T_A = 25°C, VCC = 5 V, unless otherwise noted.

Table 2.

Parameter	Description	Normal Mode (SMPL_PRD ≤ 0x09)			Low Power Mode (SMPL_PRD ≥ 0x0A)			Burst Read			Unit
		Min ¹	Typ	Max	Min ¹	Typ	Max	Min ¹	Typ	Max	
f _{SCLK}	Serial clock	0.01		2.0	0.01		0.3	0.01		1.0	MHz
t _{STALL}	Stall period between data	9			75			1/f _{SCLK}			μs
t _{READRATE}	Read rate	40			100						μs
t _{CS}	Chip select to clock edge	48.8			48.8			48.8			ns
t _{DAV}	DOUT valid after SCLK edge			100			100			100	ns
t _{DSU}	DIN setup time before SCLK rising edge	24.4			24.4			24.4			ns
t _{DHD}	DIN hold time after SCLK rising edge	48.8			48.8			48.8			ns
t _{SCLKR} , t _{SCLKF}	SCLK rise/fall times (not shown in figures)		5	12.5		5	12.5		5	12.5	ns
t _{DR} , t _{DF}	DOUT rise/fall times (not shown in figures)		5	12.5		5	12.5		5	12.5	ns
t _{SFS}	CS high after SCLK edge	5			5			5			ns
t ₁	Input sync positive pulse width	5						5			μs
t _x	Input sync low time	100						100			μs
t ₂	Input sync to data-ready output		600						600		μs
t ₃	Input sync period	833						833			μs

¹ Guaranteed by design and characterization, but not tested in production.

Timing Diagrams

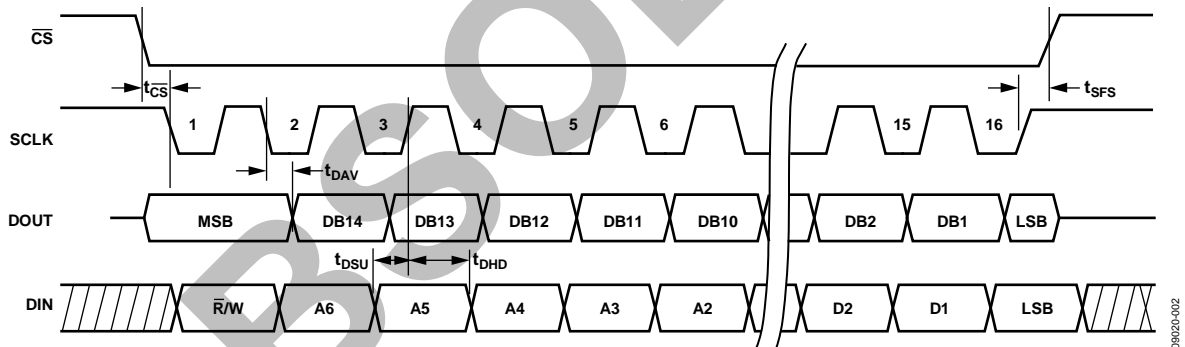


Figure 2. SPI Timing and Sequence

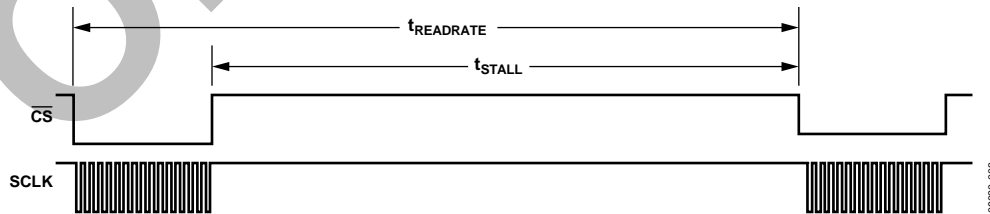


Figure 3. Stall Time and Data Rate

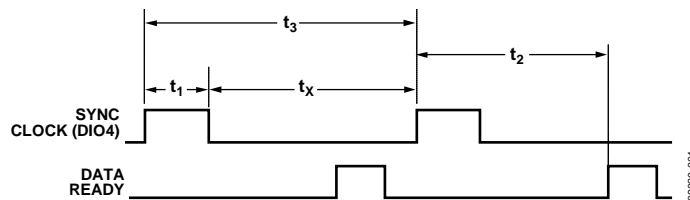


Figure 4. Input Clock Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 <i>g</i>
Any Axis, Powered	2000 <i>g</i>
VCC to GND	−0.3 V to +6.0 V
Digital Input Voltage to GND	−0.3 V to +5.3 V
Digital Output Voltage to GND	−0.3 V to VCC + 0.3 V
Analog Input to GND	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C ^{1, 2}

¹ Extended exposure to temperatures outside the specified temperature range of −40°C to +85°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of −40°C to +85°C.

² Although the device is capable of withstanding short-term exposure to 150°C, long-term exposure threatens internal mechanical integrity.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

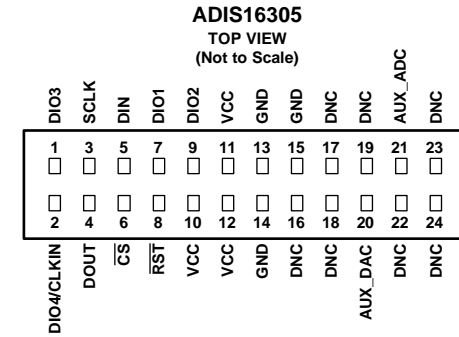
Package Type	θ_{JA}	θ_{JC}	Device Weight
24-Lead Module	39.8°C/W	14.2°C/W	6.1 grams (max)

ESD CAUTION



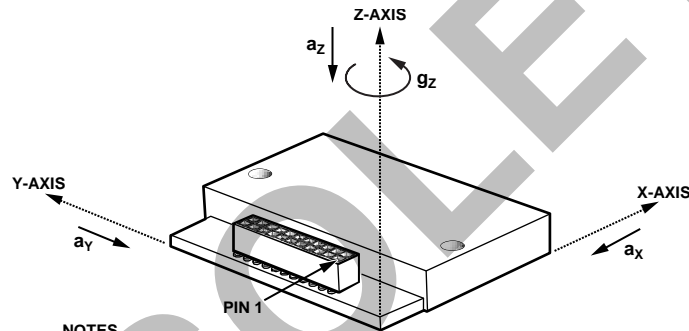
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. MATING CONNECTOR: SAMTEC FTSH-112-03 OR EQUIVALENT.
 2. DNC = DO NOT CONNECT.

Figure 5. ADIS16305 Pin Configuration



- NOTES**
1. THE ARROW DIRECTION ASSOCIATED WITH a_z , a_y , AND g_z INDICATES THE DIRECTION OF MOTION THAT PRODUCES A POSITIVE RESPONSE IN EACH ACCELEROMETER AND GYROSCOPE OUTPUT REGISTER.

Figure 6. Axial Orientation

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
1	DIO3	I/O	Configurable Digital Input/Output.
2	DIO4/CLKIN	I/O	Configurable Digital Input/Output or Sync Clock Input.
3	SCLK	I	SPI Serial Clock.
4	DOUT	O	SPI Data Output. Clocks output on SCLK falling edge.
5	DIN	I	SPI Data Input. Clocks input on SCLK rising edge.
6	CS	I	SPI Chip Select.
7, 9	DIO1, DIO2	I/O	Configurable Digital Input/Output.
8	RST	I	Reset.
10, 11, 12	VCC	S	Power Supply.
13, 14, 15	GND	S	Power Ground.
16, 17, 18, 19, 22, 23, 24	DNC	N/A	Do Not Connect.
20	AUX_DAC	O	Auxiliary, 12-Bit DAC Output.
21	AUX_ADC	I	Auxiliary, 12-Bit ADC Input.

¹ I/O is input/output, I is input, O is output, S is supply, and N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

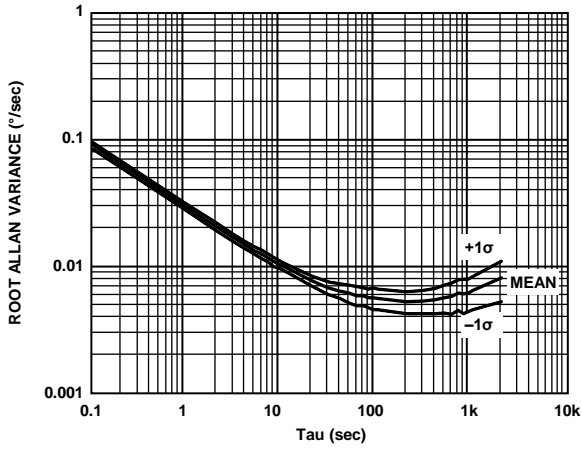


Figure 7. Gyroscope Allan Variance

09020-007

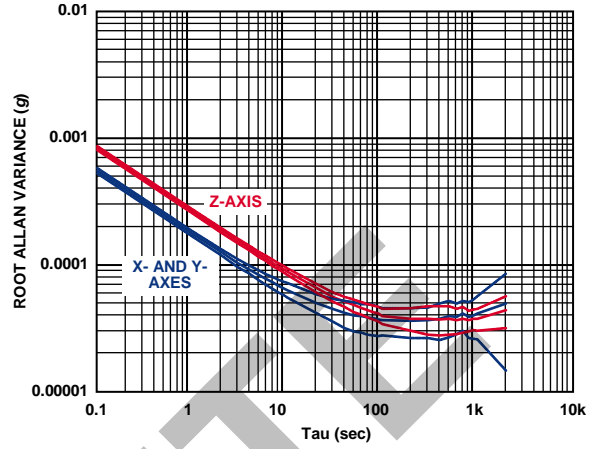


Figure 8. Accelerometer Allan Variance

09020-008

OBSOLETE

THEORY OF OPERATION

BASIC OPERATION

The ADIS16305 is an autonomous sensor system that starts up after it has a valid power supply voltage and begins producing inertial measurement data. After each sample cycle, the sensor data is loaded into the output registers, and DIO1 pulses high, which provides a new data-ready control signal for driving system-level interrupt service routines. In a typical system, a master processor accesses the output data registers through the SPI interface, using the connection diagram shown in Figure 9. Table 6 provides a generic functional description for each pin on the master processor. Table 7 describes the typical master processor settings for communicating with the ADIS16305.

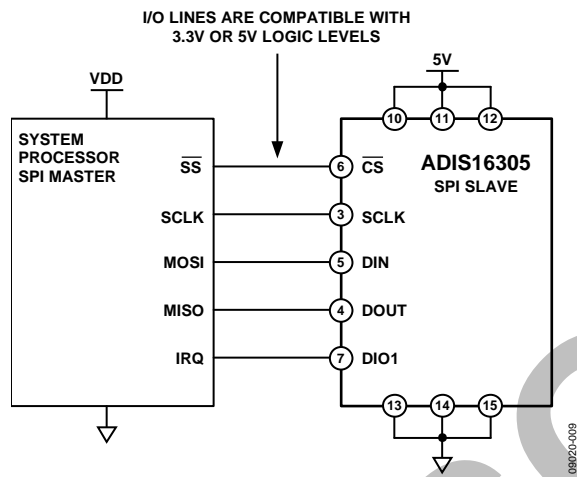


Figure 9. Electrical Connection Diagram

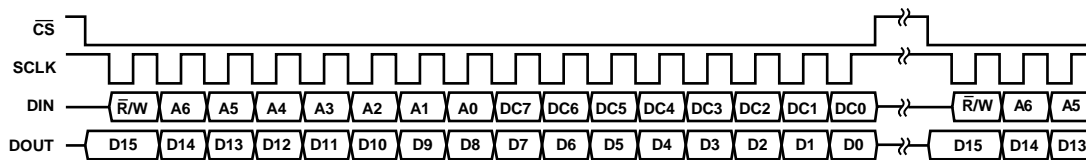
Table 6. Generic Master Processor Pin Names and Functions

Pin Name	Function
SS	Slave select
IRQ	Interrupt request
MOSI	Master output, slave input
MISO	Master input, slave output
SCLK	Serial clock

Table 7. Generic Master Processor SPI Settings

Processor Setting	Description
Master	ADIS16305 is a slave
SCLK Rate ≤ 2 MHz ¹	Normal mode, SMPL_PRR[7:0] $\leq 0x09$
SPI Mode 3	CPOL = 1 (polarity), CHPA = 1 (phase)
MSB First Mode	Bit sequence
16-Bit Mode	Shift register/data length

¹ For burst read, SCLK rate ≤ 1 MHz. For low power mode, SCLK rate ≤ 300 kHz.



NOTES

1. DOUT BITS ARE PRODUCED ONLY WHEN THE PREVIOUS 16-BIT DIN SEQUENCE STARTS WITH $\bar{R}/W = 0$.

Figure 11. SPI Communication Bit Sequence

The user registers provide addressing for all input/output operations on the SPI interface. Each 16-bit register has two 7-bit addresses: one for its upper byte and one for its lower byte. Table 8 lists the lower byte address for each register, and Figure 10 shows the generic bit assignments.

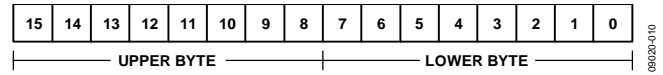


Figure 10. Generic Register Bit Assignments

READING SENSOR DATA

Although the ADIS16305 produces data independently, it operates as an SPI slave device that communicates with system (master) processors using the 16-bit segments displayed in Figure 11. Individual register reads require two of these 16-bit sequences. The first 16-bit sequence provides the read command bit ($\bar{R}/W = 0$) and the target register address (A6 to A0). The second sequence transmits the register contents (D15 to D0) on the DOUT line. For example, if $DIN = 0x0A00$, the contents of XACCL_OUT are shifted out on the DOUT line during the next 16-bit sequence.

The SPI operates in full-duplex mode, which means that the master processor can read the output data from DOUT while using the same SCLK pulses to transmit the next target address on DIN.

DEVICE CONFIGURATION

The user register memory map (see Table 8) identifies configuration registers with either a W or R/W. Configuration commands also use the bit sequence shown in Figure 11. If the MSB = 1, the last eight bits (DC7 to DC0) in the DIN sequence are loaded into the memory address associated with the address bits (A6 to A0). For example, if $DIN = 0xA11F$, $0x1F$ is loaded into Address $0x21$ (XACCL_OFF, upper byte) at the conclusion of the data frame.

The master processor initiates the backup function by setting $GLOB_CMD[3] = 1$ ($DIN = 0xBE04$). This command copies the user registers into their assigned flash memory locations and requires the power supply to stay within its normal operating range for the entire 50 ms process. The FLASH_CNT register provides a running count of these events for monitoring the long-term reliability of the flash memory.

MEMORY MAP

Table 8. User Register Memory Map

Name	R/W	Flash Backup	Address ¹	Default	Register Description	Bit Function
FLASH_CNT	R	Yes	0x00	N/A ²	Flash memory write count	See Table 28
SUPPLY_OUT	R	No	0x02	N/A ²	Power supply measurement	See Table 9
GYRO_OUT	R	No	0x04	N/A ²	Gyroscope output	See Table 9
Reserved	N/A ²	N/A ²	0x06	N/A ²	Reserved	N/A ²
Reserved	N/A ²	N/A ²	0x08	N/A ²	Reserved	N/A ²
XACCL_OUT	R	No	0x0A	N/A ²	X-axis accelerometer output	See Table 9
YACCL_OUT	R	No	0x0C	N/A ²	Y-axis accelerometer output	See Table 9
ZACCL_OUT	R	No	0x0E	N/A ²	Z-axis accelerometer output	See Table 9
TEMP_OUT	R	No	0x10	N/A ²	Gyroscope temperature measurement	See Table 9
PITCH_OUT	R	No	0x12	N/A ²	Pitch angle output (x-axis)	See Table 9
ROLL_OUT	R	No	0x14	N/A ²	Roll angle output (y-axis)	See Table 9
AUX_ADC	R	No	0x16	N/A ²	Auxiliary ADC output	See Table 9
Reserved	N/A ²	N/A ²	0x18	N/A ²	Reserved	N/A ²
GYRO_OFF	R/W	Yes	0x1A	0x0000	Gyroscope bias offset factor	See Table 16
PITCH_OFF	R	Yes	0x1C	N/A ²	Pitch angle offset factor	See Table 18
ROLL_OFF	R	Yes	0x1E	N/A ²	Roll angle offset factor	See Table 18
XACCL_OFF	R/W	Yes	0x20	0x0000	X-axis acceleration bias offset factor	See Table 17
YACCL_OFF	R/W	Yes	0x22	0x0000	Y-axis acceleration bias offset factor	See Table 17
ZACCL_OFF	R/W	Yes	0x24	0x0000	Z-axis acceleration bias offset factor	See Table 17
ALM_MAG1	R/W	Yes	0x26	0x0000	Alarm 1 amplitude threshold	See Table 30
ALM_MAG2	R/W	Yes	0x28	0x0000	Alarm 2 amplitude threshold	See Table 30
ALM_SMPL1	R/W	Yes	0x2A	0x0000	Alarm 1 sample size	See Table 31
ALM_SMPL2	R/W	Yes	0x2C	0x0000	Alarm 2 sample size	See Table 31
ALM_CTRL	R/W	Yes	0x2E	0x0000	Alarm control	See Table 32
AUX_DAC	R/W	No	0x30	0x0000	Auxiliary DAC data	See Table 25
GPIO_CTRL	R/W	No	0x32	0x0000	Auxiliary digital input/output control	See Table 23
MSC_CTRL	R/W	Yes	0x34	0x0006	Miscellaneous control: data-ready, self-test	See Table 24
SMPL_PRD	R/W	Yes	0x36	0x0001	Internal sample period (rate) control	See Table 20
SENS_AVG	R/W	Yes	0x38	0x0402	Dynamic range and digital filter control	See Table 22
SLP_CNT	W	No	0x3A	0x0000	Sleep mode control	See Table 21
DIAG_STAT	R	No	0x3C	0x0000	System status	See Table 29
GLOB_CMD	W	N/A ²	0x3E	0x0000	System command	See Table 19
Reserved	N/A ²	N/A ²	0x40 to 0x51	N/A ²	Reserved	N/A ²
LOT_ID1	R	Yes	0x52	N/A ²	Lot Identification Code 1	See Table 35
LOT_ID2	R	Yes	0x54	N/A ²	Lot Identification Code 2	See Table 35
PROD_ID	R	Yes	0x56	0x3FB1	Product identification	See Table 35
SERIAL_NUM	R	Yes	0x58	N/A ²	Serial number	See Table 35

¹ Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte plus 1.² N/A stands for not applicable.

BURST READ DATA COLLECTION

Burst read data collection is a process-efficient method for collecting data from the ADIS16305. In burst read, all output registers are clocked out on DOUT, 16 bits at a time, in sequential data cycles (each separated by one SCLK period). To start a burst read sequence, set DIN = 0x3E00. The contents of each output register are then shifted out on DOUT, starting with SUPPLY_OUT and ending with AUX_ADC (see Figure 13). The addressing sequence shown in Table 8 determines the order of the outputs in burst read.

OUTPUT DATA REGISTERS

Each output data register uses the format in Figure 12 and Table 9. Figure 6 shows the positive direction for each inertial sensor. The ND bit is equal to 1 when the register contains unread data. The EA bit is high when any error/alarm flag in the DIAG_STAT register is equal to 1.

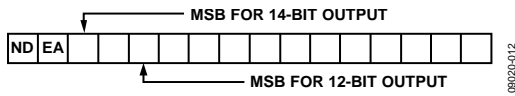


Figure 12. Output Register Bit Assignments

Table 9. Output Data Register Formats

Name	Address	Scale	Reference
SUPPLY_OUT	0x02	Power supply	Table 13
GYRO_OUT ¹	0x04	Gyroscope	Table 10
XACCL_OUT	0x0A	Acceleration (x)	Table 11
YACCL_OUT	0x0C	Acceleration (y)	Table 11
ZACCL_OUT	0x0E	Acceleration (z)	Table 11
TEMP_OUT ²	0x10	Temperature	Table 14
PITCH_OUT	0x12	Pitch angle	Table 12
ROLL_OUT	0x14	Roll angle	Table 12
AUX_ADC	0x16	ADC measurement	Table 15

¹ Assumes that the scaling is set to ±300°/sec. This factor scales with the range.
² 0x0000 = 25°C (±5°C).

Note that the codes in Table 10, Table 11, Table 12, Table 13, Table 14, and Table 15 assume typical sensitivity values.

Gyroscopes

The gyroscope output register, GYRO_OUT, uses a 14-bit, twos complement digital format. When using the factory-default range of ±300°/sec, each LSB translates into 0.05°/sec. Table 10 offers some examples for translating the digital data into rotation rate measurements. When the dynamic range is set to ±150°/sec, divide the rotation rate numbers in Table 10 by a factor of two. When the dynamic range is set to ±75°/sec, divide the rotation rate numbers in Table 10 by a factor of four.

Table 10. Rotation Rate, Twos Complement Format

Rotation Rate	Decimal	Hex	Binary
+300°/sec	+6000 LSB	0x1770	XX01 0111 0111 0000
+0.1°/sec	+2 LSB	0x0002	XX00 0000 0000 0010
+0.05°/sec	+1 LSB	0x0001	XX00 0000 0000 0001
0°/sec	0 LSB	0x0000	XX00 0000 0000 0000
-0.05°/sec	-1 LSB	0x3FFF	XX11 1111 1111 1111
-0.1°/sec	-2 LSB	0x3FFE	XX11 1111 1111 1110
-300°/sec	-6000 LSB	0x2890	XX10 1000 1001 0000

Accelerometers

The accelerometer output registers, XACCL_OUT, YACCL_OUT, and ZACCL_OUT, use a 14-bit, twos complement digital format. Table 11 offers some examples for translating the digital data into linear acceleration measurements

Table 11. Acceleration, Twos Complement Format

Acceleration	Decimal	Hex	Binary
+3.3 g	+5500 LSB	0x157C	XX01 0101 0111 1100
+1.2 mg	+2 LSB	0x0002	XX00 0000 0000 0010
+0.6 mg	+1 LSB	0x0001	XX00 0000 0000 0001
0 g	0 LSB	0x0000	XX00 0000 0000 0000
-0.6 mg	-1 LSB	0x3FFF	XX11 1111 1111 1111
-1.2 mg	-2 LSB	0x3FFE	XX11 1111 1111 1110
-3.3 g	-5500 LSB	0x2A84	XX10 1010 1000 0100

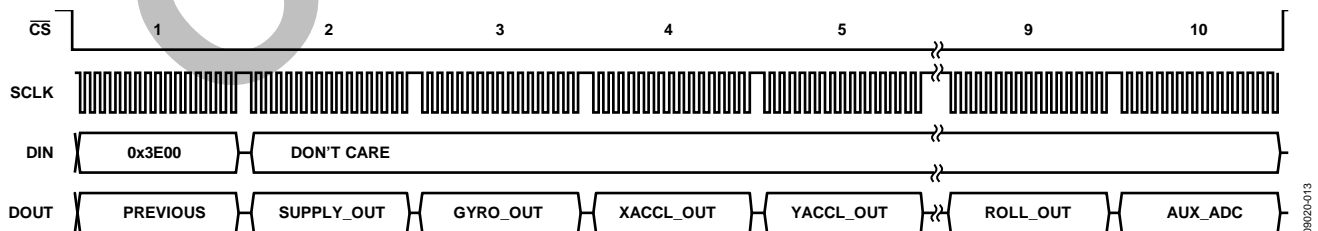


Figure 13. Burst Read Sequence

ORIENTATION ANGLES

The ROLL_OUT and PITCH_OUT registers provide a tilt angle calculation based on the accelerometer measurements. The zero reference is the point at which the z-axis faces gravity for a north-east-down (NED) configuration. Table 12 displays a number of examples for the 13-bit, twos complement digital format in both of these registers. Figure 14 provides the physical references and formulas that produce these orientation angles.

Table 12. Orientation Angles, Twos Complement Format

Angle	Decimal	Hex	Binary
+180°	+4091	0x0FFB	XXX0 1111 1111 1011
+90	+2045	0x07FD	XXX0 0111 1111 1101
+0.088°	+2 LSB	0x0002	XXX0 0000 0000 0010
+0.044°	+1 LSB	0x0001	XXX0 0000 0000 0001
0°	0 LSB	0x0000	XXX0 0000 0000 0000
-0.044°	-1	0x1FFF	XXX1 1111 1111 1111
-0.088°	-2	0x1FFE	XXX1 1111 1111 1110
-90°	-2045	0x1803	XXX1 1000 0000 0011
-179.96°	-4090	0x1006	XXX1 0000 0000 0110

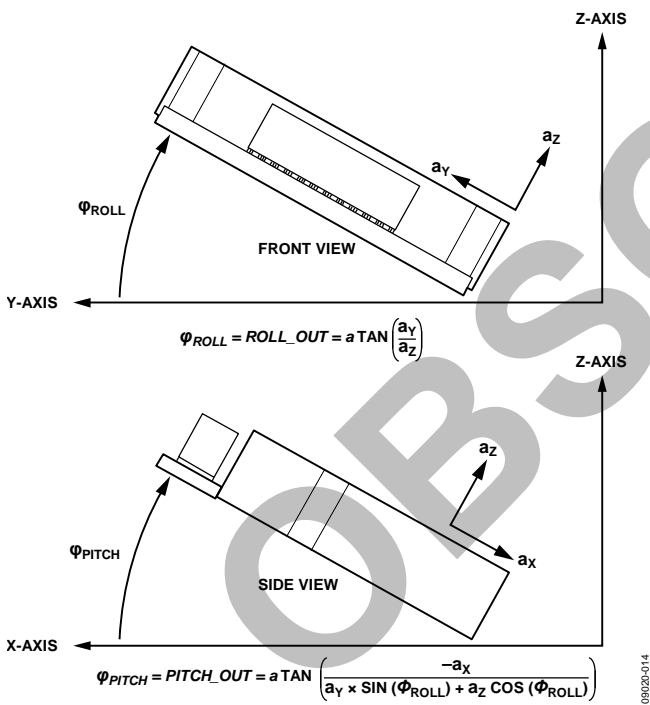


Figure 14. Orientation for PITCH_OUT and ROLL_OUT Angles

Power Supply

The SUPPLY_OUT register provides an internal measurement for the power supply voltage and uses a 12-bit, offset binary digital format. Table 13 provides several numerical examples of this format.

Table 13. Power Supply, Offset Binary Format

Supply Voltage	Decimal	Hex	Binary
5.25 V	2171 LSB	0x87B	XXXX 1000 0111 1011
5.002418 V	2069 LSB	0x815	XXXX 1000 0001 0101
5 V	2068 LSB	0x814	XXXX 1000 0001 0100
4.997582 V	2067 LSB	0x813	XXXX 1000 0001 0011
4.75 V	1964 LSB	0x7AC	XXXX 0111 1010 1100

Internal Temperature

The TEMP_OUT register provides an internal measurement for temperature and uses 12-bit, twos complement for its digital format. Table 14 provides several numerical examples of this format. This is an internal temperature measurement, which can vary from ambient conditions outside of the package.

Table 14. Temperature, Twos Complement Format

Temperature	Decimal	Hex	Binary
+105°C	+588 LSB	0x24C	XXXX 0010 0100 1100
+85°C	+441 LSB	0x1B9	XXXX 0001 1011 1001
+25.272°C	+2 LSB	0x002	XXXX 0000 0000 0010
+25.136°C	+1 LSB	0x001	XXXX 0000 0000 0001
+25°C	0 LSB	0x000	XXXX 0000 0000 0000
+24.864°C	-1 LSB	0xFF	XXXX 1111 1111 1111
+24.728°C	-2 LSB	0xFFE	XXXX 1111 1111 1110
-40°C	-478 LSB	0xE22	XXXX 1110 0010 0010

Analog Input (ADC)

The AUX_ADC register provides access to the auxiliary ADC input channel measurements and uses 12-bit, offset binary as its digital format. The ADC is a 12-bit successive approximation converter that has an input circuit equivalent to the one shown in Figure 15. The maximum input is 3.3 V. The ESD protection diodes can handle 10 mA without causing irreversible damage. The on resistance (R1) of the switch has a typical value of 100 Ω. The sampling capacitor, C2, has a typical value of 16 pF.

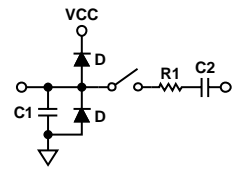


Figure 15. Equivalent Analog Input Circuit (Conversion Phase: Switch Open, Track Phase: Switch Closed)

Table 15. ADC Measurement, Offset Binary Format

Input Voltage	Decimal	Hex	Binary
3.3 V	4095 LSB	0xFFF	XXXX 1111 1111 1111
1 V	1241 LSB	0x4D9	XXXX 0100 1101 1001
1.6118 mV	2 LSB	0x002	XXXX 0000 0000 0010
805.9 μV	1 LSB	0x001	XXXX 0000 0000 0001
0 V	0 LSB	0x000	XXXX 0000 0000 0000

CALIBRATION

Manual Bias Calibration

The bias offset registers in Table 16 and Table 17 provide a manual adjustment function for the output of each sensor. For example, if GYRO_OFF = 0x1FF6 (DIN = 0x9B1F, 0x9AF6), the GYRO_OUT offset shifts by -10 LSBs, or -0.125°/sec.

Table 16. GYRO_OFF Bit Descriptions

Bits	Description (Default = 0x0000)
[15:13]	Not used.
[12:0]	Data bits. Twos complement, 0.0125°/sec per LSB. Typical adjustment range = ±50°/sec.

Table 17. XACCL_OFF, YACCL_OFF, ZACCL_OFF Bit Descriptions

Bits	Description (Default = 0x0000)
[15:12]	Not used.
[11:0]	Data bits. Twos complement, 0.6 mg/LSB. Typical adjustment range = ±1.22 g.

Frame Alignment

The PITCH_OFF and ROLL_OFF registers (see Table 18) provide the angular orientation difference between the inertial frame (internal) and the external frame (package). They follow the same orientation as PITCH_OUT and ROLL_OUT, as shown in Figure 14.

Table 18. PITCH_OFF, ROLL_OFF Bit Descriptions

Bits	Description
[15:10]	Not used.
[9:0]	Data bits. Twos complement, 0.014°/LSB.

Gyroscope Automatic Bias Null Calibration

Set GLOB_CMD[0] = 1 (DIN = 0xBE01) to execute the automatic bias null calibration function. This function measures the gyroscope output register and then loads the gyroscope offset register with the opposite value to provide a quick bias calibration. All sensor data is then reset to 0, and the flash memory is updated automatically within 50 ms (see Table 19).

Gyroscope Precision Automatic Bias Null Calibration

Set GLOB_CMD[4] = 1 (DIN = 0xBE10) to execute the precision automatic bias null calibration function. This function takes the sensor offline for 30 sec while it collects a set of data and calculates more accurate bias correction factors for each gyroscope. After this function is executed, the newly calculated correction factor is loaded into the gyroscope offset registers, all sensor data is reset to 0, and the flash memory is updated automatically within 50 ms (see Table 19).

Restoring Factory Calibration

Set GLOB_CMD[1] = 1 (DIN = 0xBE02) to execute the factory calibration restore function. This function resets each user calibration register to 0x0000 (see Table 16 and Table 17), resets all sensor data to 0, and automatically updates the flash memory within 50 ms (see Table 19).

Linear Acceleration Bias Compensation (Gyroscope)

Set MSC_CTRL[7] = 1 (DIN = 0xB486) to enable correction for low frequency acceleration influences on gyroscope bias. Note that the DIN sequence also preserves the factory default condition for the data-ready function (see Table 24).

OPERATIONAL CONTROL

Global Commands

The GLOB_CMD register provides trigger bits for several useful functions. Setting the assigned bit to 1 starts each operation, which returns the bit to 0 after completion. For example, set GLOB_CMD[7] = 1 (DIN = 0xBE80) to execute a software reset, which stops the sensor operation and runs the device through its start-up sequence. This sequence includes loading the control registers with their respective flash memory locations prior to producing new data. Reading the GLOB_CMD register (DIN = 0x3E00) starts the burst read sequence.

Table 19. GLOB_CMD Bit Descriptions

Bit(s)	Description
[15:8]	Not used
[7]	Software reset command
[6:5]	Not used
[4]	Precision autonull command
[3]	Flash update command
[2]	Auxiliary DAC data latch
[1]	Factory calibration restore command
[0]	Autonull command

Internal Sample Rate

The SMPL_PRD register provides discrete sample rate settings using the bit assignments in Table 20 and the following equation:

$$t_s = t_B \times (N_s + 1)$$

For example, when SMPL_PRD[7:0] = 0x0A, the sample rate is 149 SPS.

Table 20. SMPL_PRD Bit Descriptions

Bit(s)	Description (Default = 0x0001)
[15:8]	Not used
[7]	Time base (t_B) 0 = 0.61035 ms, 1 = 18.921 ms
[6:0]	Increment setting (N_s) Internal sample period = $t_s = t_B \times (N_s + 1)$

The default sample rate setting of 819.2 SPS provides optimal performance. For systems that value slower sample rates, keep the internal sample rate at 819.2 SPS. Use the programmable filter (SENS_AVG) to reduce the bandwidth, which helps to prevent aliasing. The data-ready function (MSC_CTRL) can drive an interrupt routine that uses a counter to help ensure data coherence at reduced rates.

Power Management

Setting $SMPL_PRD \geq 0x0A$ also sets the sensor to low power mode. For systems that require lower power dissipation, in-system characterization helps users to quantify the associated performance trade-offs. In addition to sensor performance, this mode affects SPI data rates (see Table 2). Set $SLP_CNT[8] = 1$ ($DIN = 0xBB01$) to start the indefinite sleep mode, which requires a \overline{CS} assertion (high to low), reset, or power cycle to wake up. Use $SLP_CNT[7:0]$ to put the device into sleep mode for a specified period. For example, $SLP_CNT[7:0] = 0x64$ ($DIN = 0xBA64$) puts the ADIS16305 to sleep for 50 sec.

Table 21. SLP_CNT Bit Descriptions

Bit(s)	Description
[15:9]	Not used
[8]	Indefinite sleep mode; set to 1
[7:0]	Programmable sleep time bits, 0.5 sec/LSB

Sensor Bandwidth

The signal chain for each MEMS sensor has several filter stages, which shape their frequency response. Figure 16 provides a block diagram for both gyroscope and accelerometer signal paths. Table 22 provides additional information for digital filter configuration.

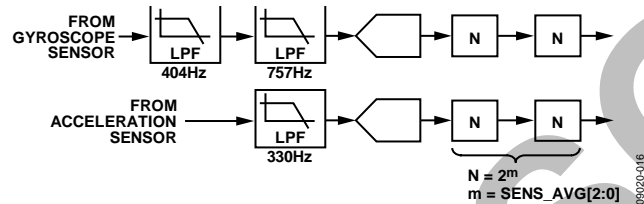


Figure 16. MEMS Analog and Digital Filters

Digital Filtering

The N blocks in Figure 16 are part of the programmable low-pass filter, which provides additional noise reduction on the inertial sensor outputs. This filter contains two cascaded averaging filters that provide a Bartlett window, FIR filter response (see Figure 17). For example, set $SENS_AVG[2:0] = 100$ ($DIN = 0xB804$) to set each stage to 16 taps. When used with the default sample rate of 819.2 SPS, this value reduces the sensor bandwidth to approximately 16 Hz.

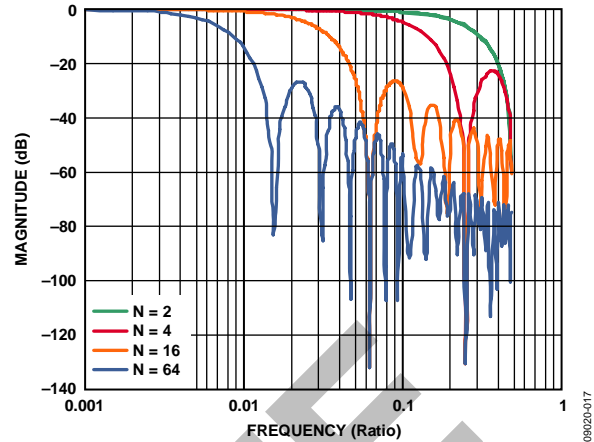


Figure 17. Bartlett Window, FIR Filter Frequency Response (Phase Delay = N Samples)

Dynamic Range

The $SENS_AVG[10:8]$ bits provide three dynamic range settings for this gyroscope. The lower dynamic range settings ($\pm 75^\circ/sec$ and $\pm 150^\circ/sec$) limit the minimum filter tap sizes to maintain resolution. For example, set $SENS_AVG[10:8] = 010$ ($DIN = 0xB902$) for a measurement range of $\pm 150^\circ/sec$. Because this setting can influence the filter settings, program $SENS_AVG[10:8]$ and then $SENS_AVG[2:0]$ if more filtering is required.

Table 22. SENS_AVG Bit Descriptions

Bit(s)	Description
[15:11]	Not used
[10:8]	Measurement range (sensitivity) selection 100 = $\pm 300^\circ/sec$ (default condition) 010 = $\pm 150^\circ/sec$, filter taps ≥ 4 (Bits[2:0] $\geq 0x02$) 001 = $\pm 75^\circ/sec$, filter taps ≥ 16 (Bits[2:0] $\geq 0x04$)
[7:3]	Not used
[2:0]	Number of taps in each stage, $N = 2^m$; maximum setting = 6 (110), $N = 2^6 = 64$ taps/stage

INPUT/OUTPUT FUNCTIONS

General-Purpose I/O

DIO1, DIO2, DIO3, and DIO4 are configurable, general-purpose I/O lines that serve multiple purposes according to the following control register priority: MSC_CTRL, ALM_CTRL, and GPIO_CTRL. For example, set GPIO_CTRL = 0x080C (DIN = 0xB20C, and then 0xB308) to configure DIO1 and DIO2 as inputs and DIO3 and DIO4 as outputs, with DIO3 set low and DIO4 set high.

In this configuration, read GPIO_CTRL (DIN = 0x3200) to monitor the digital state of DIO1 and DIO2.

Table 23. GPIO_CTRL Bit Descriptions

Bit(s)	Description
[15:12]	Not used
[11]	General-Purpose I/O Line 4 (DIO4) data level
[10]	General-Purpose I/O Line 3 (DIO3) data level
[9]	General-Purpose I/O Line 2 (DIO2) data level
[8]	General-Purpose I/O Line 1 (DIO1) data level
[7:4]	Not used
[3]	General-Purpose I/O Line 4 (DIO4) direction control (1 = output, 0 = input)
[2]	General-Purpose I/O Line 3 (DIO3) direction control (1 = output, 0 = input)
[1]	General-Purpose I/O Line 2 (DIO2) direction control (1 = output, 0 = input)
[0]	General-Purpose I/O Line 1 (DIO1) direction control (1 = output, 0 = input)

Input Clock Configuration

The input clock function allows for external control over-sampling in the ADIS16305. Set SMPL_PRD[7:0] = 0x00 (DIN = 0xB600) to enable this function. See Table 2 and Figure 4 for timing information.

Data-Ready I/O Indicator

The factory default sets DIO1 as a positive data-ready indicator signal. The MSC_CTRL[2:0] bits provide configuration options for changing the default. For example, set MSC_CTRL[2:0] = 100 (DIN = 0xB404) to change the polarity of the data-ready signal on DIO1 for interrupt inputs that require negative logic inputs for activation. The pulse width is between 100 μ s and 200 μ s over all conditions.

Table 24. MSC_CTRL Bit Descriptions

Bit(s)	Description
[15:12]	Not used
[11]	Memory test (cleared upon completion) (1 = enabled, 0 = disabled)
[10]	Internal self-test enable (cleared upon completion) (1 = enabled, 0 = disabled)
[9]	Manual self-test, negative stimulus (1 = enabled, 0 = disabled)
[8]	Manual self-test, positive stimulus (1 = enabled, 0 = disabled)
[7]	Linear acceleration bias compensation for gyroscopes (1 = enabled, 0 = disabled)
[6]	Point of percussion alignment, accelerometer (1 = enabled, 0 = disabled)
[5:3]	Not used
[2]	Data ready enable (1 = enabled, 0 = disabled)
[1]	Data ready polarity (1 = active high, 0 = active low)
[0]	Data ready line select (1 = DIO2, 0 = DIO1)

Auxiliary DAC

The 12-bit AUX_DAC line can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches 0 V, the linearity begins to degrade (~100 LSB beginning point). As the sink current increases, the nonlinear range increases. The DAC latch command moves the values of the AUX_DAC register into the DAC input register, enabling both bytes to take effect at the same time.

Table 25. AUX_DAC Bit Descriptions

Bits	Description
[15:12]	Not used
[11:0]	Data bits, scale factor = 0.8059 mV/LSB Offset binary format, 0 V = 0 LSB

Table 26. Setting AUX_DAC = 1 V

DIN	Description
0xB0D9	AUX_DAC[7:0] = 0xD9 (217 LSB).
0xB104	AUX_DAC[15:8] = 0x04 (1024 LSB).
0xBE04	GLOB_CMD[2] = 1. Move values into the DAC input register, resulting in a 1 V output level.

DIAGNOSTICS

Self-Test

The self-test function allows the user to verify the mechanical integrity of each MEMS sensor. It applies an electrostatic force to each sensor element, which results in mechanical displacement that simulates a response to actual motion. Table 1 lists the expected response for each sensor, which provides pass/fail criteria. Set MSC_CTRL[10] = 1 (DIN = 0xB504) to run the internal self-test routine, which exercises all inertial sensors, measures each response, makes pass/fail decisions, and reports them to error flags in the DIAG_STAT register. This process takes 35 ms to complete and report the results to DIAG_STAT[5], DIAG_STAT[10], and DIAG_STAT[15:13]. MSC_CTRL[10] resets itself to 0 after completing the routine. The MSC_CTRL[9:8] bits provide manual control over the self-test function for investigation of potential failures. Table 27 outlines an example test flow for using this option to verify the gyroscope function.

Table 27. Manual Self-Test Example Sequence

DIN	Description
0xB601	SMPL_PRD[7:0] = 0x01, sample rate = 819.2 SPS
0xB904	SENS_AVG[15:8] = 0x04, gyro range = ±300°/sec
0xB802	SENS_AVG[7:0] = 0x02, four-tap averaging filter Delay = 50 ms
0x0400	Read GYRO_OUT
0xB502	MSC_CTRL[9] = 1, gyroscope negative self-test Delay = 50 ms
0x0400	Read GYRO_OUT Determine whether the bias in the gyroscope output changed according to the self-test response specified in Table 1
0xB501	MSC_CTRL[9:8] = 01, gyroscope/accelerometer positive self-test Delay = 50 ms
0x0400	Read GYRO_OUT Determine whether the bias in the gyroscope output changed according to the self-test response specified in Table 1
0xB500	MSC_CTRL[15:8] = 0x00

While the self-test still functions when the device is in motion, zero motion typically produces the most reliable results. The settings in Table 27 are flexible and allow for optimization around speed and noise influence. For example, using fewer filtering taps decreases delay times but increases the possibility of noise influence.

Flash Memory Management

The FLASH_CNT register (see Table 28) provides a tool for managing the flash memory’s endurance. The FLASH_CNT register increments every time there is a write to the flash memory. Figure 18 quantifies the relationship between data retention and junction temperature.

Table 28. FLASH_CNT Bit Descriptions

Bits	Description
[15:0]	Binary counter for writing to flash memory

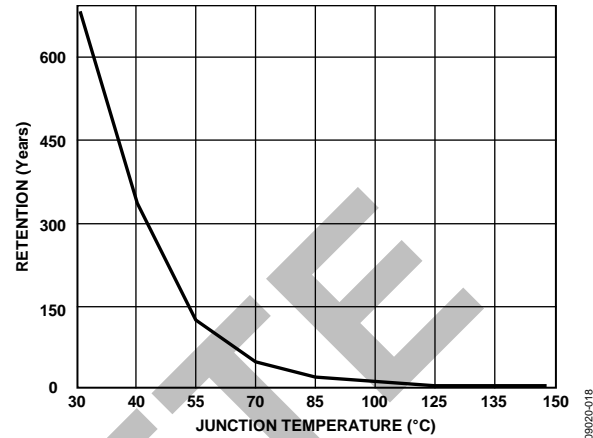


Figure 18. Flash/EE Memory Data Retention

Checksum Test

Set MSC_CTRL[11] = 1 (DIN = 0x9D08) to verify the flash memory integrity against the factory check sum and read DIAG_STAT[6] to check the results 20 ms after the command.

Status

The error flags provide indicator functions for common system level issues. All of the flags are cleared (set to 0) after each DIAG_STAT register read cycle. If an error condition remains, the error flag returns to 1 during the next sample cycle. The DIAG_STAT[1:0] bits do not require a read of this register to return to 0. If the power supply voltage goes back into range, these two flags are cleared automatically.

Table 29. DIAG_STAT Bit Descriptions

Bit(s)	Description
[15]	Z-axis accelerometer self-test failure (1 = fail, 0 = pass)
[14]	Y-axis accelerometer self-test failure (1 = fail, 0 = pass)
[13]	X-axis accelerometer self-test failure (1 = fail, 0 = pass)
[12:11]	Not used
[10]	Gyroscope self-test failure (1 = fail, 0 = pass)
[9]	Alarm 2 status (1 = active, 0 = inactive)
[8]	Alarm 1 status (1 = active, 0 = inactive)
[7]	Not used
[6]	Flash test, checksum flag (1 = fail, 0 = pass)
[5]	Self-test diagnostic error flag (1 = fail, 0 = pass)
[4]	Sensor overrange (1 = fail, 0 = pass)
[3]	SPI communication failure (1 = fail, 0 = pass) ¹
[2]	Flash update failure (1 = fail, 0 = pass)
[1]	Power supply > 5.25 V (1 = power supply > 5.25 V, 0 = power supply ≤ 5.25 V)
[0]	Power supply < 4.75 V (1 = power supply < 4.75 V, 0 = power supply ≥ 4.75 V)

¹ The SPI error flag in DIAG_STAT[3] goes to 1 when the number of SCLKs is not equal to an integer multiple of 16.

Alarm Registers

The alarm function provides monitoring for two independent conditions. The ALM_CTRL register provides control inputs for trigger source, data filtering (prior to comparison), static comparison, dynamic rate-of-change comparison, and output indicator configurations. The ALM_MAGx registers establish the trigger threshold and polarity configurations. Table 33 gives an example of how to configure a static alarm. The ALM_SMPLx registers provide the number of samples to use in the dynamic rate-of-change configuration. The period equals the number in the ALM_SMPLx register multiplied by the sample period time, which is established by the SMPL_PRD register. See Table 34 for an example of how to configure the sensor for this type of function.

Table 30. ALM_MAG1, ALM_MAG2 Bit Descriptions

Bit(s)	Description
[15]	Comparison polarity (1 = greater than, 0 = less than)
[14]	Not used
[13:0]	Data, matches the format of the trigger source

Table 31. ALM_SMPL1, ALM_SMPL2 Bit Descriptions

Bits	Description
[15:8]	Not used
[7:0]	Data bits: number of samples (both 0x00 and 0x01 = 1)

Table 32. ALM_CTRL Bit Designations

Bits	Value	Description
[15:12]		Alarm 2 trigger source selection
	0000	Disable
	0001	Power supply output
	0010	Gyroscope output
	0011	Not used
	0100	Not used
	0101	X-axis accelerometer output
	0110	Y-axis accelerometer output
	0111	Z-axis accelerometer output
	1000	Temperature output
	1001	Pitch angle output
	1010	Roll angle output
	1011	Auxiliary ADC measurement
[11:8]		Alarm 1 trigger source selection (see Bits[15:12])
[7]		Rate of change (ROC) enable for Alarm 2 1 = rate of change, 0 = static level
[6]		Rate of change (ROC) enable for Alarm 1 1 = rate of change, 0 = static level
[5]		Not used
[4]		Comparison data filter setting ¹ 1 = filtered data, 0 = unfiltered data
[3]		Not used
[2]		Alarm output enable (1 = enable, 0 = disable)
[1]		Alarm output polarity (1 = high, 0 = low)
[0]		Alarm output line select (1 = DIO2, 0 = DIO1)

¹ Incline outputs (pitch, roll) always use filtered data in this comparison.

Table 33. Alarm Configuration Example 1

DIN	Description
0xAF55, 0xAE17	ALM_CTRL = 0x5517 Alarm 1 input = XACCL_OUT Alarm 2 input = XACCL_OUT Static level comparison, filtered data DIO2 output indicator, positive polarity
0xA783, 0xA641	ALM_MAG1 = 0x8341 Alarm 1 is true if XACCL_OUT > +0.5 g
0xA93C, 0xA8BF	ALM_MAG2 = 0x3CBF Alarm 2 is true if XACCL_OUT < -0.5 g

Table 34. Alarm Configuration Example 2

DIN	Description
0xAF76, 0xAEC7	ALM_CTRL = 0x76C7 Alarm 1 input = YACCL_OUT Alarm 2 input = ZACCL_OUT Rate-of-change comparison, unfiltered data DIO2 output indicator, positive polarity
0xB601	SMPL_PRD = 0x0001 Sample rate = 819.2 SPS
0xAA08	ALM_SMPL1 = 0x0008 Alarm 1 rate-of-change period = 9.77 ms
0xAC50	ALM_SMPL2 = 0x0050 Alarm 2 rate-of-change period = 97.7 ms
0xA783, 0xA641	ALM_MAG1 = 0x8341 Alarm 1 is true when Δ XACCL_OUT > 0.5 g over a period of 9.77 ms
0xA93C, 0xA8BF	ALM_MAG2 = 0x3CBF Alarm 1 is true when Δ XACCL_OUT < -0.5 g over a period of 97.7 ms

PRODUCT IDENTIFICATION

Table 35 provides a summary of the registers that identify the product: PROD_ID, which identifies the product type; LOT_ID1 and LOT_ID2, the 32-bit lot identification code; and SERIAL_NUM, which displays the 12-bit serial number. All four registers are two bytes in length. When using the SERIAL_NUM value to calculate the serial number, mask off the upper four bits and convert the remaining 12 bits to a decimal number.

Table 35. Identification Registers

Register Name	Address	Description
LOT_ID1	0x52	Lot Identification Code 1
LOT_ID2	0x54	Lot Identification Code 2
PROD_ID	0x56	ADIS16305: 0x3FB1 (16,305)
SERIAL_NUM	0x58	Serial number, 0 to 4095

APPLICATIONS INFORMATION

INTERFACE PRINTED CIRCUIT BOARD (PCB)

The [ADIS16305/PCBZ](#) includes one [ADIS16305ALMZ](#), one interface PCB, and one interface flex. This combination simplifies the process of prototype connections of the [ADIS16305ALMZ](#) with an existing processor system.

J1 and J2 are dual-row, 2 mm (pitch) connectors that work with a number of ribbon cable systems, including 3M Part Number 152212-0100-GB (ribbon crimp connector) and 3M Part Number 3625/12 (ribbon cable). Figure 19 provides a hole pattern design for installing the [ADIS16305/PCBZ](#) so that the flex fits well in between the [ADIS16305ALMZ](#) and the interface PCB. Figure 20 provides the pin assignments for each connector, and the pin descriptions match those listed in Table 5. The [ADIS16305](#) does not require external capacitors for normal operation; therefore, the interface PCB does not use the C1/C2 pads (not shown in Figure 19).

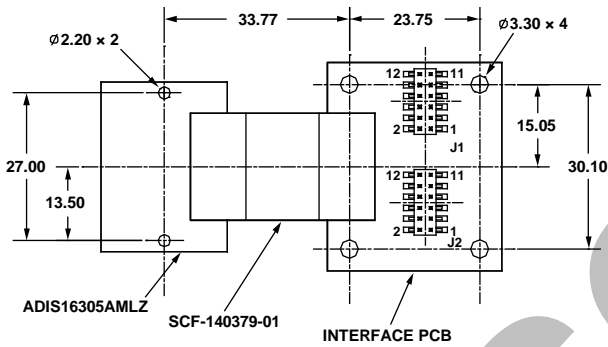


Figure 19. Physical Diagram for Mounting the [ADIS16305/PCBZ](#)

J1		J2			
RST	1	SCLK	AUX_ADC	1	GND
CS	3	DOUT	AUX_DAC	3	DIO3
DNC	5	DIN	GND	5	DIO4
GND	7	GND	DNC	7	DNC
GND	9	VCC	DNC	9	DNC
VCC	11	VCC	DIO2	11	DIO1
	2			2	
	4			4	
	6			6	
	8			8	
	10			10	
	12			12	

Figure 20. J1/J2 Pin Assignments for Interface PCB

GYROSCOPE BIAS OPTIMIZATION

The factory calibration addresses initial bias errors along with temperature-dependent bias behaviors. Installation and certain environmental conditions can introduce modest bias errors. The precision autonull command provides a simple predeployment method for correcting these errors to an accuracy of approximately 0.008°/sec, using an average of 30 sec. Set GLOB_CMD[4] = 1 (DIN = BE10) to start this operation. Averaging the sensor output data for 100 sec can provide incremental performance gains, as well. Controlling device rotation, power supply, and temperature during these averaging times helps to ensure optimal accuracy during this process. Refer to the [AN-1041 Application Note](#) for more information about optimizing performance.

OUTLINE DIMENSIONS

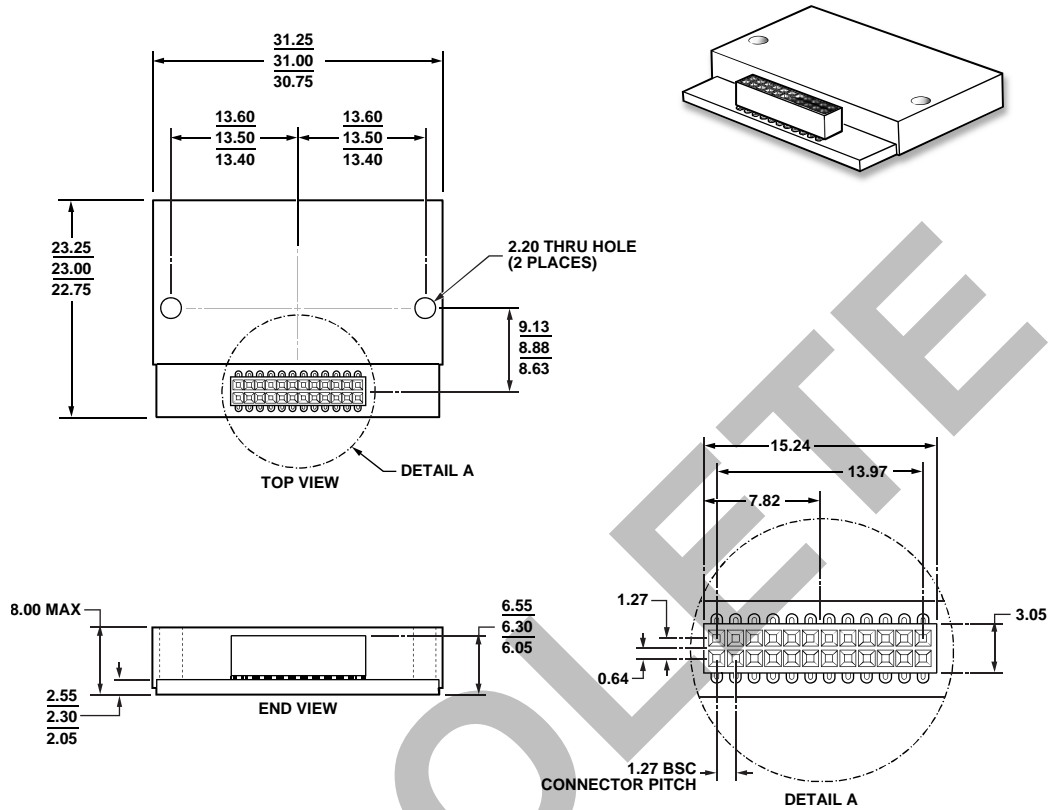


Figure 21. 24-Lead Module with Connector Interface (ML-24-4)
Dimensions shown in millimeters

04-06-2010-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADIS16305AMLZ	-40°C to +85°C	24-Lead Module with Connector Interface	ML-24-4
ADIS16305/PCBZ		Interface Board	

¹ Z = RoHS Compliant Part.

NOTES

OBSOLETE