ADC Architectures III: Sigma-Delta ADC Basics

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INTRODUCTION

The sigma-delta (Σ-Δ) ADC is the converter of choice for modern voiceband, audio, and high-resolution precision industrial measurement applications. The highly digital architecture is ideally suited for modern fine-line CMOS processes, thereby allowing easy addition of digital functionality without significantly increasing the cost. Because of its widespread use, it is important to understand the fundamental principles behind this converter architecture.

Due to the length of the topic, the discussion of Σ-Δ ADCs requires two tutorials, MT-022 and MT-023. This first tutorial (MT-022) first discusses the history of Σ-Δ and the fundamental concepts of oversampling, quantization noise shaping, digital filtering, and decimation. Tutorial MT-023 discusses more advanced topics related to Σ-Δ, including idle tones, multi-bit Σ-Δ ADCs, multistage noise shaping Σ-Δ ADCs (MASH), bandpass Σ-Δ ADCs, as well as some example applications.

HISTORICAL PERSPECTIVE

The Σ-Δ ADC architecture had its origins in the early development phases of pulse code modulation (PCM) systems—specifically, those related to transmission techniques called *delta modulation* and *differential PCM*. (An excellent discussion of both the history and concepts of the Σ-Δ ADC can be found by Max Hauser in Reference 1). Delta modulation was first invented at the ITT Laboratories in France by E. M. Deloraine, S. Van Mierlo, and B. Derjavitch in 1946 (References 2, 3).

The principle was "rediscovered" several years later at the Phillips Laboratories in Holland, whose engineers published the first extensive studies both of the single-bit and multi-bit concepts in 1952 and 1953 (References 4, 5). In 1950, C. C. Cutler of Bell Telephone Labs in the U.S. filed an important patent on differential PCM which covered the same essential concepts (Reference 6).

The driving force behind delta modulation and differential PCM was to achieve higher transmission efficiency by transmitting the *changes* (delta) in value between consecutive samples rather than the actual samples themselves.

In *delta modulation*, the analog signal is quantized by a one-bit ADC (a comparator) as shown in Figure 1A. The comparator output is converted back to an analog signal with a 1-bit DAC, and subtracted from the input after passing through an integrator. The shape of the analog signal is transmitted as follows: a "1" indicates that a positive excursion has occurred since the last sample, and a "0" indicates that a negative excursion has occurred since the last sample.
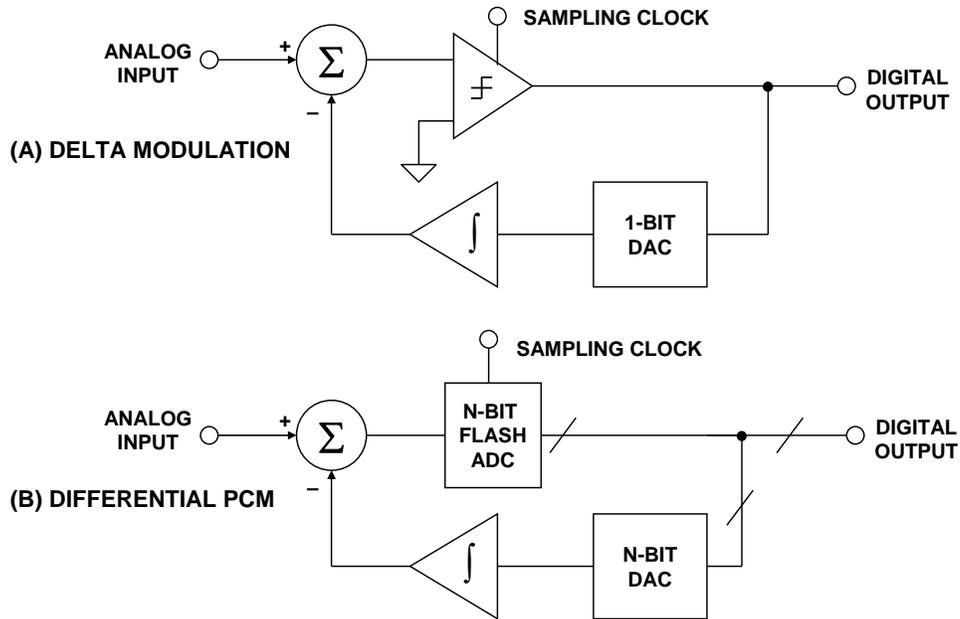
Figure 1: Delta Modulation and Differential PCM

If the analog signal remains at a fixed dc level for a period of time, an alternating pattern of "0s" and "1s" is obtained. It should be noted that *differential PCM* (see Figure 1B) uses exactly the same concept except a multibit ADC is used rather than a single comparator to derive the transmitted information.

Since there is no limit to the number of pulses of the same sign that may occur, delta modulation systems are capable of tracking signals of any amplitude. In theory, there is no peak clipping. However, the theoretical limitation of delta modulation is that the analog signal must not change too rapidly. The problem of slope clipping is shown in Figure 2. Here, although each sampling instant indicates a positive excursion, the analog signal is rising too quickly, and the quantizer is unable to keep pace.
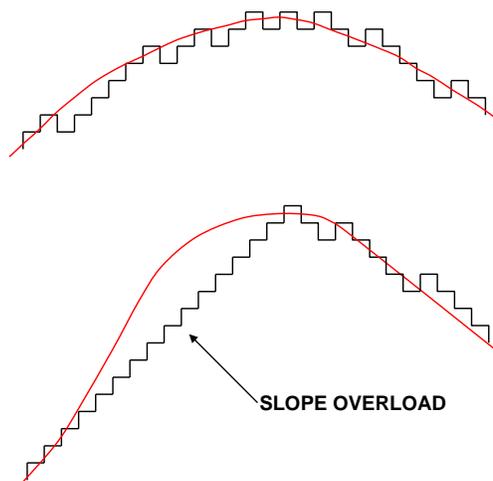

Figure 2: Quantization Using Delta Modulation

Slope clipping can be reduced by increasing the quantum step size or increasing the sampling rate. Differential PCM uses a multibit quantizer to effectively increase the quantum step sizes at the increase of complexity. Tests have shown that in order to obtain the same quality as classical PCM, delta modulation requires very high sampling rates, typically 20× the highest frequency of interest, as opposed to Nyquist rate of 2×.

For these reasons, delta modulation and differential PCM have never achieved any significant degree of popularity, however a slight modification of the delta modulator leads to the basic Σ-Δ architecture, one of the most popular ADC architectures in use today.

In 1954 C. C. Cutler of Bell Labs filed a very significant patent which introduced the principle of *oversampling* and *noise shaping* with the specific intent of achieving higher resolution (Reference 7). His objective was not specifically to design a Nyquist ADC, but to transmit the oversampled noise-shaped signal without reducing the data rate. Thus Cutler's converter embodied all the concepts in a Σ-Δ ADC with the exception of *digital filtering* and *decimation* which would have been too complex and costly at the time using vacuum tube technology.

Occasional work continued on these concepts over the next several years, including an important patent of C. B. Brahm filed in 1961 which gave details of the analog design of the loop filter for a second-order multibit noise shaping ADC (Reference 8). Transistor circuits began to replace vacuum tubes over the period, and this opened up many more possibilities for implementation of the architecture.

In 1962, Inose, Yasuda, and Murakami elaborated on the single-bit oversampling noise-shaping architecture proposed by Cutler in 1954 (Reference 9). Their experimental circuits used solid state devices to implement first and second-order Σ-Δ modulators. The 1962 paper was followed by a second paper in 1963 which gave excellent theoretical discussions on oversampling and noise-shaping (Reference 10). These two papers were also the first to use the name *delta-sigma* to describe the architecture. The name *delta-sigma* stuck until the 1970s when AT&T engineers began using name *sigma-delta*. Since that time, both names have been used; however, sigma-delta may be the more correct of the two.

It is interesting to note that all the work described thus far was related to transmitting an oversampled digitized signal directly rather than the implementation of a Nyquist ADC. In 1969 D. J. Goodman at Bell Labs published a paper describing a true Nyquist Σ-Δ ADC with a digital filter and a decimator following the modulator (Reference 11). This was the first use of the Σ-Δ architecture for the explicit purpose of producing a Nyquist ADC. In 1974 J. C. Candy, also of Bell Labs, described a multibit oversampling Σ-Δ ADC with noise shaping, digital filtering, and decimation to achieve a high resolution Nyquist ADC (Reference 12).

The IC Σ-Δ ADC offers several advantages over the other architectures, especially for high resolution, low frequency applications. First and foremost, the single-bit Σ-Δ ADC is inherently monotonic and requires no laser trimming. The Σ-Δ ADC also lends itself to low cost foundry CMOS processes because of the digitally intensive nature of the architecture. Examples of early monolithic Σ-Δ ADCs are given in References 13-21. Since that time there have been a constant

stream of process and design improvements in the fundamental architecture proposed in the early works cited above.

Modern CMOS Σ-Δ ADCs (and DACs, for that matter) are the converters of choice for voiceband and audio applications. The highly digital architectures lend themselves nicely to fine-line CMOS. In addition, high resolution (up to 24 bits) low frequency Σ-Δ ADCs have virtually replaced the older integrating converters in precision industrial measurement applications.

BASICS OF Σ-Δ ADCS

There have been innumerable descriptions of the architecture and theory of Σ-Δ ADCs, but most commence with a maze of integrals and deteriorate from there. Some engineers who do not understand the theory of operation of Σ-Δ ADCs are convinced, from study of a typical published article, that it is too complex to comprehend easily.

There is nothing particularly difficult to understand about Σ-Δ ADCs, as long as you avoid the detailed mathematics, and this section has been written in an attempt to clarify the subject. A Σ-Δ ADC contains very simple analog electronics (a comparator, voltage reference, a switch, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. This digital circuitry consists of a digital signal processor (DSP) which acts as a filter (generally, but not invariably, a low pass filter). It is not necessary to know precisely how the filter works to appreciate what it does. To understand how a Σ-Δ ADC works, familiarity with the concepts of *oversampling, quantization noise shaping, digital filtering,* and *decimation* is required.

Let us consider the technique of oversampling with an analysis in the frequency domain. Where a dc conversion has a *quantization error* of up to ½ LSB, a sampled data system has *quantization noise*. A perfect classical N-bit sampling ADC has an rms quantization noise of $q/\sqrt{12}$ uniformly distributed within the Nyquist band of dc to $f_s/2$ (where q is the value of an LSB and f_s is the sampling rate) as shown in Figure 3A. Therefore, its SNR with a full-scale sinewave input will be $(6.02N + 1.76)$ dB. (Refer to Tutorial MT-001 for the derivation). If the ADC is less than perfect, and its noise is greater than its theoretical minimum quantization noise, then its *effective* resolution will be less than N-bits. Its actual resolution (often known as its Effective Number of Bits or ENOB) will be defined by

$$\text{ENOB} = \frac{\text{SNR} - 1.76\text{dB}}{6.02\text{dB}}.$$
Eq. 1

If we choose a much higher sampling rate, Kf_s (see Figure 3B), the rms quantization noise remains $q/\sqrt{12}$, but the noise is now distributed over a wider bandwidth dc to $Kf_s/2$. If we then apply a digital low pass filter (LPF) to the output, we remove much of the quantization noise, but do not affect the wanted signal—so the ENOB is improved. We have accomplished a high resolution A/D conversion with a low resolution ADC. The factor K is generally referred to as the *oversampling ratio*. It should be noted at this point that oversampling has an added benefit in that it relaxes the requirements on the analog antialiasing filter. This is a big advantage of Σ-Δ,

especially in consumer audio applications where the cost of a sharp cutoff linear phase filter can be significant.
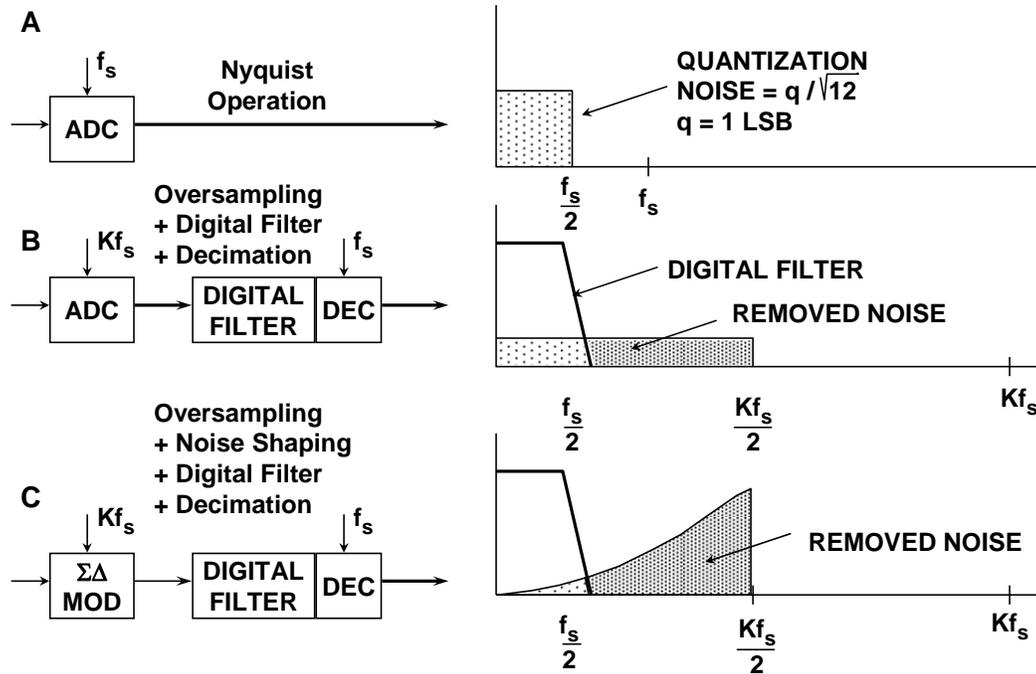

Figure 3: Oversampling, Digital Filtering, Noise Shaping, and Decimation

Since the bandwidth is reduced by the digital output filter, the output data rate may be lower than the original sampling rate (Kf_s) and still satisfy the Nyquist criterion. This may be achieved by passing every Mth result to the output and discarding the remainder. The process is known as "decimation" by a factor of M. Despite the origins of the term (*decem* is Latin for ten), M can have any integer value, provided that the output data rate is more than twice the signal bandwidth. Decimation does not cause any loss of information (see Figure 3B).

If we simply use oversampling to improve resolution, we must oversample by a factor of 2^{2N} to obtain an N-bit increase in resolution. The Σ-Δ converter does not need such a high oversampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband as shown in Figure 3C.

If we take a 1-bit ADC (a comparator), drive it with the output of an integrator, and feed the integrator with an input signal summed with the output of a 1-bit DAC fed from the ADC output, we have a first-order Σ-Δ modulator as shown in Figure 4. Add a digital low pass filter (LPF) and decimator at the digital output, and we have a Σ-Δ ADC—the Σ-Δ modulator shapes the quantization noise so that it lies above the passband of the digital output filter, and the ENOB is therefore much larger than would otherwise be expected from the oversampling ratio.
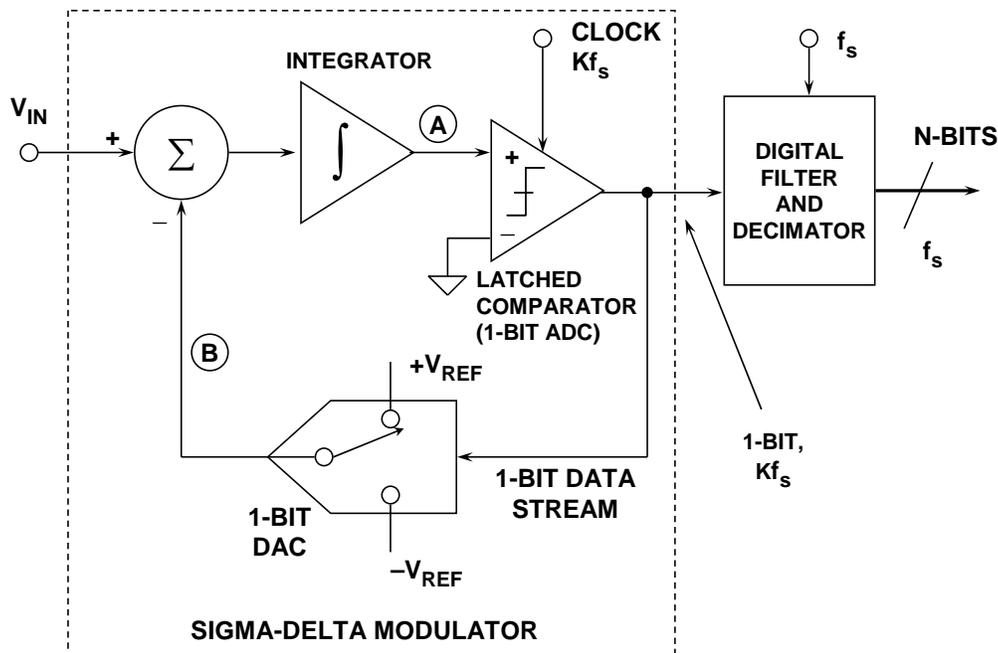
Figure 4: First-Order Sigma-Delta ADC

Intuitively, a Σ-Δ ADC operates as follows. Assume a dc input at V_{IN}. The integrator is constantly ramping up or down at node A. The output of the comparator is fed back through a 1-bit DAC to the summing input at node B. The negative feedback loop from the comparator output through the 1-bit DAC back to the summing point will force the average dc voltage at node B to be equal to V_{IN}. This implies that the average DAC output voltage must equal the input voltage V_{IN}. The average DAC output voltage is controlled by the *ones-density* in the 1-bit data stream from the comparator output. As the input signal increases towards $+V_{REF}$, the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. Similarly, as the signal goes negative towards $-V_{REF}$, the number of "ones" in the serial bit stream decreases, and the number of "zeros" increases. From a very simplistic standpoint, this analysis shows that the average value of the input voltage is contained in the serial bit stream out of the comparator. The digital filter and decimator process the serial bit stream and produce the final output data.

For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged, will a meaningful value result. The Σ-Δ modulator is very difficult to analyze in the time domain because of this apparent randomness of the single-bit data output. If the input signal is near positive full-scale, it is clear that there will be more "1"s than "0"s in the bit stream. Likewise, for signals near negative full-scale, there will be more "0"s than "1"s in the bit stream. For signals near midscale, there will be approximately an equal number of "1"s and "0"s. Figure 5 shows the output of the integrator for two input conditions. The first is for an input of zero (midscale). To decode the output, pass the output samples through a simple digital lowpass filter that averages every four samples. The output of the filter is 2/4. This value represents bipolar zero. If more samples are averaged, more dynamic range is achieved. For example, averaging 4 samples gives 2 bits of resolution,

while averaging 8 samples yields 4/8, or 3 bits of resolution. In the bottom waveform of Figure 5, the average obtained for 4 samples is 3/4, and the average for 8 samples is 6/8.
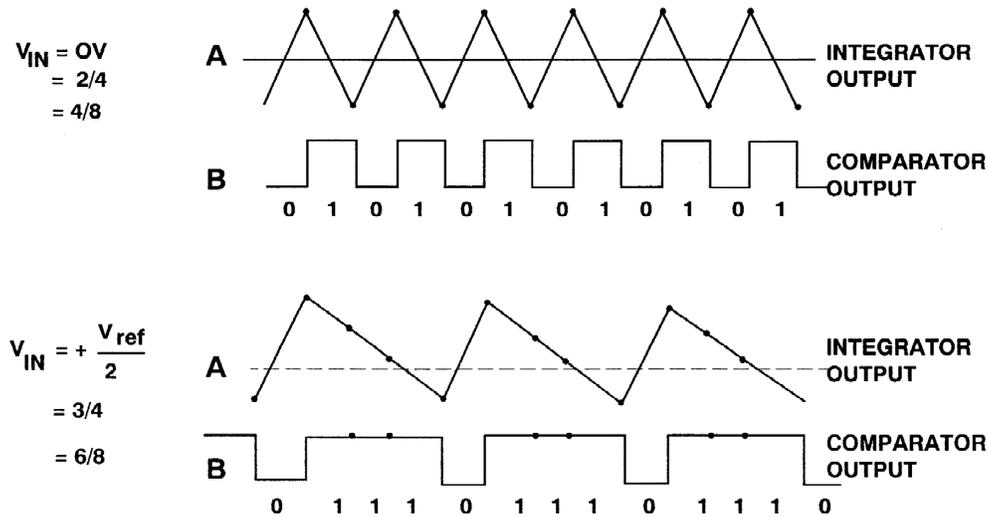

$V_{IN} = OV$
$= 2/4$
$= 4/8$

A — INTEGRATOR OUTPUT

B — COMPARATOR OUTPUT

0 1 0 1 0 1 0 1 0 1 0 1

$V_{IN} = + \dfrac{V_{ref}}{2}$
$= 3/4$
$= 6/8$

A — INTEGRATOR OUTPUT

B — COMPARATOR OUTPUT

0 1 1 1 0 1 1 1 0 1 1 1 0

**Figure 5: Sigma-Delta Modulator Waveforms**

For an interactive tutorial on the time domain characteristics of the Σ-Δ modulator, refer to the Sigma-Delta Tutorial located in the Analog Devices' Design Center which gives a graphical illustration of the behavior of an idealized Σ-Δ ADC.

The Σ-Δ ADC can also be viewed as a synchronous voltage-to-frequency converter followed by a counter. If the number of "1"s in the output data stream is counted over a sufficient number of samples, the counter output will represent the digital value of the input. Obviously, this method of averaging will only work for dc or very slowly changing input signals. In addition, 2^N clock cycles must be counted in order to achieve N-bit effective resolution, thereby severely limiting the effective sampling rate.

It should be noted that because the digital filter is an integral part of the Σ-Δ ADC, there is a built-in "pipeline" delay (sometimes called "latency") primarily determined by the number of taps in the digital filter. Digital filters in Σ-Δ ADCs can be quite large (several hundred taps), so the latency may become an issue in multiplexed applications where the appropriate amount of settling time must be allowed after switching channels.

FREQUENCY DOMAIN ANALYSIS OF A SIGMA-DELTA ADC AND NOISE SHAPING

Further time-domain analysis is not productive, and the concept of noise shaping is best explained in the frequency domain by considering the simple Σ-Δ modulator model in Figure 6.

1 (X – Y)

Q =
QUANTIZATION
NOISE

X – Y

X

Σ

+

– Y

ANALOG FILTER
H(f) = **1**
f

Σ

Y
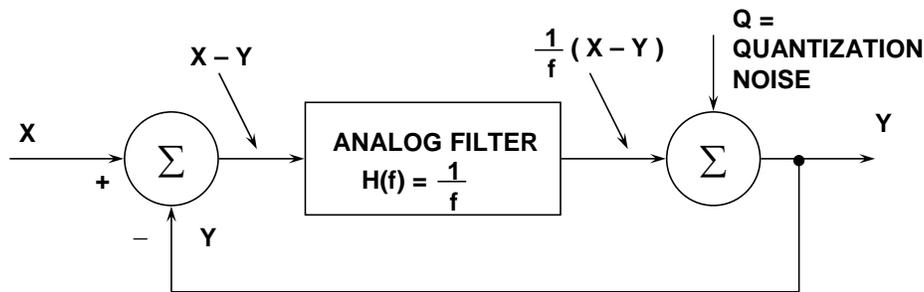
$Y = \frac{1}{f}(X - Y) + Q$

REARRANGING, SOLVING FOR Y:

$Y = \frac{X}{f+1} + \frac{Qf}{f+1}$

SIGNAL TERM   **NOISE TERM**

Figure 6: Simplified Frequency Domain Linearized Model
of a Sigma-Delta Modulator

The integrator in the modulator is represented as an analog lowpass filter with a transfer function equal to $H(f) = 1/f$. This transfer function has an amplitude response which is inversely proportional to the input frequency. The 1-bit quantizer generates quantization noise, Q, which is injected into the output summing block. If we let the input signal be X, and the output Y, the signal coming out of the input summer must be $X - Y$. This is multiplied by the filter transfer function, $1/f$, and the result goes to one input of the output summer. By inspection, we can then write the expression for the output voltage Y as:

$$Y = \frac{1}{f}(X - Y) + Q . \qquad \text{Eq. 2}$$

This expression can easily be rearranged and solved for Y in terms of X, f, and Q:

$$Y = \frac{X}{f+1} + \frac{Q \cdot f}{f+1} . \qquad \text{Eq. 3}$$

Note that as the frequency f approaches zero, the output voltage Y approaches X with no noise component. At higher frequencies, the amplitude of the signal component approaches zero, and the noise component approaches Q. At high frequency, the output consists primarily of quantization noise. In essence, the analog filter has a lowpass effect on the signal, and a highpass effect on the quantization noise. Thus the analog filter performs the noise shaping function in the Σ-Δ modulator model. For a given input frequency, higher order analog filters offer more attenuation. The same is true of Σ-Δ modulators, provided certain precautions are taken.

By using more than one integration and summing stage in the Σ-Δ modulator, we can achieve higher orders of quantization noise shaping and even better ENOB for a given oversampling ratio as is shown in Figure 7 for both a first and second-order Σ-Δ modulator.
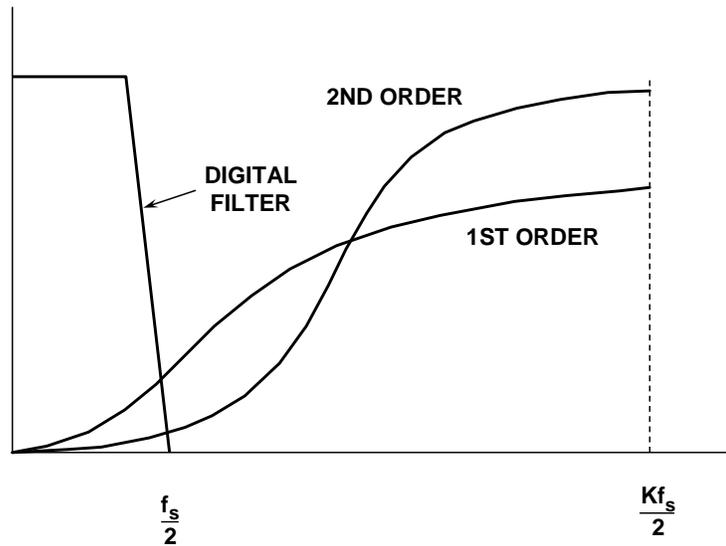

Figure 7: Sigma-Delta Modulators Shape Quantization Noise

The block diagram for the second-order Σ-Δ modulator is shown in Figure 8. Third, and higher, order Σ-Δ ADCs were once thought to be potentially unstable at some values of input—recent analyses using *finite* rather than infinite gains in the comparator have shown that this is not necessarily so, but even if instability does start to occur, the DSP in the digital filter and decimator can be made to recognize incipient instability and react to prevent it.
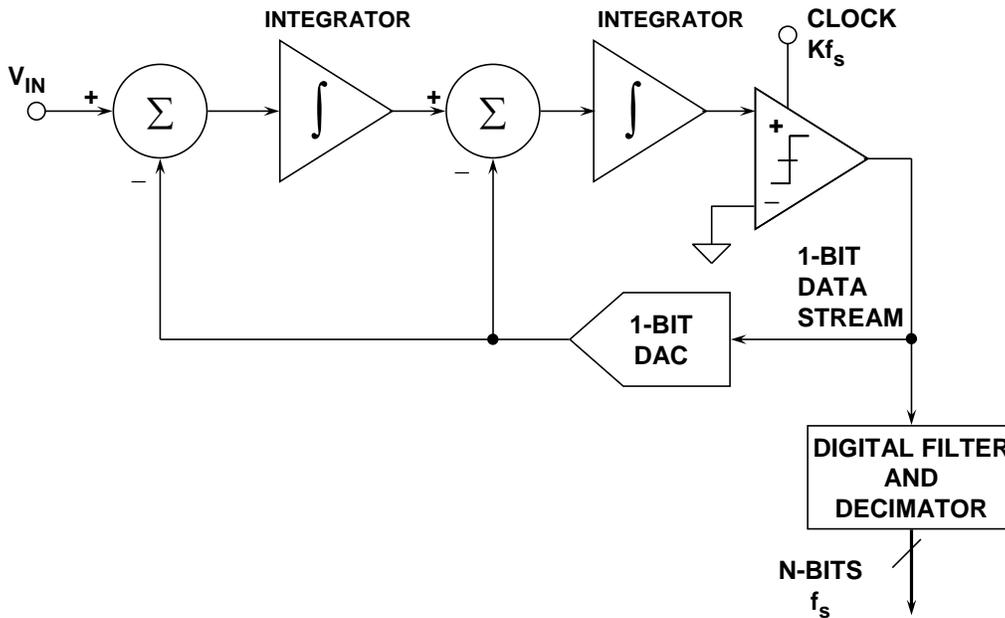

Figure 8: Second-Order Sigma-Delta ADC

Figure 9 shows the relationship between the order of the Σ-Δ modulator and the amount of oversampling necessary to achieve a particular SNR. For instance, if the oversampling ratio is 64, an ideal second-order system is capable of providing an SNR of about 80 dB. This implies approximately 13 effective number of bits (ENOB). Although the filtering done by the digital filter and decimator can be done to any degree of precision desirable, it would be pointless to carry more than 13 binary bits to the outside world. Additional bits would carry no useful signal information, and would be buried in the quantization noise unless post-filtering techniques were employed. Additional resolution can be obtained from the 1-bit system by increasing the oversampling ratio and/or by using a higher-order modulator. Other methods are often used to achieve higher resolution, such as the multi-bit Σ-Δ architecture, and are discussed in Tutorial MT-023.
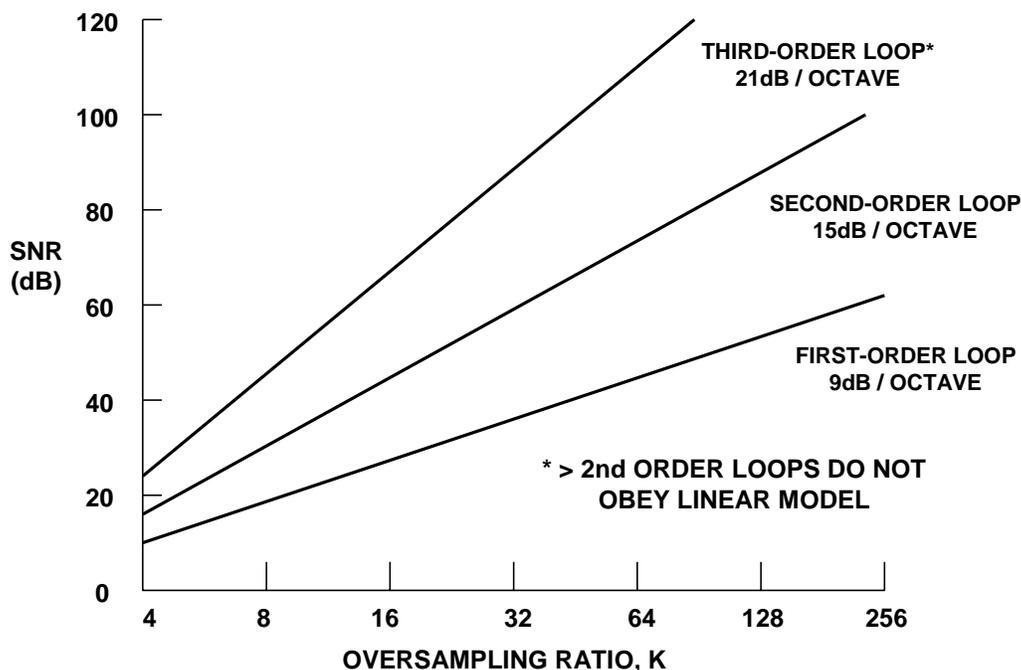

*Figure 9: SNR Versus Oversampling Ratio for
First, Second, and Third-Order Loops*

SUMMARY

This tutorial has covered the basics of Σ-Δ ADCs from a historical perspective including the important concepts of oversampling, digital Filtering, noise shaping, and decimation. Tutorial MT-023 covers some of the more advanced concepts and applications of Σ-Δ ADCs, such as idle tones, multi-bit Σ-Δ, MASH, and bandpass Σ-Δ.

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