

System Development Platform User Guide

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Regulatory Compliance

The EVAL-SDP-CB1Z is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The EVAL-SDP-CB1Z board has been certified to comply with the essential requirements of the European EMC directive 89/36/EC amended by 93/68/EEC and therefore carries the “CE” mark.



The EVAL-SDP-CB1Z board evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EVAL-SDP-CB1Z boards in the protective shipping package.



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PREFACE

Thank you for purchasing the EVAL-SDP-CB1Z System Development Platform (SDP) from Analog Devices, Inc. The SDP is used as part of the evaluation system for many ADI components.

The SDP board is designed to be used in conjunction with various ADI component evaluation boards as part of a customer evaluation environment. The SDP provides USB connectivity through a USB 2.0 high speed connection to the computer allowing users to evaluate components on this platform from a PC application. The SDP is based on ADSP-BF527 Blackfin processor, with the Blackfin processor peripheral communication lines available to the component daughter board through the two identical 120-pin small footprint connectors

Product Overview

The board features:

- Analog Devices ADSP-BF527 Blackfin processor
 - Core performance up to 600 MHz
 - 208 -ball CSP-BGA package
 - 24 MHz CLKIN oscillator
 - 5 Mb of internal RAM memory

Purpose of This Manual

- 32Mb flash memory
 - Numonyx M29W320EB or
 - Numonyx M25P32
- SDRAM memory
 - Micron MT48LC16M16A2P-6A - 16 Mb x 16 bits (256 Mb/32 MB)
- 2 x 120-pin small foot print connectors
 - Hirose FX8 -120P-SV1(91),120 Pin Header
- Blackfin processor peripherals exposed
 - SPI
 - SPORT
 - TWI/I²C
 - GPIO
 - PPI
 - Asynchronous Parallel

For more information, go to <http://www.analog.com/sdp>.

Purpose of This Manual

The *SDP User Guide* provides instructions for installing the SDP hardware (EVAL-SDP-CB1Z board) and software onto your computer. The necessary installation files are provided with the evaluation daughter board package.

Intended Audience

The primary audience for this manual is a system engineer who seeks to understand how to set up the SDP board and begin USB communications to the computer.

Manual Contents

The manual consists of:

- Chapter 1, “[Getting Started](#)” on page 1-1
Provides software and hardware installation procedure, PC system requirements and basic board information.
- Chapter 2, “[Hardware Description](#)” on page 2-1
Provides information on the EVAL-SDP-CB1Z components.
- Chapter 3, “[Schematic](#)” on page 3-1
Provides EVAL-SDP-CB1Z schematics.

What’s New in This Manual

Revision 1.2 of the SDP User Guide adds the following:

- Corrected the pin names for pin 21 ($\overline{\text{PAR_RD}}$) and pin 22 ($\overline{\text{PAR_CS}}$) in the table describing the 120 pin connector. In [Table 2-1 on page 2-3](#) of the revision 1.1 book, the pin names were swapped, but the pin descriptions were correct. The pin assignments in [Figure 2-1 on page 2-3](#) following the table of the revision 1.1 book were correct.

Technical or Customer Support

You can reach Analog Devices, Inc. Customer Support in the following ways:

- Visit the SDP Web site at
<http://www.analog.com/sdp>
- E-mail processor questions to
processor.support@analog.com (World wide support)
processor.europe@analog.com (Europe support)
processor.china@analog.com (China support)
- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
USA

Product Information

Product information can be obtained from the Analog Devices Web site.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analogue integrated circuits, amplifiers, converters, and digital signal processors.

Also note, MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.




Visit MyAnalog.com to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (File menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the Close command appears on the File menu).
{this that}	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as <i>this</i> or <i>that</i> . One or the other is required.
[this that]	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional <i>this</i> or <i>that</i> .
[this,...]	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipsis; read the example as an optional comma-separated list of <i>this</i> .
.SECTION	Commands, directives, keywords, and feature names are in text with letter gothic font.
<i>filename</i>	Non-keyword placeholders appear in text with italic style format.

Notation Conventions

Example	Description
	<p>Note: For correct operation, ...</p> <p>A Note provides supplementary information on a related topic. In the online version of this book, the word Note appears instead of this symbol.</p>
	<p>Caution: Incorrect device operation may result if ...</p> <p>Caution: Device damage may result if ...</p> <p>A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word Caution appears instead of this symbol.</p>
	<p>Warning: Injury to device users may result if ...</p> <p>A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word Warning appears instead of this symbol.</p>

1 GETTING STARTED

This chapter provides specific information to assist you with using the SDP board as part of your evaluation system.

The following topics are covered.

- [“Package Contents”](#)
- [“PC Configuration”](#)
- [“USB Installation”](#)
- [“Powering Up/Down the SDP”](#)

Package Contents

Your EVAL-SDP-CB1Z board package contains the following items.

- EVAL-SDP-CB1Z board
- 1m USB Standard-A to mini-B cable

Contact the vendor where you purchased your SDP board or contact Analog Devices, Inc. if any item is missing.

PC Configuration

For correct operation of the SDP board, your computer must have the following minimum configuration

- Windows XP Service Pack 2 or Windows Vista
- USB 2.0 port

The SDP board evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused SDP boards in the protective shipping package.



When removing the SDP board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components.

USB Installation

Perform the following tasks to safely install the SDP board onto the computer.

There are two stages in the software application installation procedure. The first installs the application software. The second installs the .NET Framework 3.5 and the necessary drivers.

Installing the Software

1. Run the application install provided. The first stage will install the Applications GUI and necessary support files onto the computer
2. Immediately following the application install, the .NET Framework 3.5 and the driver package for the SDP board is installed. If the .NET Framework 3.5 is already pre-installed on the computer in question, this stage will be skipped and step two will consist of a driver package installation only

Connecting the SDP Board to the PC

- Attach the SDP board to a USB 2.0 port on the computer via the Standard-A to Mini-B cable provided.

Verifying Driver Installation

Before using the SDP board, verify the driver software has installed properly.

- Open the Windows Device Manager and verify the SDP board appears under ADI Development Tools as shown in [Figure 1-1](#).

USB Installation

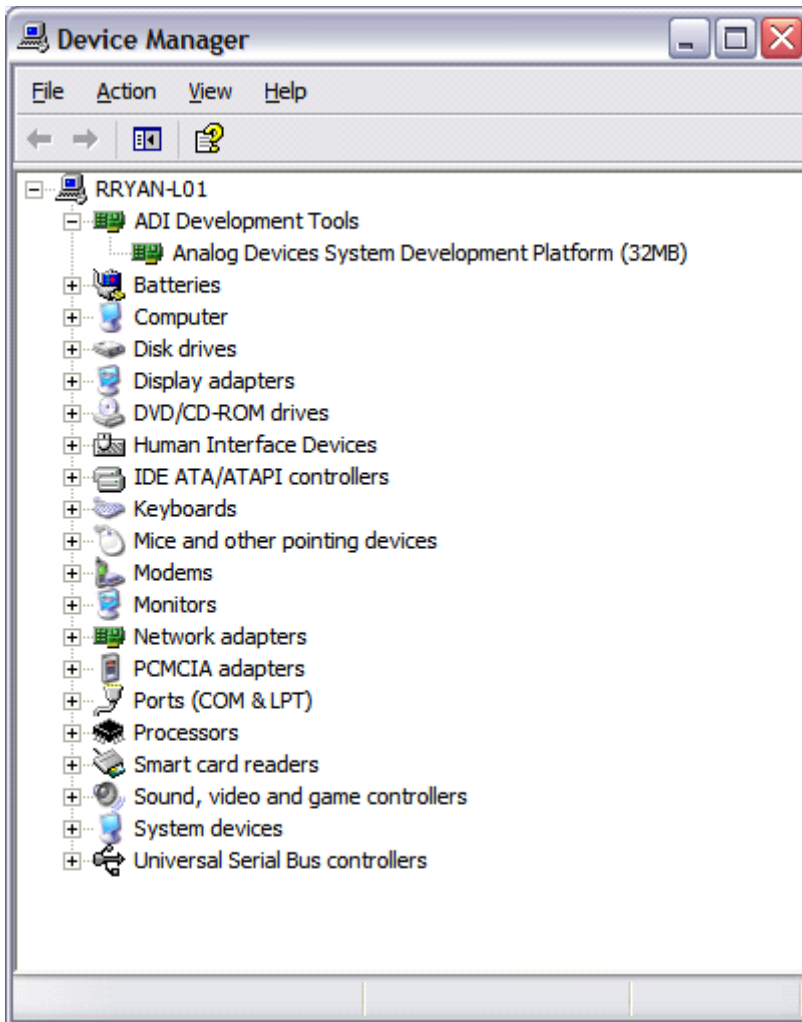


Figure 1-1. Device Manager

Powering Up/Down the SDP

The following sections describe how to safely power up and down the SDP.

Powering Up the SDP Board

1. Connect the SDP board to the daughter evaluation board through the 120 pin mating connectors.
2. Power the daughter board
3. Connect the USB port on the computer to the SDP board.

Powering Down the SDP Board

1. Power down the daughter evaluation board
2. Disconnect the USB port on the computer from the SDP board
3. Disconnect the SDP board from the daughter evaluation board

Powering Up/Down the SDP

2 HARDWARE DESCRIPTION

This chapter describes the hardware design of the EVAL- SDP -CB1Z board.

The following topics are covered.

- “[LEDs](#)” — Describes the SDP on board LEDs.
- “[Connector Details](#)” — Details the pin assignments on the 120 pin Connectors
- “[Power](#)” — Lists power requirements of the SDP and identifies connector power inputs and output pins
- “[Daughter Board Design Guidelines](#)” — Provides guidelines regarding how to design daughter boards for use with the SDP
- “[Mechanical Specifications](#)” — Provides dimensional information

LEDs

There are two LEDs located on the SDP board. Refer to [Figure 2-1](#).

POWER LED (LED2)

The green power LED indicates that the SDP board is powered. This is not an indication of USB connectivity between the SDP and the PC.

Connector Details

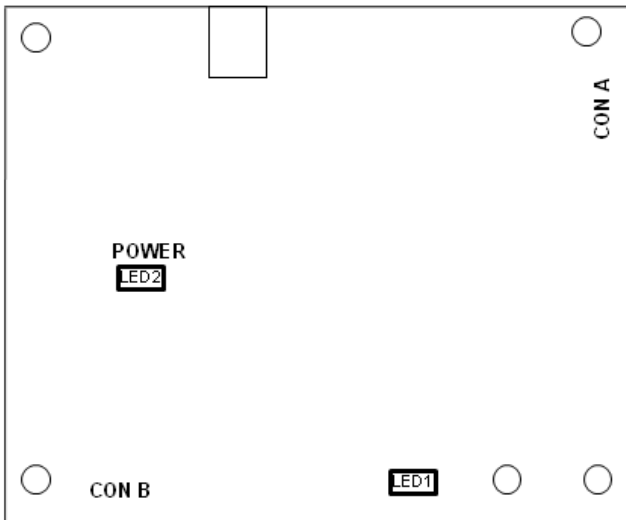


Figure 2-1. SDP Board LEDs

LED 1

The orange LED is an LED to be used as a diagnostic tool for evaluation application developers.

Connector Details

The SDP board contains two identical Hirose FX8-120P-SV1(91), 120 pin header, connectors. Through these connectors, the peripheral communication interfaces of ADSP-BF527 Blackfin processor are exposed. The exposed peripherals are:

- SPI
- SPORT
- I²C/TWI

- GPIO
- Asynchronous Parallel
- PPI
- UART
- Timers

Also, included on the connector specification are input and output power pins, ground pins, and pins reserved for future use.

For further details on the peripheral interfaces, including timing diagrams, see the *ADSP-BF52x Blackfin Processor Hardware Reference*.

Connector Pin Assignments

The connector pin assignments have been defined independently of the any internal pin sharing, which occurs on the Blackfin processor. [Table 2-1](#) lists the connector pins and identifies the functionality assigned to each connector pin on the SDP board.

Table 2-1. 120 Pin Connector Pin Assignments

Pin No.	Pin Name	Description
1	VIN	Power to SDP board. Requires 200mA @ 4 – 7 Volts.
2	NC	No Connect. Leave this pin unconnected. Do not ground.
3	GND	Connect to ground plane of board.
4	GND	Connect to ground plane of board.
5	USB_VBUS	Connected directly to the USB +5v Supply.
6	GND	Connect to ground plane of board.
7	PAR_D23	Parallel Data Bus Bit 23. ¹ (No connect.)
8	PAR_D21	Parallel Data Bus Bit 21. ¹ (No connect.)
9	PAR_D19	Parallel Data Bus Bit 19. ¹ (No connect.)

Connector Details

Table 2-1. 120 Pin Connector Pin Assignments (Cont'd)

Pin No.	Pin Name	Description
10	PAR_D17	Parallel Data Bus Bit 17. ¹ (No connect.)
11	GND	Connect to ground plane of board.
12	PAR_D14	Parallel Data Bus Bit 14.
13	PAR_D13	Parallel Data Bus Bit 13.
14	PAR_D11	Parallel Data Bus Bit 11.
15	PAR_D9	Parallel Data Bus Bit 9.
16	PAR_D7	Parallel Data Bus Bit 7.
17	GND	Connect to ground plane of board.
18	PAR_D5	Parallel Data Bus Bit 5.
19	PAR_D3	Parallel Data Bus Bit 3.
20	PAR_D1	Parallel Data Bus Bit 1.
21	PAR_RD	Asynchronous Parallel Read Strobe.
22	PAR_CS	Asynchronous Parallel Chip Select.
23	GND	Connect to ground plane of board.
24	PAR_A3	Parallel Address Bus Bit 3.
25	PAR_A1	Parallel Address Bus Bit 1.
26	PAR_FS3	Synchronous (PPI) Parallel Frame Sync 3.
27	PAR_FS1	Synchronous (PPI) Parallel Frame Sync 1.
28	GND	Connect to ground plane of board.
29	SPORT_DR3	SPORT Data Receive 3. ¹ (No connect.)
30	SPORT_DR2	SPORT Data Receive 2. ¹ (No connect.)
31	SPORT_DR1	SPORT Data Receive 1. Secondary SPORT Data into processor.
32	SPORT_DT1	SPORT Data Transmit 1. Secondary SPORT Data from processor.
33	SPORT_DT2	SPORT Data Transmit 2. ¹ (No connect.)
34	SPORT_DT3	SPORT Data Transmit 3. ¹ (No connect.)

Table 2-1. 120 Pin Connector Pin Assignments (Cont'd)

Pin No.	Pin Name	Description
35	SPORT_INT	SPORT Interrupt. Used to trigger a non-periodic SPORT event.
36	GND	Connect to ground plane of board.
37	SPI_SEL_B	SPI Chip Select B. Use this to control a second device on the SPI bus.
38	SPI_SEL_C	SPI Chip Select C. Use this for a third device on the SPI bus.
39	SPI_SEL1/SPI_SS	SPI Chip Select 1. ² (See Pin Sharing .) Used to connect to SPI Boot Flash if required. Also used as Chip Select when Blackfin processor is operating as SPI Slave.
40	GND	Connect to ground plane of board.
41	SDA_1	I ² C Data 1. ² (See Pin Sharing .)
42	SCL_1	I ² C Data 1. ² (See Pin Sharing .)
43	GPI00	General Purpose Input/Output.
44	GPI02	General Purpose Input/Output.
45	GPI04	General Purpose Input/Output.
46	GND	Connect to ground plane of board.
47	GPI06	General Purpose Input/Output. ² (See Pin Sharing .)
48	TMR_A	Timer A flag pin. Use as first Timer if required.
49	TMR_C	Timer C flag pin. ¹ (No connect.)
50	NC	No Connect. Leave this pin unconnected. Do not ground.
51	NC	No Connect. Leave this pin unconnected. Do not ground.
52	GND	Connect to ground plane of board.
53	NC	No Connect. Leave this pin unconnected. Do not ground.
54	NC	No Connect. Leave this pin unconnected. Do not ground.
55	NC	No Connect. Leave this pin unconnected. Do not ground.
56	EEPROM_A0	EEPROM A0. Connect to A0 Address line of the EEPROM
57	NC	No Connect. Leave this pin unconnected. Do not ground.

Connector Details

Table 2-1. 120 Pin Connector Pin Assignments (Cont'd)

Pin No.	Pin Name	Description
58	GND	Connect to ground plane of board.
59	UART_RX	UART Receive Data. ² (See Pin Sharing .)
60	$\overline{\text{RESET_IN}}$	Active low pin to reset EVAL-SDP-CB1Z board.
61	BMODE1	Boot Mode 1. Pull up with 10k Ω resistor to set SDP to boot from SPI Flash. Enabled on Connector A only.
62	UART_TX	UART Receive Data. ² (See Pin Sharing .)
63	GND	Connect to ground plane of board.
64	NC	No Connect. Leave this pin unconnected. Do not ground.
65	NC	No Connect. Leave this pin unconnected. Do not ground.
66	NC	No Connect. Leave this pin unconnected. Do not ground.
67	NC	No Connect. Leave this pin unconnected. Do not ground.
68	NC	No Connect. Leave this pin unconnected. Do not ground.
69	GND	Connect to ground plane of board.
70	NC	No Connect. Leave this pin unconnected. Do not ground.
71	NC	No Connect. Leave this pin unconnected. Do not ground.
72	TMR_D	Timer D flag pin. ² (See Pin Sharing .)
73	TMR_B	Timer B flag pin. Use as second Timer if required.
74	GPI07	General Purpose Input/Output. ² (See Pin Sharing .)
75	GND	Connect to ground plane of board.
76	GPI05	General Purpose Input/Output.
77	GPI03	General Purpose Input/Output.
78	GPI01	General Purpose Input/Output.
79	SCL_0	I ² C Clock 0. Daughter Board EEPROM must be connected to this bus.
80	SDA_0	I ² C Data 0. Daughter Board EEPROM must be connected to this bus.

Table 2-1. 120 Pin Connector Pin Assignments (Cont'd)

Pin No.	Pin Name	Description
81	GND	Connect to ground plane of board.
82	SPI_CLK	SPI Clock.
83	SPI_MISO	SPI Master In, Slave Out Data.
84	SPI_MOSI	SPI Master Out, Slave In Data.
85	SPI_SEL_A	SPI Chip Select A. Use this to control the first device on the SPI bus.
86	GND	Connect to ground plane of board.
87	SPORT_TSCCLK	SPORT Transmit Clock.
88	SPORT_DT0	SPORT Data Transmit 0. Primary SPORT Data from processor.
89	SPORT_TFS	SPORT Transmit Frame Sync.
90	SPORT_RFS	SPORT Receive Frame Sync.
91	SPORT_DR0	SPORT Data Receive 0. Primary SPORT Data into processor.
92	SPORT_RSCLK	SPORT Receive Clock
93	GND	Connect to ground plane of board.
94	PAR_CLK	Clock for Synchronous Parallel Interface (PPI).
95	PAR_FS2	Synchronous (PPI) Parallel Frame Sync 2.
96	PAR_A0	Parallel Address Bus Bit 0.
97	PAR_A2	Parallel Address Bus Bit 2.
98	GND	Connect to ground plane of board.
99	PAR_INT	Parallel Interrupt. Used to trigger a non-periodic Parallel event.
100	$\overline{\text{PAR_WR}}$	Asynchronous Parallel Write Strobe.
101	PAR_D0	Parallel Data Bus Bit 0.
102	PAR_D2	Parallel Data Bus Bit 2.
103	PAR_D4	Parallel Data Bus Bit 4.
104	GND	Connect to ground plane of board.
105	PAR_D6	Parallel Data Bus Bit 6.

Connector Details

Table 2-1. 120 Pin Connector Pin Assignments (Cont'd)

Pin No.	Pin Name	Description
106	PAR_D8	Parallel Data Bus Bit 8.
107	PAR_D10	Parallel Data Bus Bit 10.
108	PAR_D12	Parallel Data Bus Bit 12.
109	GND	Connect to ground plane of board.
110	PAR_D15	Parallel Data Bus Bit 15.
111	PAR_D16	Parallel Data Bus Bit 16. ¹ (No connect.)
112	PAR_D18	Parallel Data Bus Bit 18. ¹ (No connect.)
113	PAR_D20	Parallel Data Bus Bit 20. ¹ (No connect.)
114	PAR_D22	Parallel Data Bus Bit 22. ¹ (No connect.)
115	GND	Connect to ground plane of board.
116	VI0(+3.3V)	+3.3V Output. 20mA max current available to power IO voltage on daughter board.
117	GND	Connect to ground plane of board.
118	GND	Connect to ground plane of board.
119	NC	No Connect. Leave this pin unconnected. Do not ground.
120	NC	No Connect. Leave this pin unconnected. Do not ground.

1 Functionality not implemented on the EVAL-SDP-CB1Z.

2 Shared across both connectors.

Each interface provided by the SDP is available on unique pins of the SDP's 120 pin connector. The connector pin numbering scheme is outline in [Figure 2-2](#).

Hardware Description

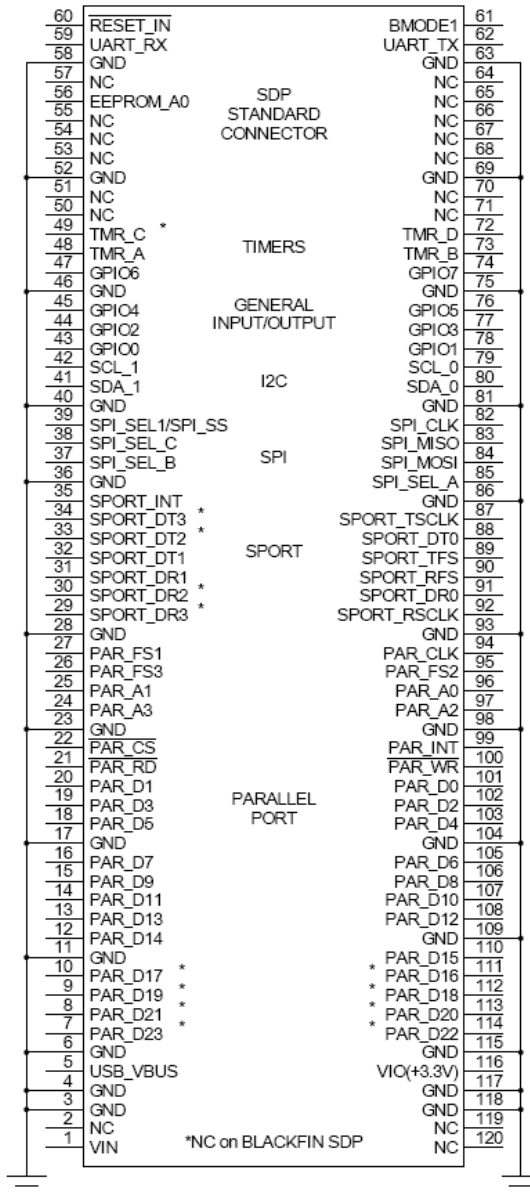


Figure 2-2. 120 Pin Connector Outline

Pin Sharing

Two types of pin sharing occur on the SDP board and must be taken into account when using two or more of the connector's peripherals interfaces between a daughter board and the SDP board. The first type is pin sharing that occurs internally in the Blackfin processor. The second type is pin sharing that occurs when a single Blackfin processor output pin is shared across both connector A and connector B.

Internal Blackfin processor pin sharing can restrict the simultaneous availability of peripheral interfaces on a single connector or across both connectors. The Blackfin processor's internal design has multiple signals physically sharing each single output pin. As mentioned previously, the pins on the 120 pin connector were defined independently of this pin sharing. This has the effect of limiting the peripherals which can be used simultaneously on the SDP. A system designer must consult the *ADSP-BF52x Blackfin Processor Hardware Reference* for the ADSP-BF527 processor to ensure the selected peripherals are available simultaneously and their signals do not share Blackfin processor output pins. An example of this sharing is that the SPORT and PPI peripherals physically share the same Blackfin processor pins. Therefore, these two interfaces cannot be utilized in a single application.

Pin sharing also occurs from certain Blackfin processor output pins to both Connector A and Connector B. The following signals are connected from a single Blackfin processor output pin to both Connector A and Connector B:

- I²C Bus 1, pins 42 and 43
- SCL 0 on I²C Bus 0, pin 79
- GPIO 6 and GPIO 7, pins 47 and 67
- Timer D, pin 72
- UART, pins 59 and 62

Power

The SDP board requires that any daughter board connected to the SDP board provides the SDP board with 5V @ 200mA. This supply should be made available on Pin 1 (VIN) of the 120 pin connector. This supply is required to power the Blackfin processor, the memory, and the other components on the SDP Board. The SDP board also provides 3.3V @ 20mA on Pin 116 (VIO_3.3) to connected daughter boards as the VIO voltage for the daughter board. Pin 5 (USB_VBUS) is connected to the +5V line of the USB connector, providing 5V+/- 10% as an output of the SDP board.

Daughter Board Design Guidelines

The daughter board design guidelines specify the layout, connector position, keep out areas and dimensions of potential daughter boards. This guidance is to ensure that a daughter board can connect off either Connector A or Connector B of the SDP board. Following these guidelines ensures that both connectors on the SDP can have any one of the catalogue of daughter boards physically attached to the connectors simultaneously.

Connector Location

The daughter board connector and securing screw holes are to be located in the top left hand corner. This arrangement can be seen for Daughter Board A in [Figure 2-3](#). Note Daughter Board B is the same as A rotated clockwise through 90°. The exact location of the connector from the board's edge is important in order to allow both boards connect at the same time. As can be seen in [Figure 2-3](#), if either board exceeds these dimensions, it is not possible to connect the other. Every effort was made to extend the 5.9mm dimension as large as possible in order to allow space for vias between the connector and the edge of the board. These are abso-

Daughter Board Design Guidelines

lute max dimensions and should not be exceeded. See [Figure 2-3](#) for further details.

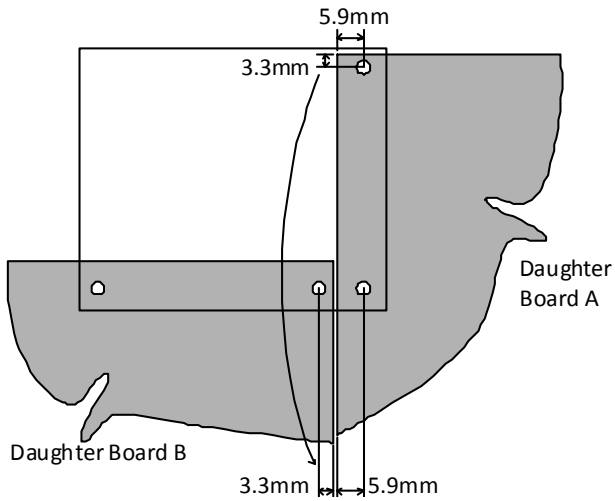


Figure 2-3. Maximum Board Dimensions for Connector Placement

The full specification drawing for the connector location on the daughter board can be seen in [Figure 2-4](#).

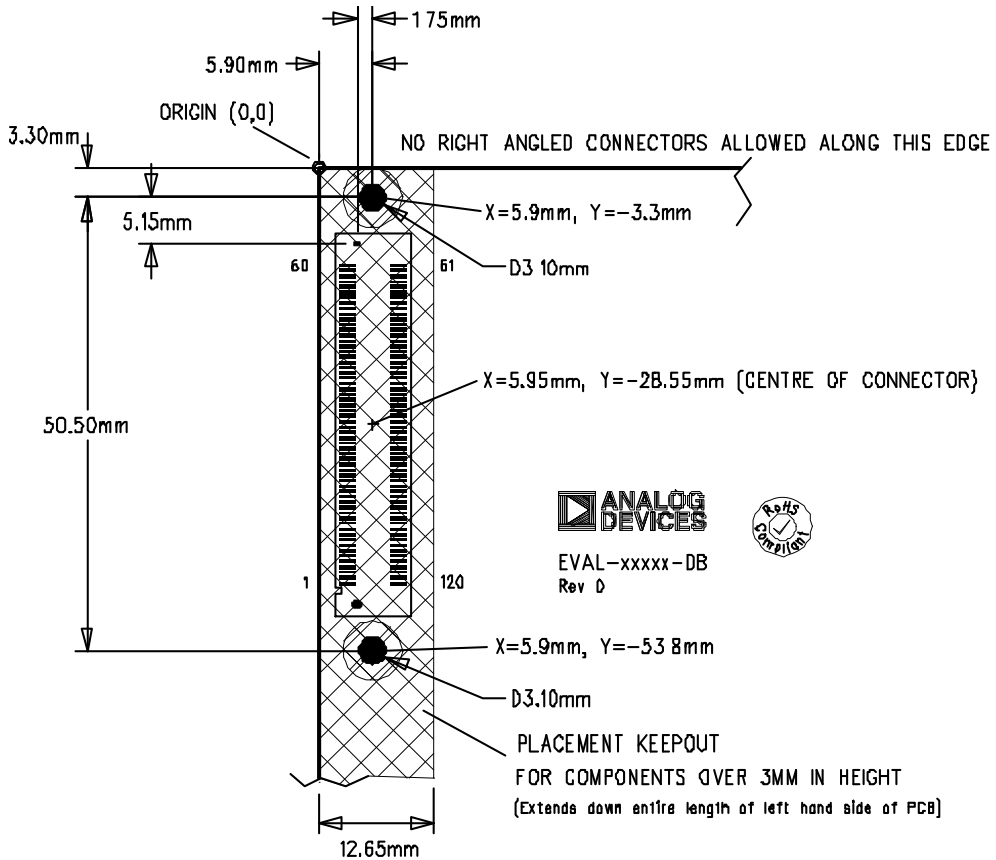


Figure 2-4. Connector Placement on Compatible Daughter Board

The mating daughter board 120 pin connector is the Hirose FX8-120S-SV(21), 120-pin receptacle, FEC 132-4660, Digikey H1219-ND. Please consult the connector's data sheet for full details on the connector. Note pins 1 to 60 are placed on the left side of the connector and pins 61 to 120 are placed on the right side of the connector.

Mechanical Specifications

Keep Out Area

In order to allow the greatest flexibility for future controller boards, a keepout area is established for components higher than 3mm. The keepout area is 12.65mm wide and extends down the entire left side of the daughter board.

Restriction on Right Angle Connectors

Due to the close proximity of the edges of daughter boards A and B (seen in [Figure 2-3 on page 2-12](#)) right angle connectors are not allowed on the top and left edges of the daughter boards and (if required) should be placed on the right or bottom edges. The phrase "right angle connector" is used to describe any connector that requires the connection to protrude over the edge of the board (for example, right angle SMB or screw terminal)

Mechanical Specifications

The mechanical specifications of the SDP board are 2.75" x 2.25" (69.85mm x 27.15mm). The height of the 120 pin connectors from the bottom of the board is approximately 0.152" (3.86 mm). The tallest component on the top is approximately 0.125" (3.175 mm), and the tallest components on the bottoms are the connectors at approximately 0.152" (3.86 mm). Refer to [Figure 2-5](#).

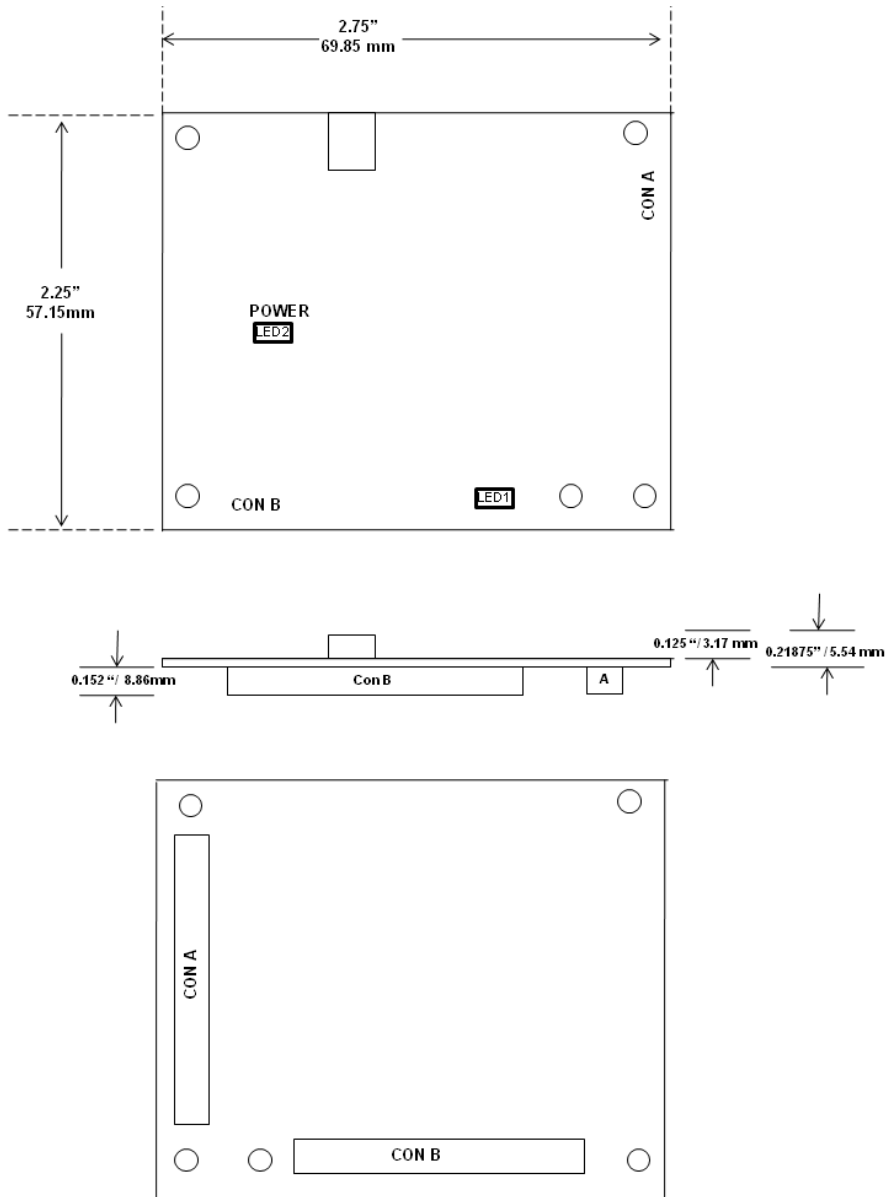


Figure 2-5. SDP Board Mechanical Specifications

Mechanical Specifications

3 SCHEMATIC

This chapter provides the schematic drawings for the EVAL- SDP -CB1Z board. The schematic pages include:

- System Development Platform—Power
- System Development Platform—Memory
- System Development Platform—Clocks_USB
- System Development Platform—Blackfin_I/O
- System Development Platform—Connector A
- System Development Platform—Connector B

6

5

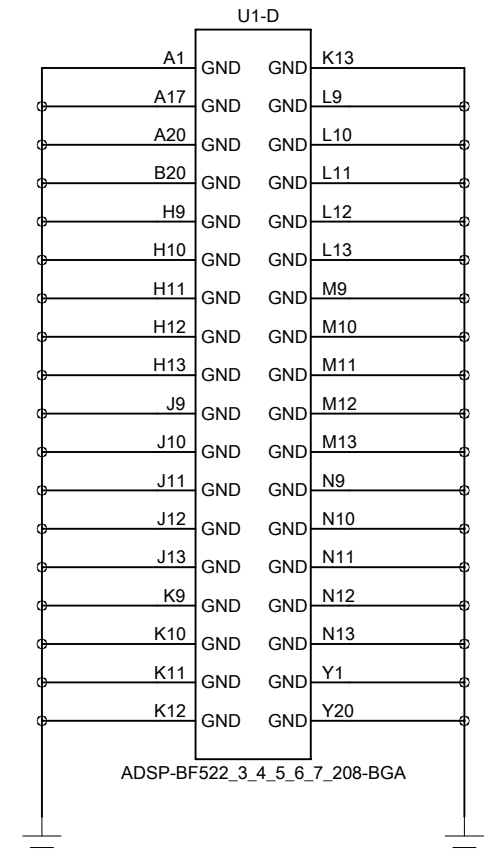
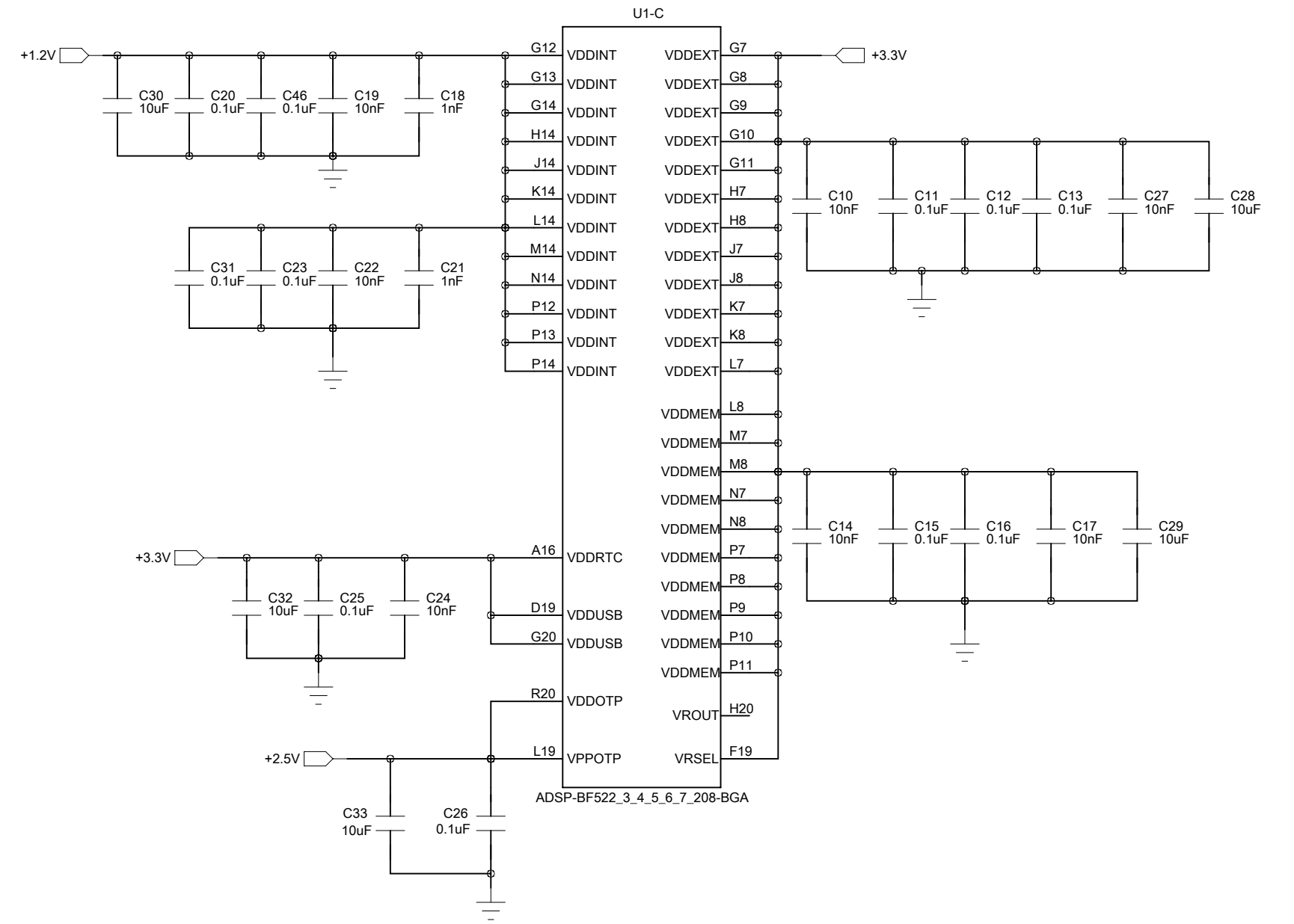
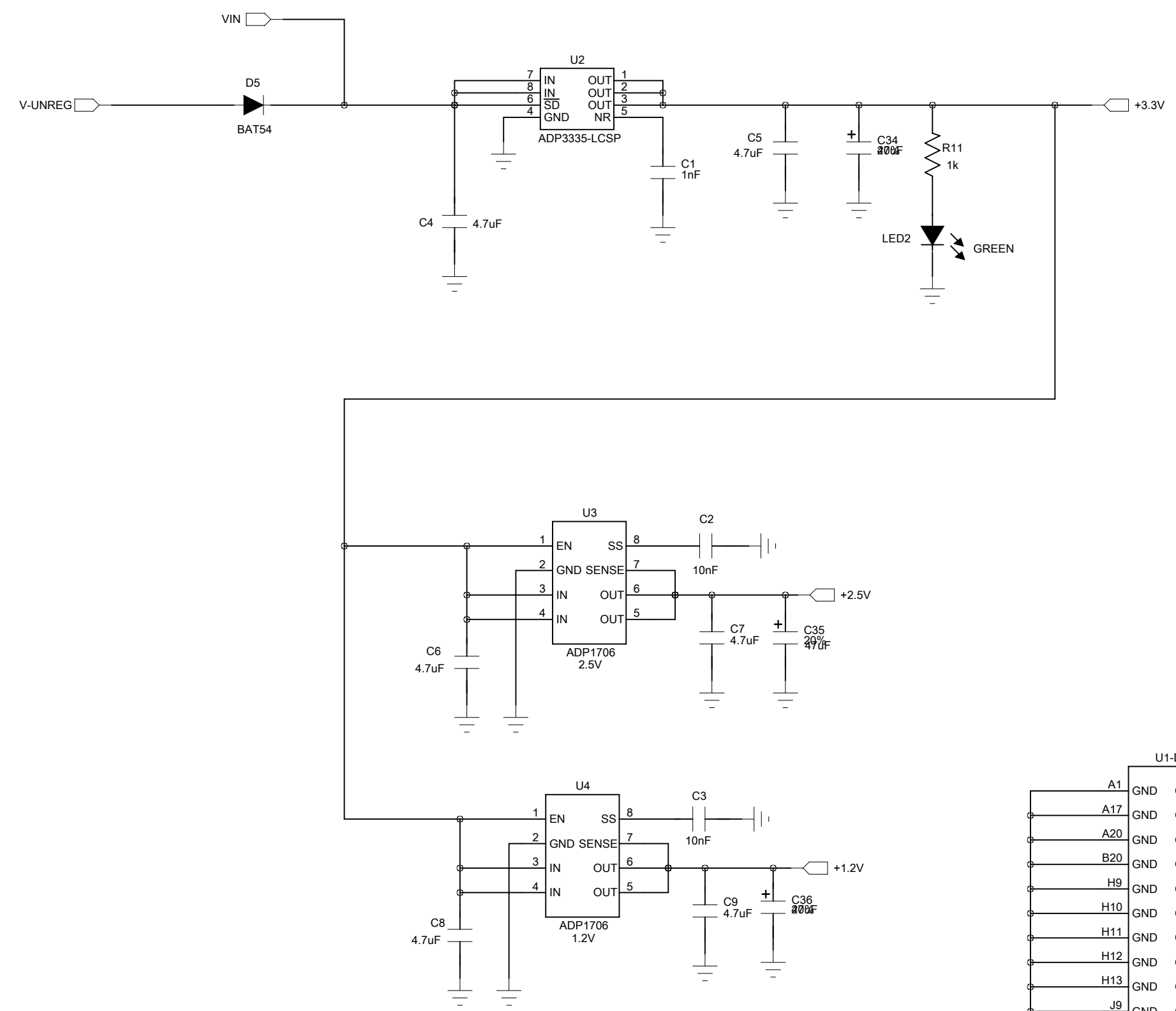
4

3

2

1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: ANALOG DEVICES			
TITLE: SYSTEM DEVELOPMENT PLATFORM POWER			
CODE:	SIZE:	DRAWING NO:	REV: B
SCALE:		SHEET: 1 OF 6	

DRAWN:	DATED: 13-01-09
CHECKED:	DATED: 14-01-10
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

D
C
B
A

D
C
B
A

6

5

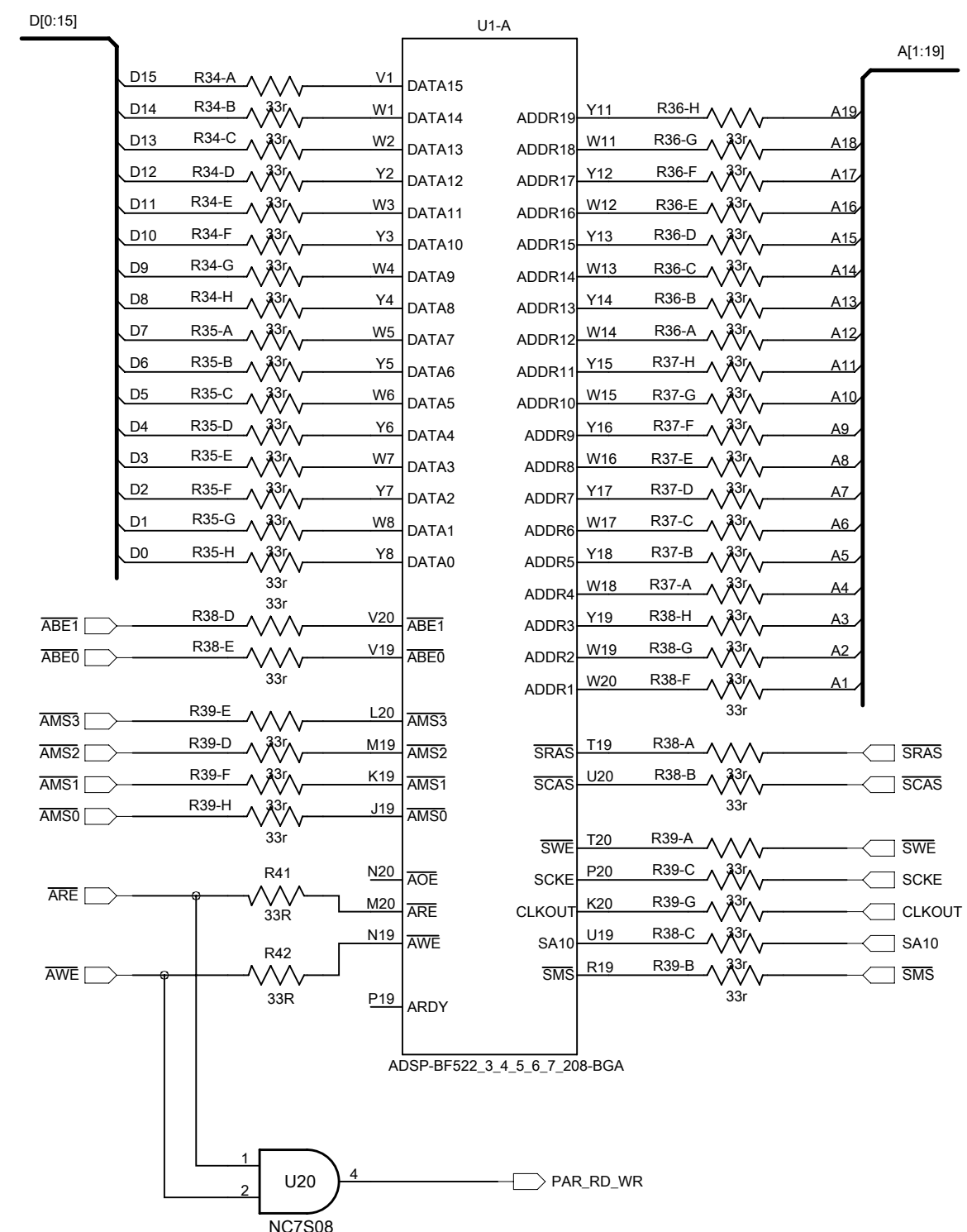
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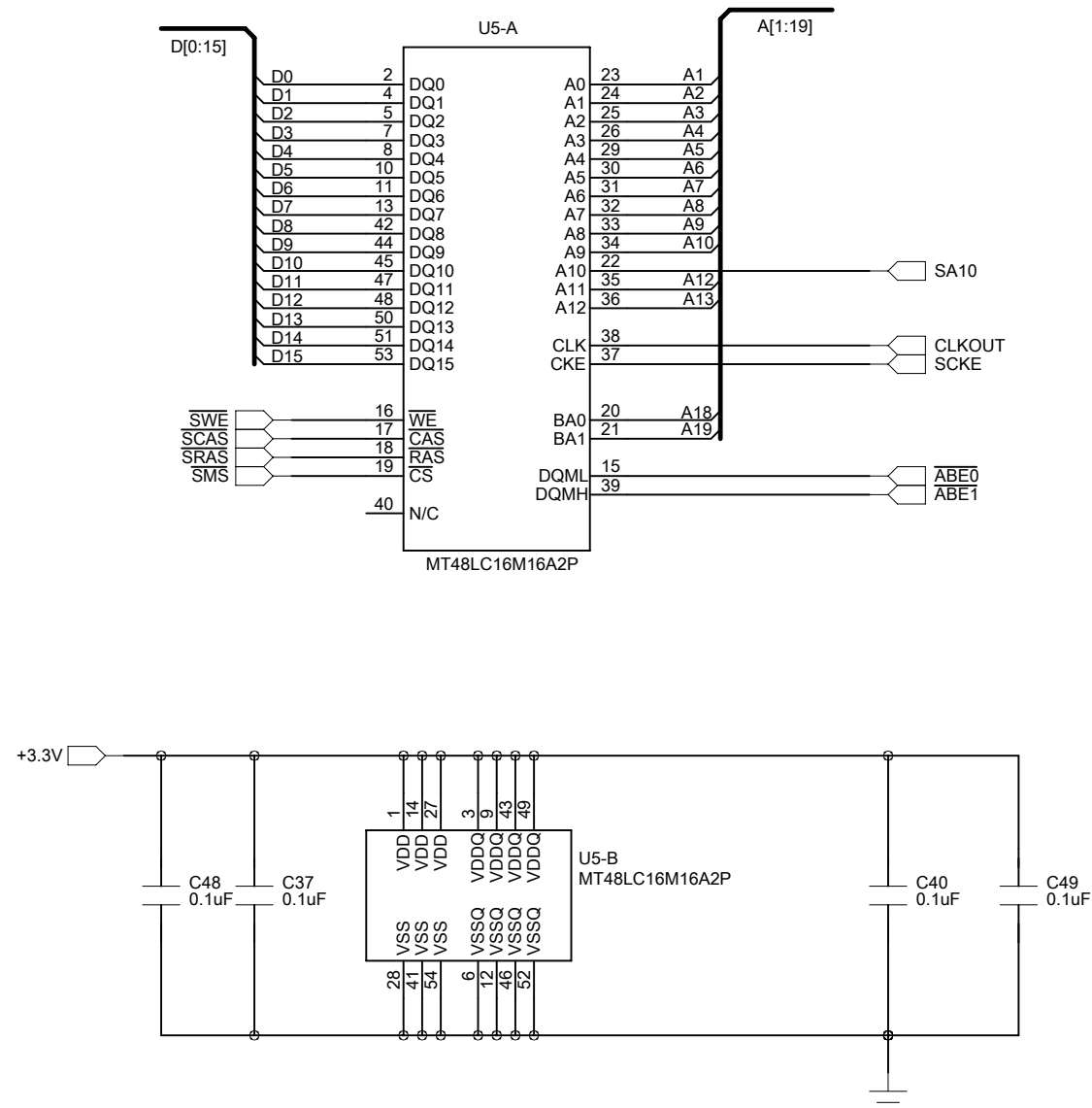
2

1

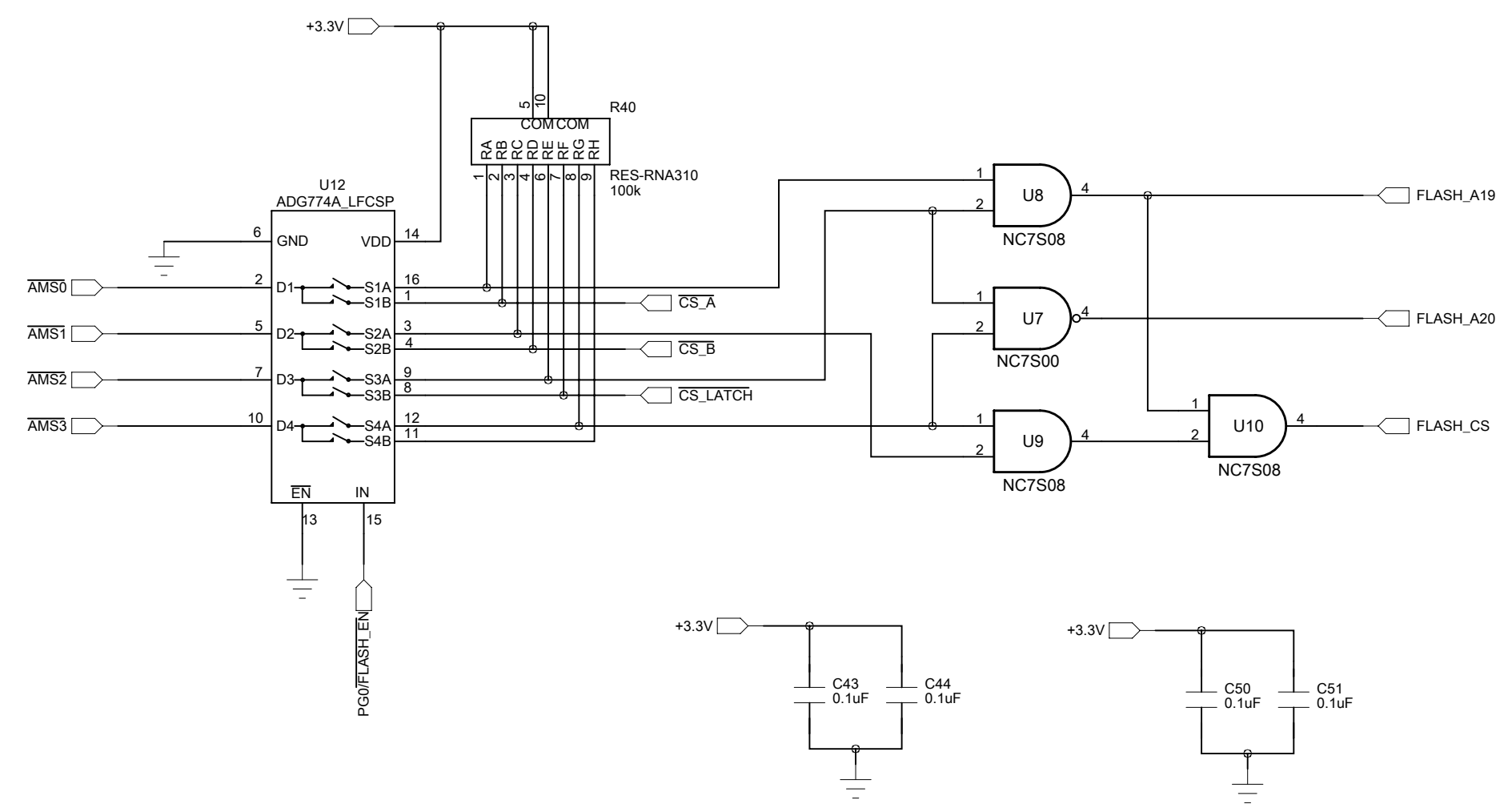
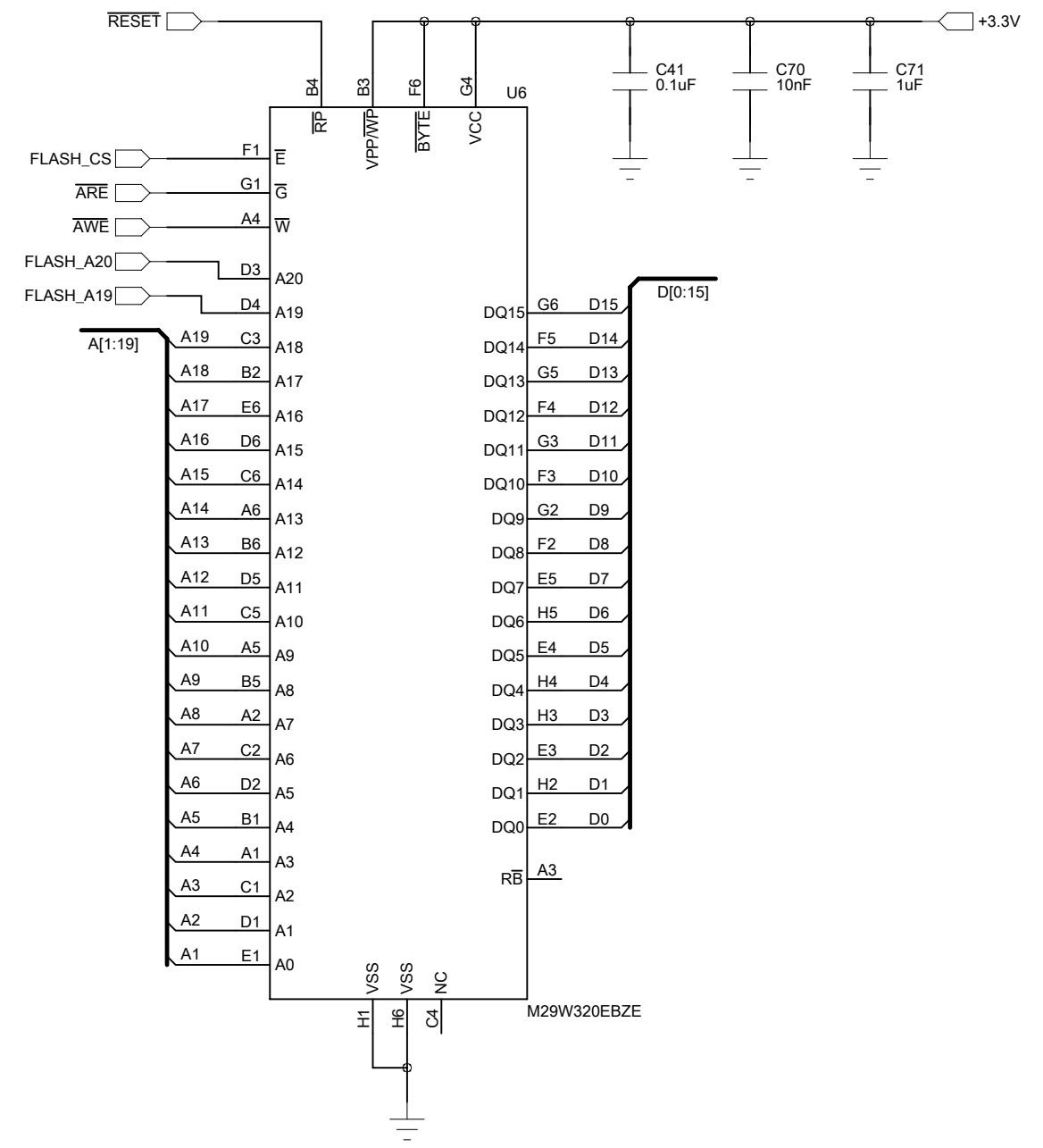
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



32 MByte SDRAM
* Fit part MT48LC16M16A2P-75:D for 32 MByte SDRAM



4MByte Flash



COMPANY: ANALOG DEVICES			
TITLE: SYSTEM DEVELOPMENT PLATFORM (MEMORY)			
CODE:	SIZE:	DRAWING NO:	REV:
		SDP1Z	B
SCALE:			SHEET: 2 OF 6

DRAWN:	DATED: 13-01-09
CHECKED:	DATED: 14-01-10
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

6

5

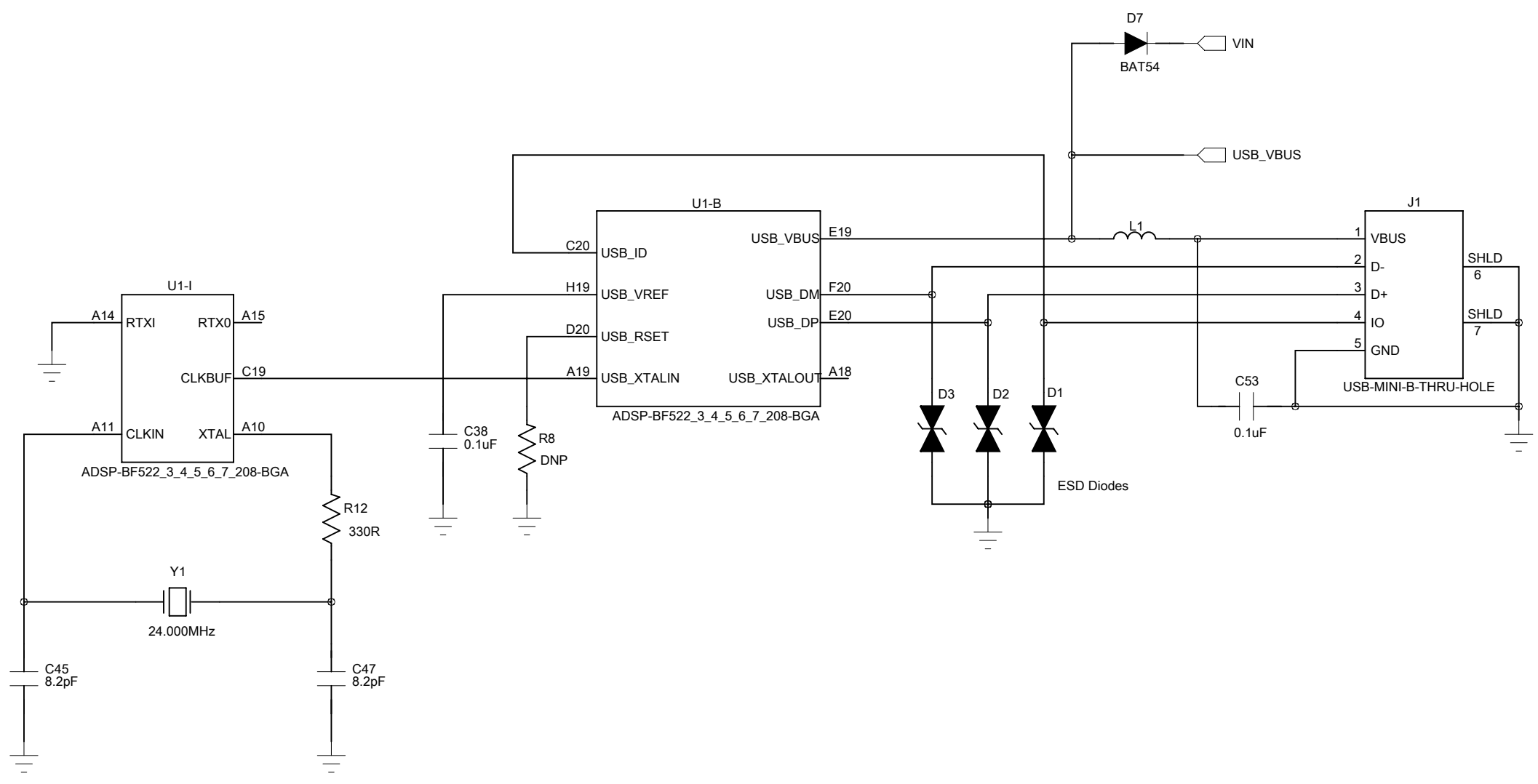
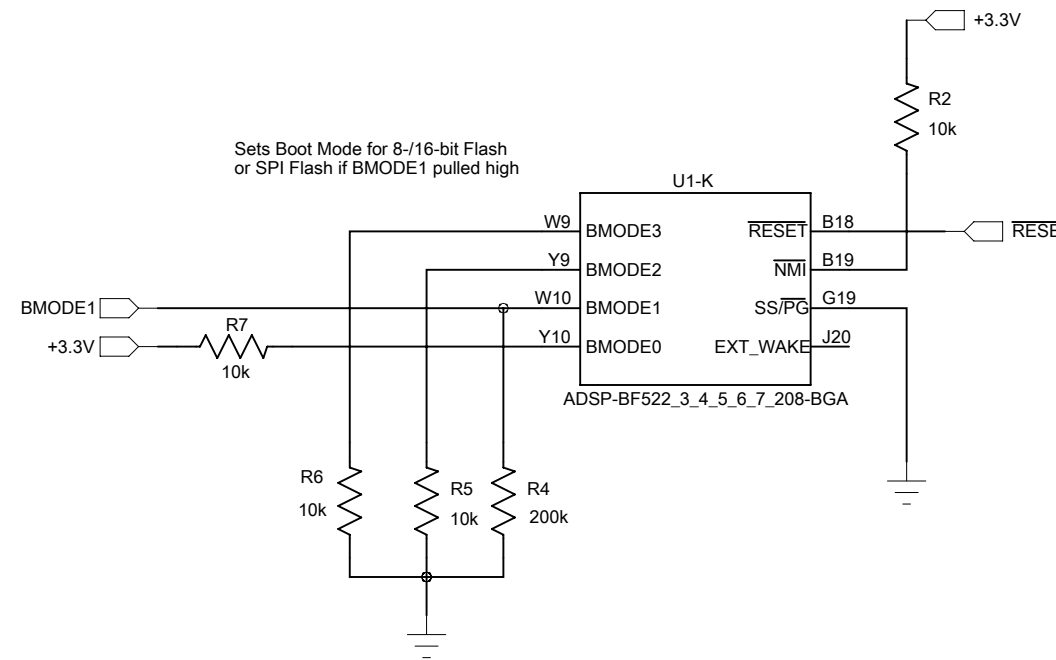
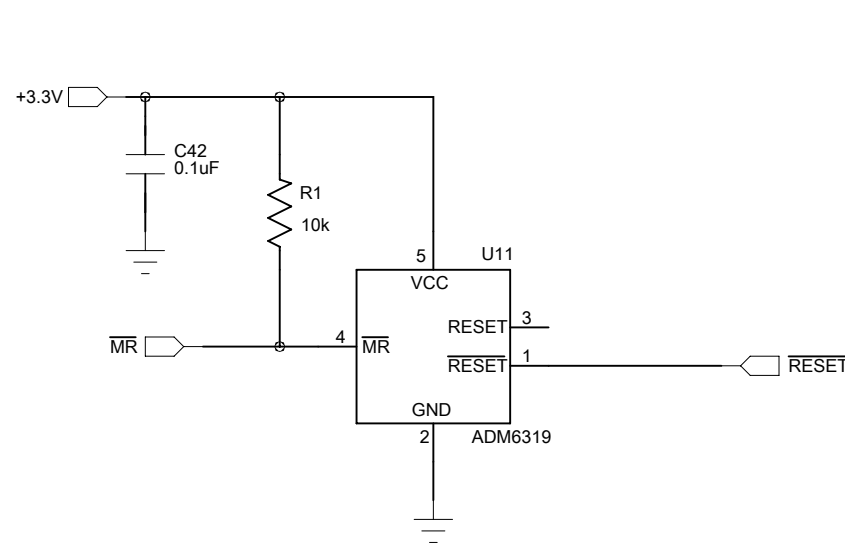
4

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2

1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: ANALOG DEVICES			
TITLE: SYSTEM DEVELOPMENT PLATFORM (CLOCKS_USB)			
DRAWN:	DATED: 13-01-09	CODE:	SIZE:
CHECKED:	DATED: 14-01-10	DRAWING NO: SDP1Z	
QUALITY CONTROL:	DATED:	REV: B	
RELEASED:	DATED:	SCALE:	
SHEET: 3 OF 6			DATE:

6

5

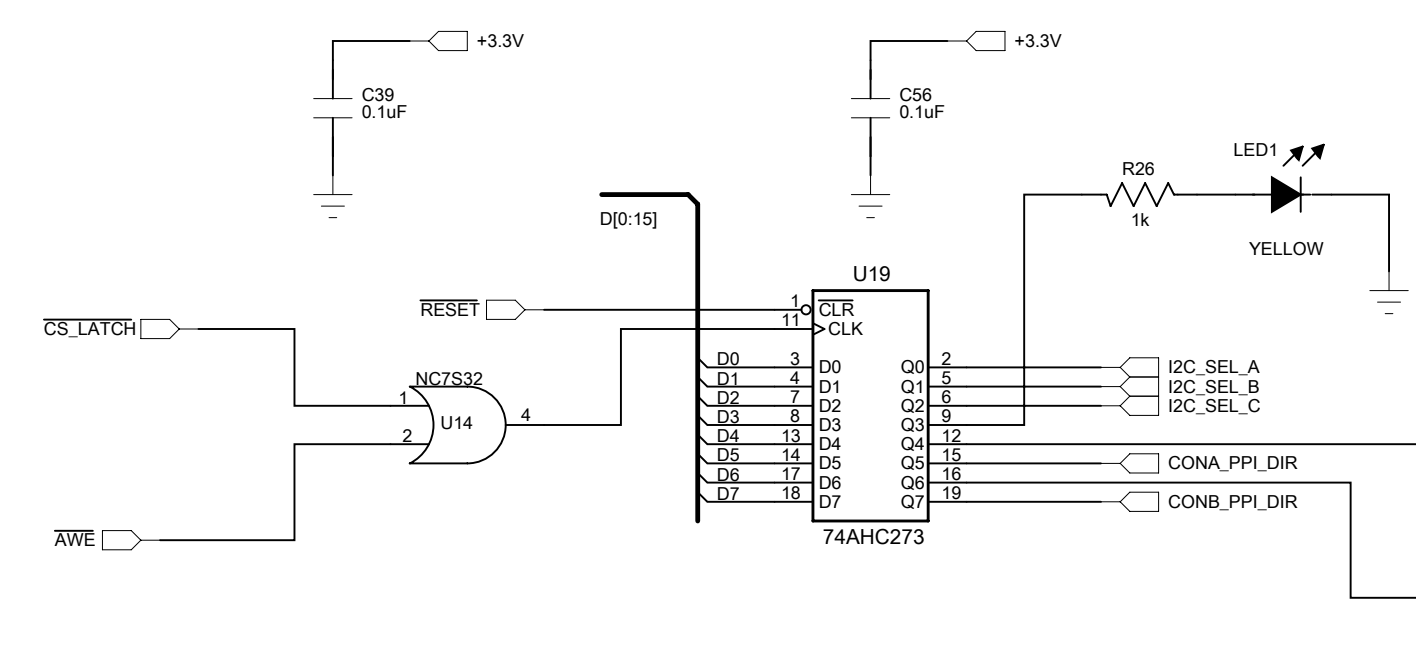
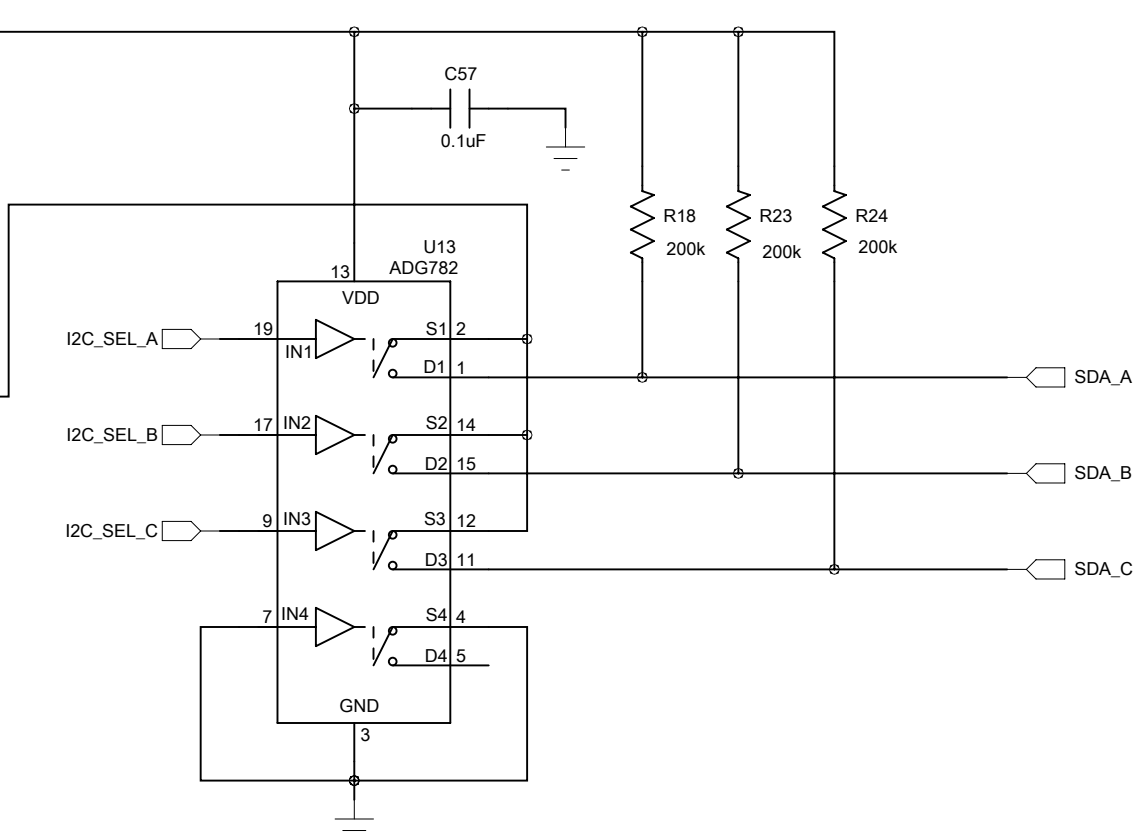
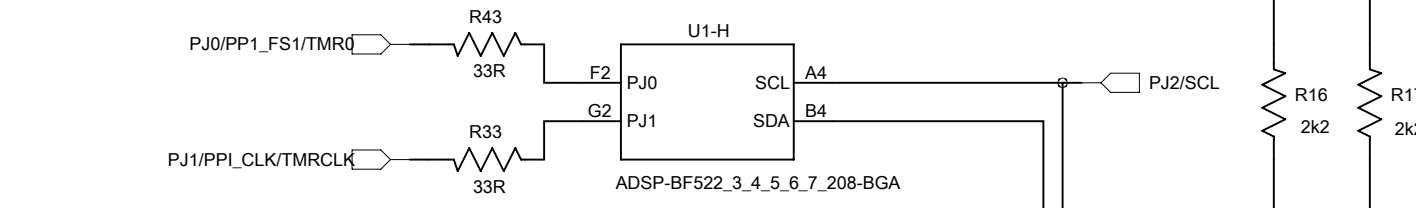
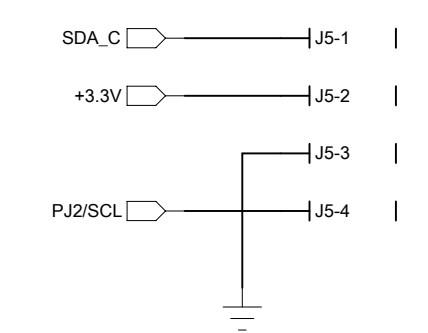
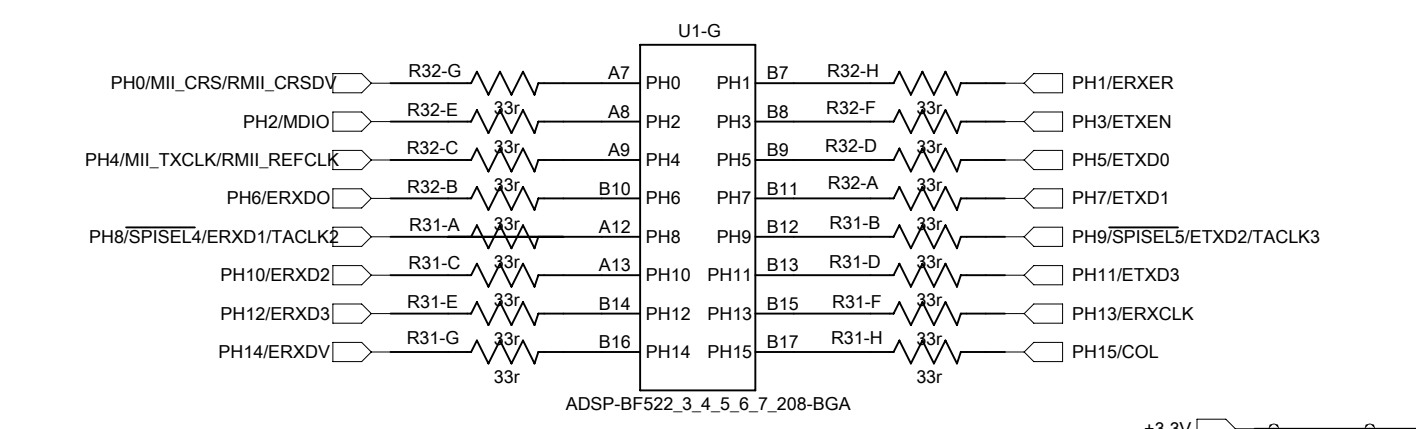
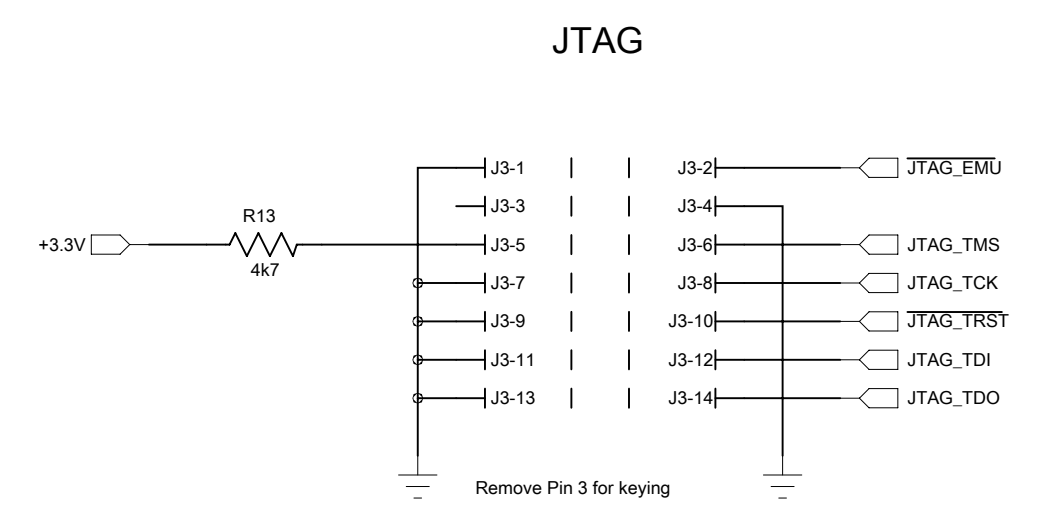
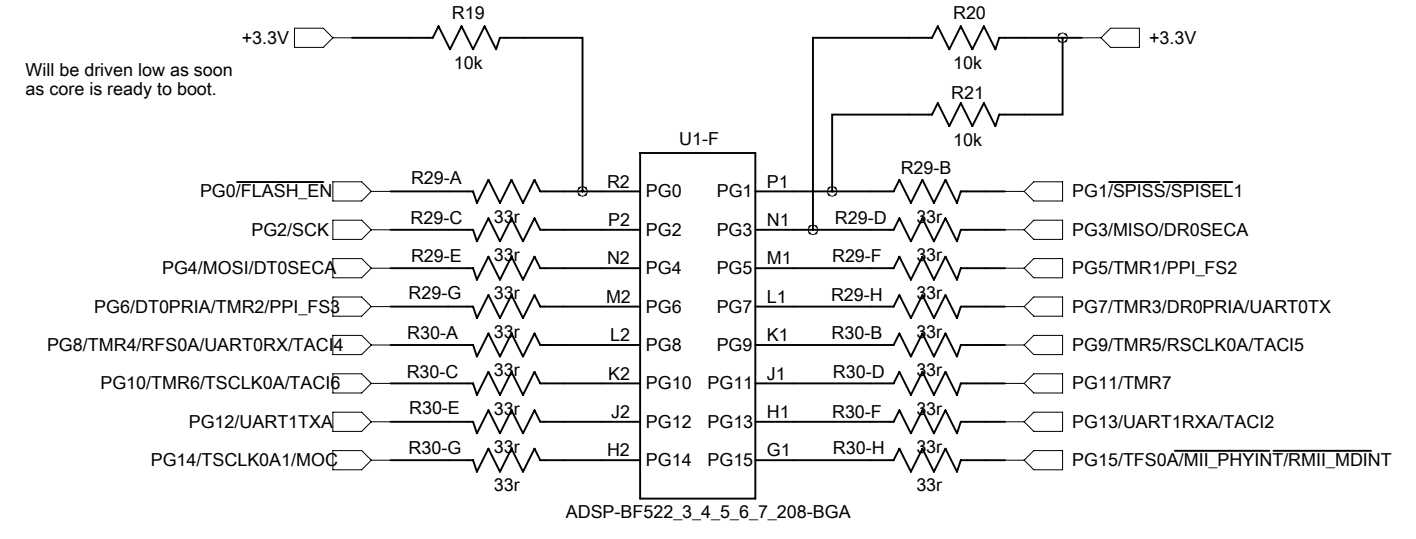
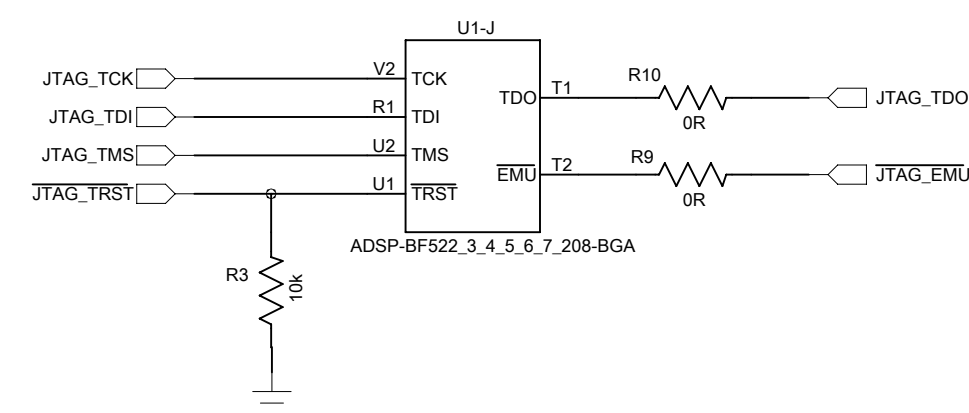
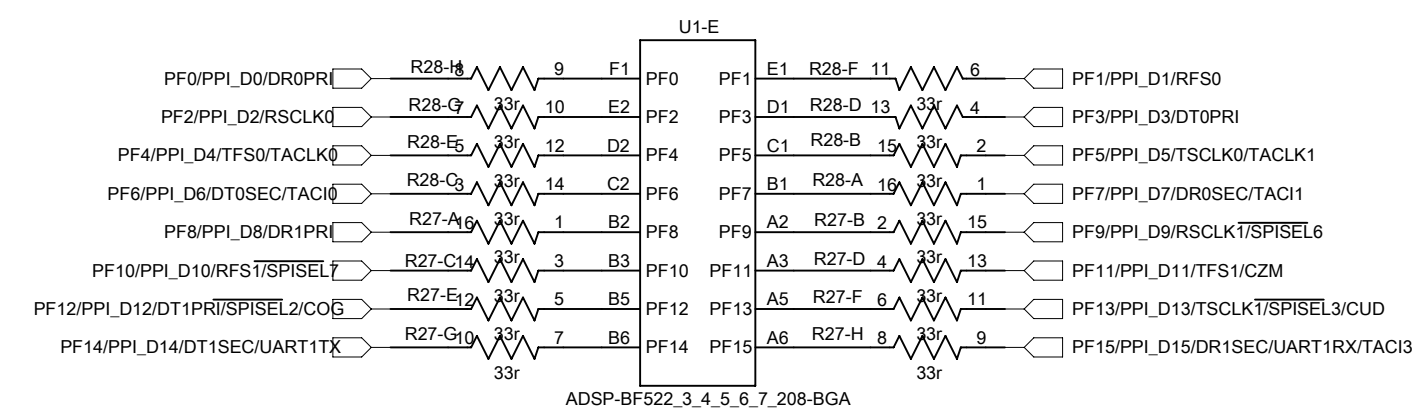
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1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DRAWN:	DATED: 13-01-09
CHECKED:	DATED: 14-01-10
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY: **ANALOG DEVICES**

TITLE: **SYSTEM DEVELOPMENT PLATFORM (BLACKFIN I/O)**

CODE:	SIZE:	DRAWING NO:	REV:
		SDP1Z	B

SCALE: SHEET: 4 OF 6

6

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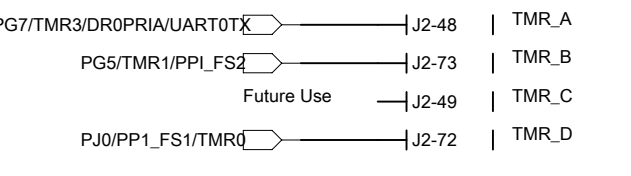
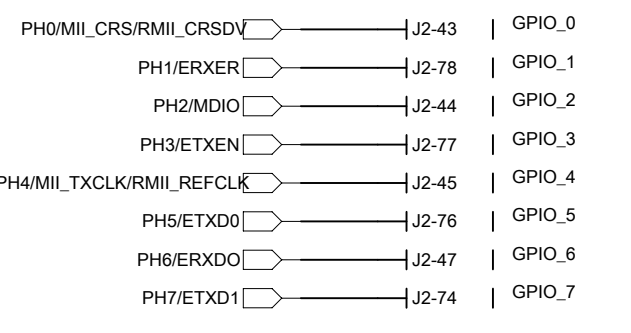
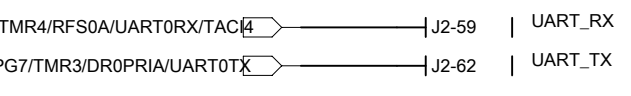
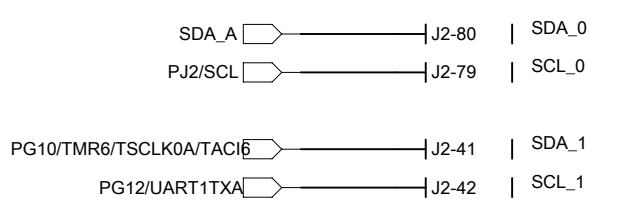
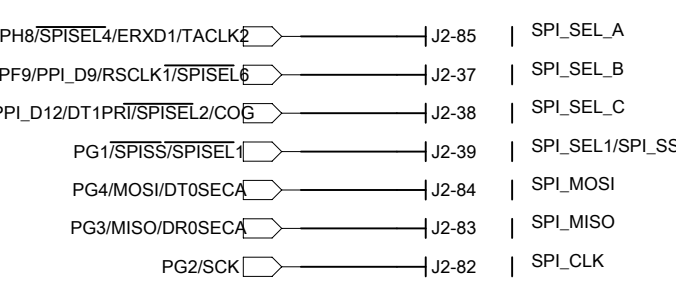
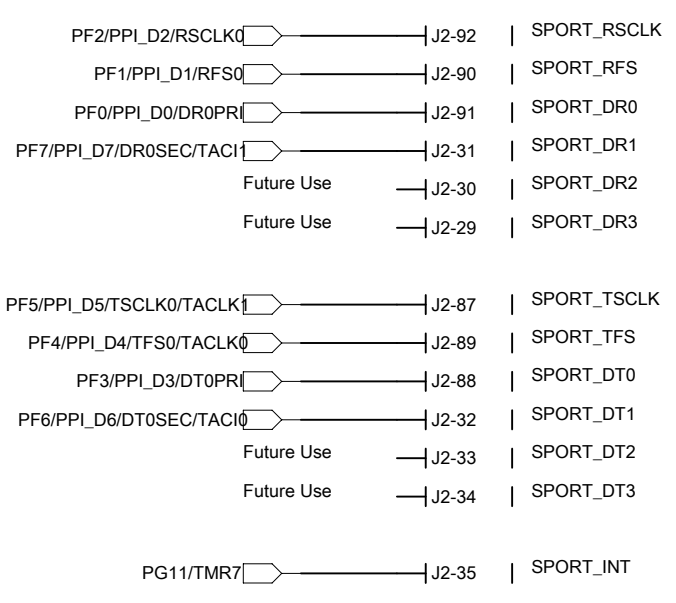
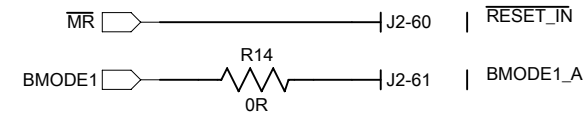
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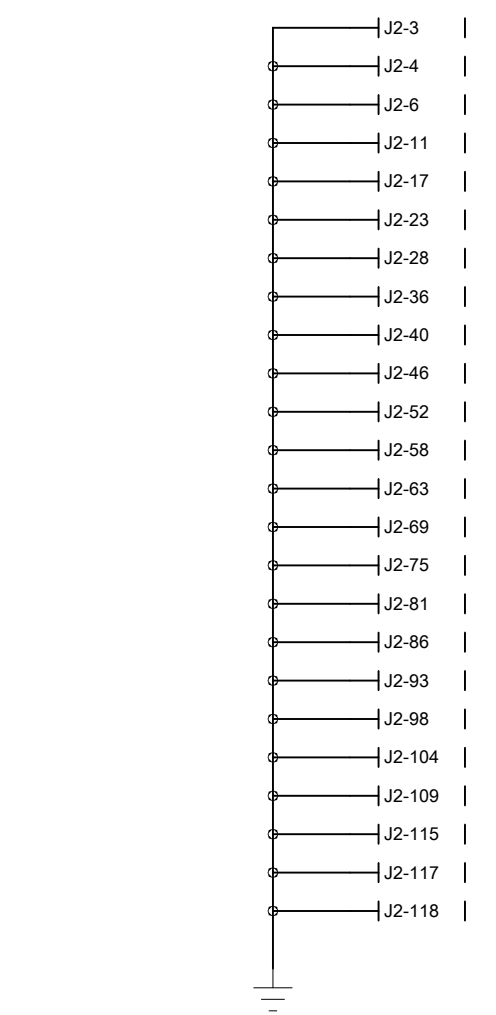
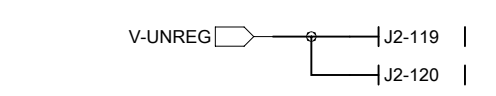
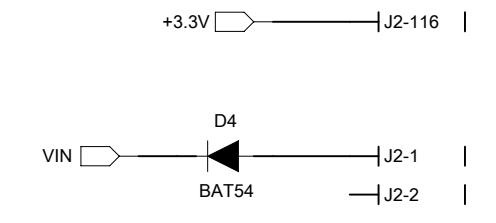
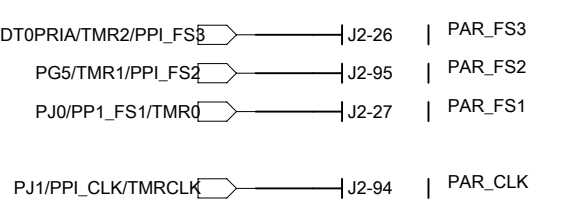
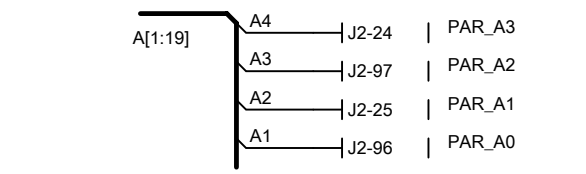
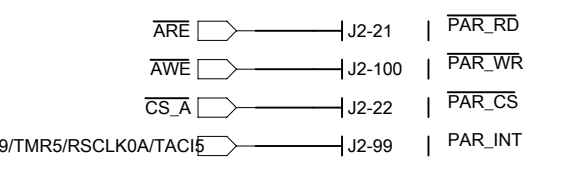
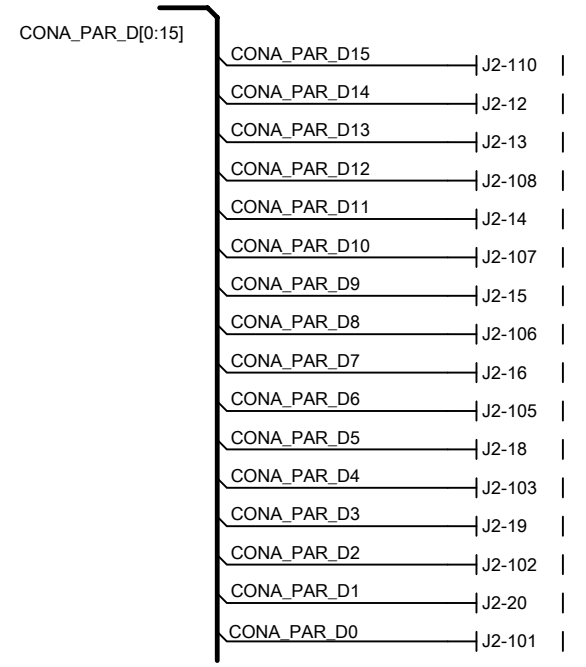
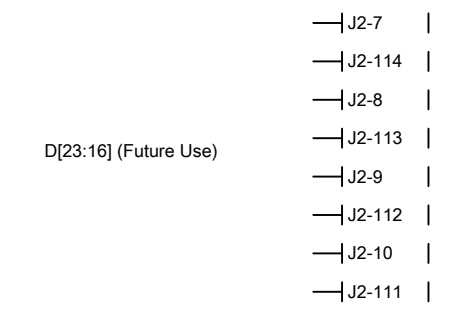
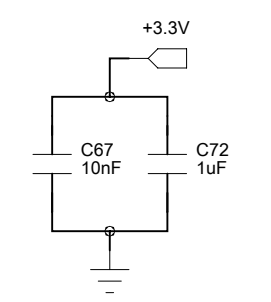
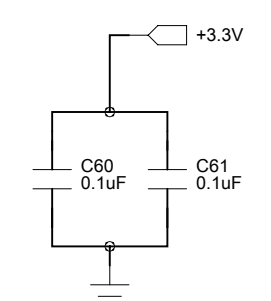
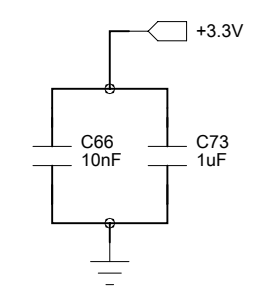
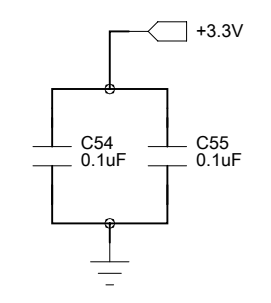
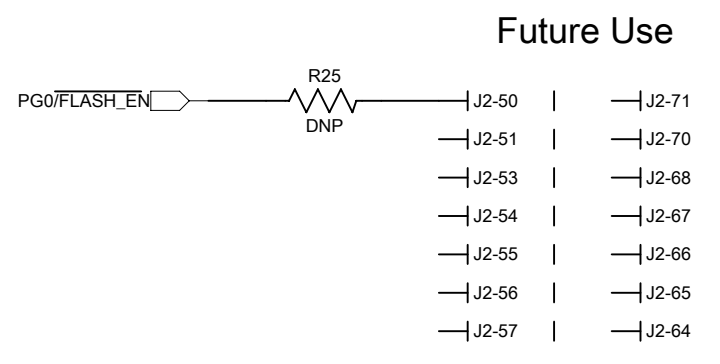
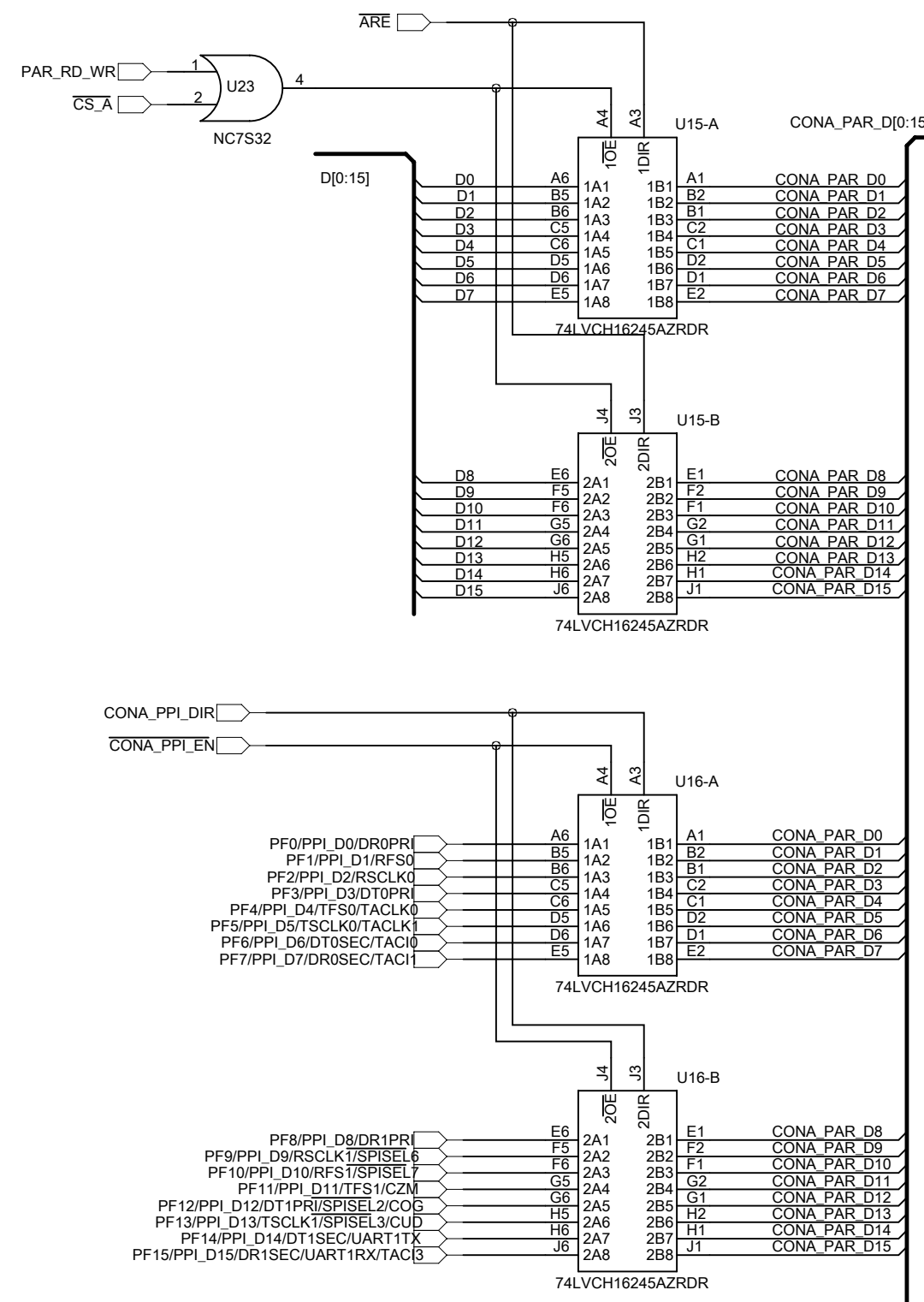
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1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DIR=1: A->B; DIR=0: B->A



COMPANY: ANALOG DEVICES			
TITLE: SYSTEM DEVELOPMENT PLATFORM (CONNECTOR A)			
DRAWN:	DATED: 13-01-09	CODE:	SIZE:
CHECKED:	DATED: 14-01-10	DRAWING NO:	REV: B
QUALITY CONTROL:	DATED:	SDP1Z	
RELEASED:	DATED:		
SCALE:		SHEET: 5 OF 6	

6

5

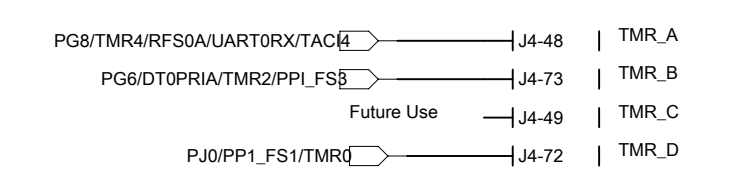
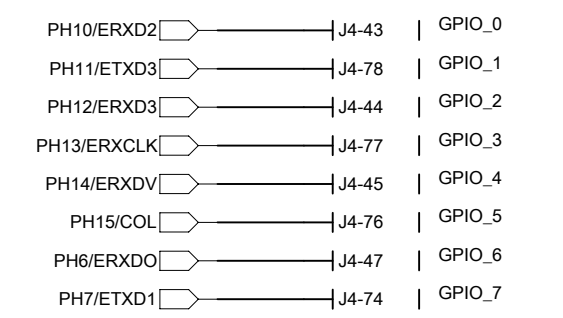
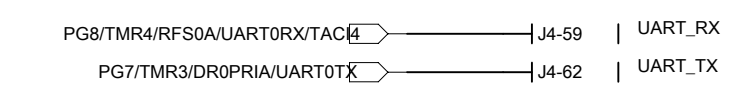
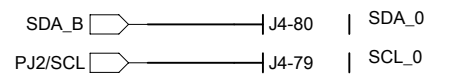
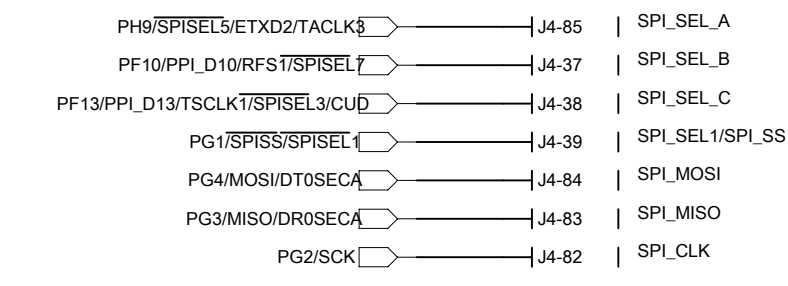
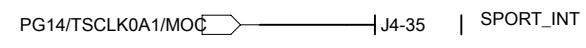
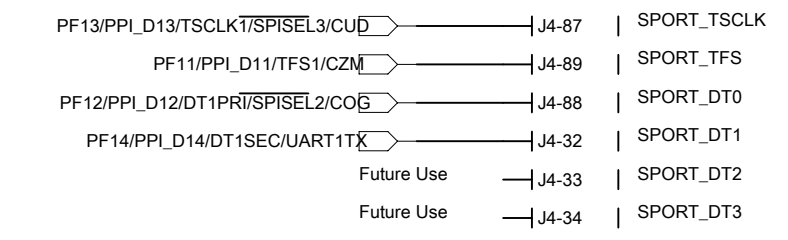
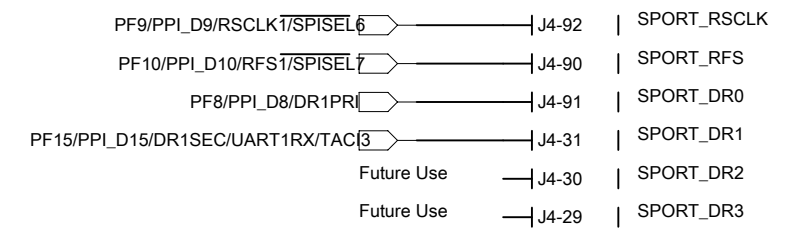
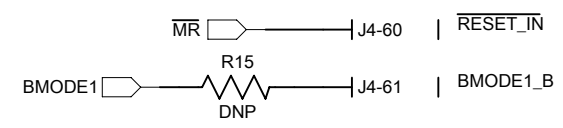
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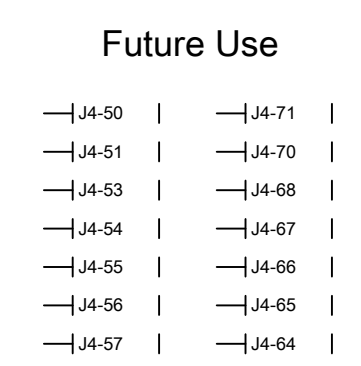
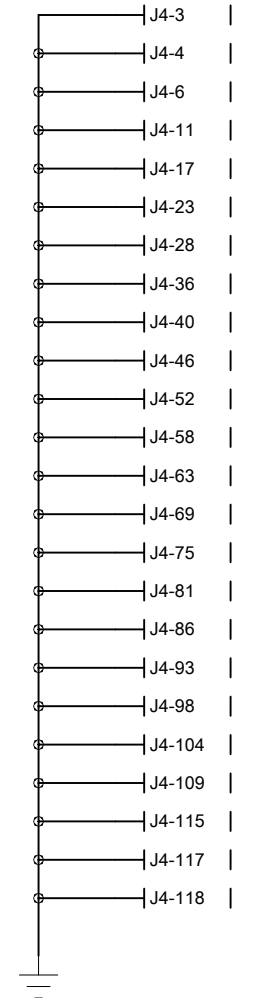
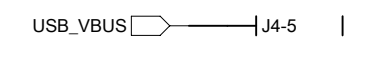
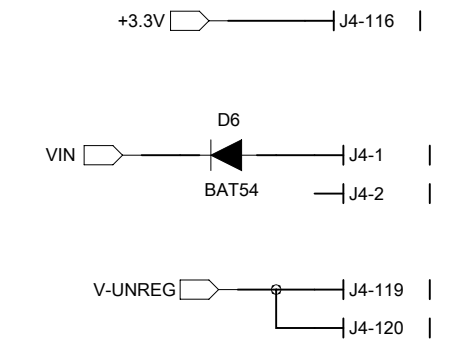
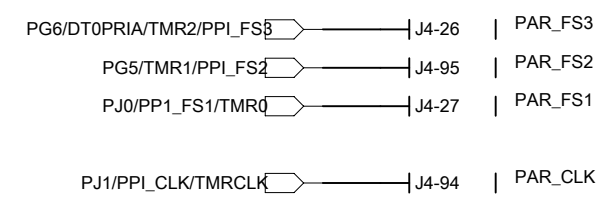
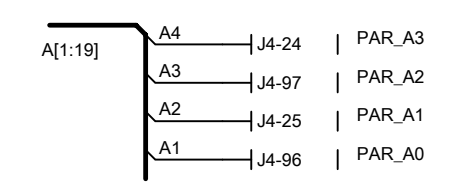
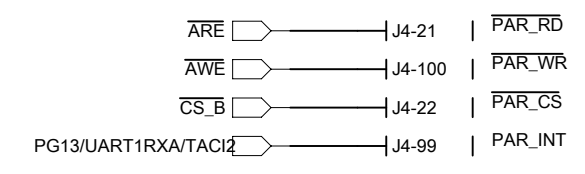
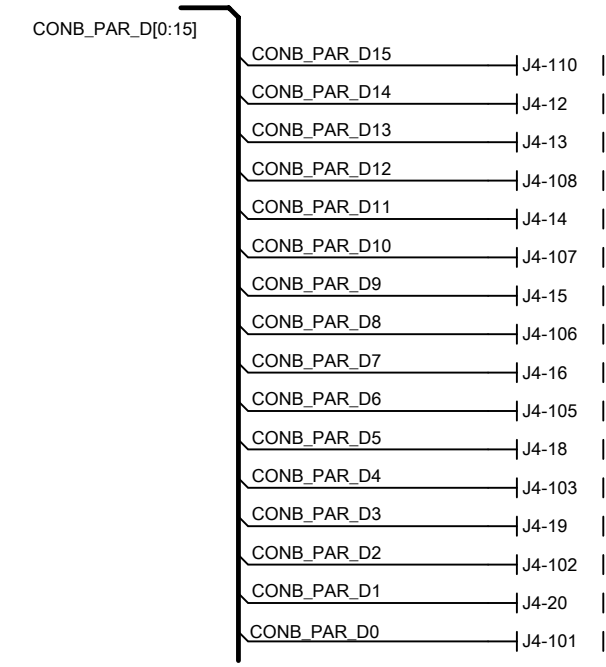
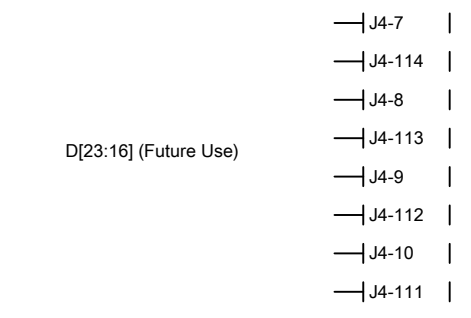
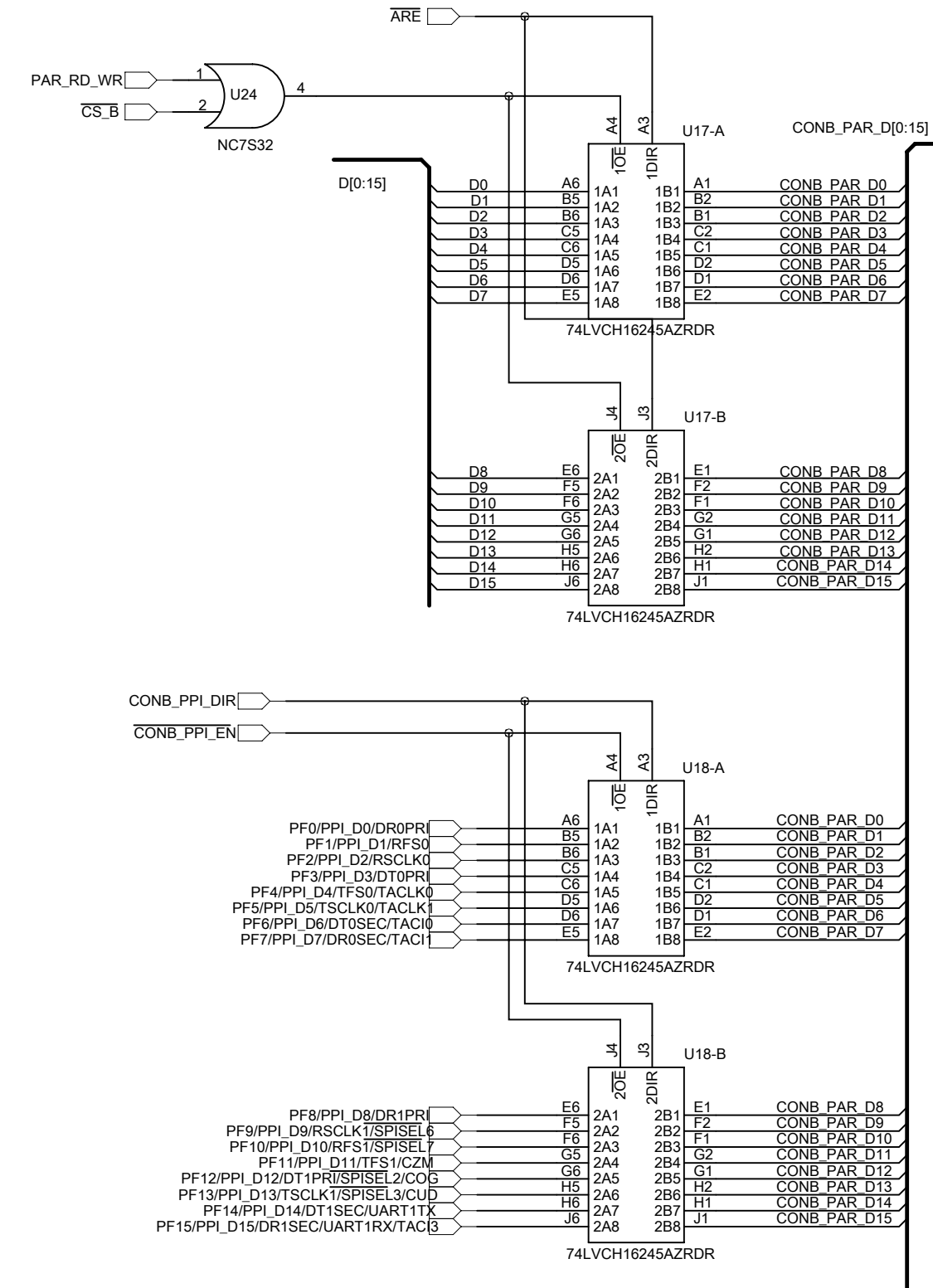
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1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DIR=1: A->B; DIR=0: B->A



COMPANY: ANALOG DEVICES			
TITLE: SYSTEM DEVELOPMENT PLATFORM (CONNECTOR B)			
DRAWN:	DATED: 13-01-09	CODE:	SIZE:
CHECKED:	DATED: 14-01-10	DRAWING NO:	REV: B
QUALITY CONTROL:	DATED:	SDP1Z	
RELEASED:	DATED:	SCALE:	SHEET: 6 OF 6